UMC

UM92870 Series

Integrated DTMF Receiver

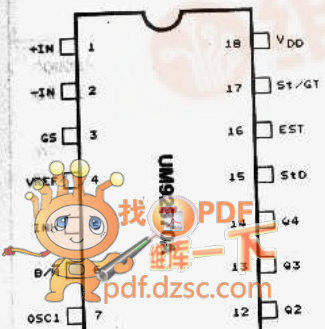
Features

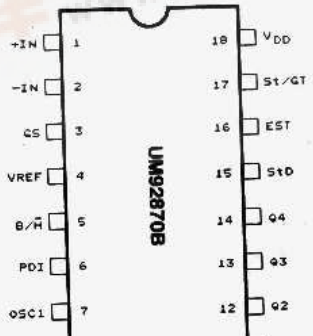
- Full DTMF receiver in single 18-pin package
- Single 5-volt power supply
- Internal gain setting amplifier
- Adjustable guard time
- Built-in dial-tone filter
- Uses inexpensive 3.5795 MHz crystal
- CMOS for low power consumption
- Tristate outputs
- Early steering output

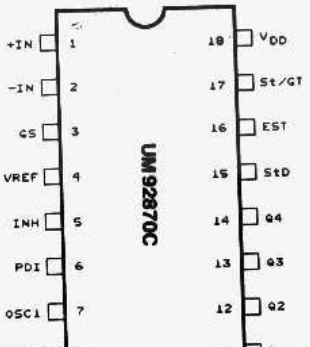
General Description

The UM92870 is a complete DTMF receiver designed to detect standard DTMF signals. It includes a differential input amplifier, filter section, decoder section, and steering logic circuits. The differential input amplifier allows adjustment of gain and choice of input configuration. The filter section provides a dial tone filter for dial-tone rejection and separates the dual-tone signal into low-group and high-group tones. The decoder decodes all 16 DTMF tone pairs into a four bit code. The steering logic circuits allow the designer to tailor system parameters such as talk-off and noise immunity. The UM92870 is packaged in 3 standard 18-pin DIP configurations and requires only a few external passive components.

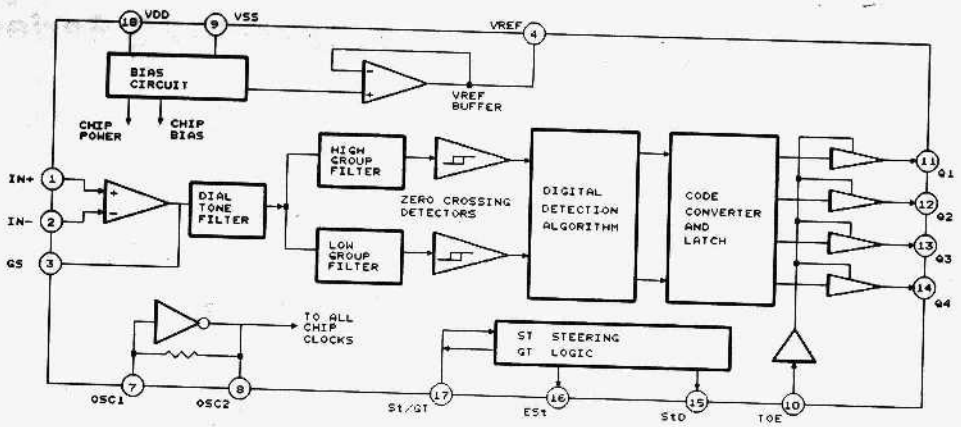
Pin Configurations







Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	IN+	I	Non-inverting input of op-amp.
2	IN-	I	Inverting input of op-amp.
3	GS	I	Gain select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	VREF	O	Reference Voltage output. May be used to bias the inputs at midrail, V_{DD} / 2.
5,6	INH , B/ H , PDI	I,I,I	INH: DTMF signal control,When this pin is pulled high, detection of tone pairs containing the 1633Hz component is inhibited. To detect all 16 standard digits this pin must be pulled low. B/ $\overline{H}$: Digital output format control. When this pin is pulled low, the UM92870 output is given in hexadecimal code. When input is high, output is in 2-of-8 binary code. Output codes are shown in Table 1. PDI: power down input. To enter power down mode, this pin must be pulled high.

UM92870A	Pin No. 5,6	INH , B/ $\overline{H}$
UM92870B	Pin No. 5,6	B/ $\overline{H}$, PDI
UM92870C	Pin No. 5,6	INH, PDI

Pin Description (Continued)

Pin No.	Symbol	I/O	Description
7	OSCI	I	Clock input.
8	OSC2	I	Clock output. A 3.5795 MHz crystal connected betwwen OSC1 and OSC2 completes the oscillator circuit.
9	Vss	I	Negative power supply input.
10	TOE	I	Three-state output enable. Logic high enables the output from Q1 through Q4.
11 - 14	Q1 - Q4	O	Three-state output. When enabled by TOE, provides the code which corresponds to the last valid tone-pair received. See Table 1.
15	StD	O	Delayed steering output. Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/Gt falls below VTST.
16	ESt	O	Early steering output. Presents a logic high once the digital algorithm has detected a valid tone pair. Any subsequent loss of signal condition will cause ESt to return to a logic low.
17	St/GT	I/O	Steering input/guard time output (bi-directional). A voltage greater than VTST detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than VTST output acts to reset the external steering time constant; its state is a function of ESt and the voltage on St.

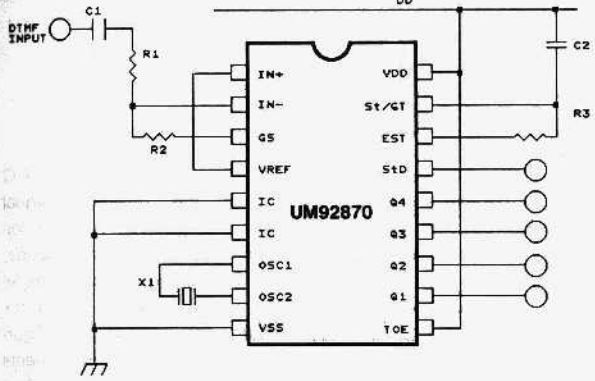
Digit	TOE	Hexadecimal				Binary Coded 2 of 8				Low Group Frequency (Hz)	High Group Frequency (Hz)
		Q4	Q3	Q2	Q1	Q4	Q3	Q2	Q1		
1	H	0	0	0	1	0	0	0	0	697	1209
2	H	0	0	1	0	0	0	0	1	697	1336
3	H	0	0	1	1	0	0	1	0	697	1477
4	H	0	1	0	0	0	1	0	0	770	1209
5	H	0	1	0	1	0	1	0	1	770	1336
6	H	0	1	1	0	0	1	1	0	770	1477
7	H	0	1	1	1	1	0	0	0	852	1209
8	H	1	0	0	0	1	0	0	1	852	1336
9	H	1	0	0	1	1	0	1	0	852	1477
0	H	1	0	1	0	1	1	0	1	941	1336
*	H	1	0	1	1	1	1	0	0	941	1209
#	H	1	1	0	0	1	1	1	0	941	1477
A	H	1	1	0	1	0	0	1	1	697	1633
B	H	1	1	1	0	0	1	1	1	770	1633
C	H	1	1	1	1	1	0	1	1	852	1633
D	H	0	0	0	0	1	1	1	1	941	1633
ANY	L	Z	Z	Z	Z	Z	Z	Z	Z	-	-

Function Description

The UM92870 monolithic DTMF receiver offers small size, low power consumption and high performance. Its general operation is described as follows:

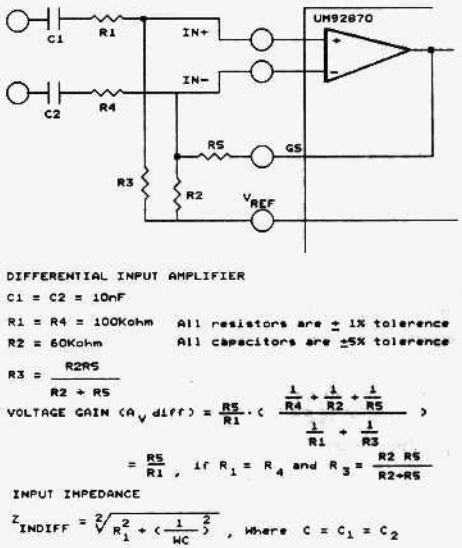
Differential Input Amplifier

To aid design flexibility, the UM92870 provides a differential input operational amplifier as well as a bias source (VREF) which is used to bias the input at midrail. Adjustment of gain is achieved by connecting a feedback resistor to the op-amp output (GS). Fiqure 1 shows the differential configuration with the op-amp connected for unity gain and VREF biasing the input at VDD/2. Figure 2 shows the differential configuration, which permits the adjustment of gain with the feedback resistor, R5.



Notes:
R1,R2 = 100kohm 1%
R3 = 300kohm 1%
C1,C2 = 100 nF 5%
X1 = 3.579545 MHz

Figure 1. Single Ended Input Configuration



DIFFERENTIAL INPUT AMPLIFIER

C1 = C2 = 10nF

R1 = R4 = 100Kohm All resistors are ± 1% tolerence

R2 = 60Kohm All capacitors are ±5% tolerence

$$R3 = \frac{R2R5}{R2 + R5}$$

$$\text{VOLTAGE GAIN } (A_V \text{ diff}) = \frac{R5}{R1} \cdot \left(\frac{\frac{1}{R4} + \frac{1}{R2} + \frac{1}{R5}}{\frac{1}{R1} + \frac{1}{R3}} \right)$$

$$= \frac{R5}{R1}, \text{ if } R_1 = R_4 \text{ and } R_3 = \frac{R2\,R5}{R2+R5}$$

INPUT IMPEDANCE

$$Z_{INDIFF} = 2\sqrt{R_1^2 + \left(\frac{1}{WC}\right)^2}, \text{ Where } C = C_1 = C_2$$

Figure 2. Differential Input Configuration

Filter Section

The differential input stage is followed by a low pass continuous RC active filter which performs an anti- frequency components by two sixth order switched capacitor bandpass filters. Each component tone is then