

**INTEGRATED CIRCUITS**

# DATA SHEET

## UMA1015AM

Low-power dual frequency  
synthesizer for radio  
communications

Product specification

1997 Sep 03

Supersedes data of 1997 Jun 10

File under Integrated Circuits, IC17

## Low-power dual frequency synthesizer for radio communications

## UMA1015AM

### FEATURES

- Two fully programmable RF dividers up to 1.1 GHz
- Fully programmable reference divider up to 35 MHz
- 2 : 1 or 1 : 1 ratio of selectable reference frequencies
- Fast three-line serial bus interface
- Adjustable phase comparator gain
- Programmable out-of-lock indication for both loops
- On-chip voltage doubler
- Low current consumption from 3 V supply
- Separate power-down mode for each synthesizer
- Up to 4 open-drain output ports
- Crystal input frequency signal inverted and buffered output on separate pin.

### APPLICATIONS

- Cordless telephone
- Hand-held mobile radio.

### GENERAL DESCRIPTION

The UMA1015AM is a low-power dual frequency synthesizer for radio communications which operates in the 50 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz.

The device is programmed via a 3-wire serial bus which operates up to 10 MHz. The charge pump currents (gains) are fixed by an external resistance at pin 20 ( $I_{SET}$ ).

The BiCMOS device is designed to operate from 2.7 V (3 NiCd cells) to 5.5 V at low current. Digital supplies  $V_{DD1}$  and  $V_{DD2}$  must be at the same potential. The charge pump supply ( $V_{CC}$ ) can be provided by an external source or on-chip voltage doubler.  $V_{CC}$  must be equal to or higher than  $V_{DD1}$ .

Each synthesizer can be powered-down independently via the serial bus to save current. It is also possible to power-down the device via the HPD input (pin 5).

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DD1}, V_{DD2}$	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
$V_{CC}$	charge pump supply voltage	external supply; doubler disabled; $V_{CC} \geq V_{DD}$	2.7	–	6.0	V
$V_{CCvd}$	charge pump supply from voltage doubler	doubler enabled	–	$2V_{DD1} - 0.6$	6.0	V
$I_{DD1} + I_{DD2} + I_{CC}$	operating supply current	both synthesizers ON; doubler disabled; $V_{DD1} = V_{DD2} = 3$ V	–	8.7	–	mA
$I_{DDpd} + I_{CCpd}$	total current in power-down mode	doubler disabled; $V_{DD1} = V_{DD2} = 3$ V	–	3	–	$\mu$ A
$I_{DDpd}$	current in power-down mode from supply $V_{DD1}$ and $V_{DD2}$	doubler enabled; $V_{DD1} = V_{DD2} = 3$ V	–	0.25	–	mA
$f_{RF}$	RF input frequency for each synthesizer		50	–	1100	MHz
$f_{XTALIN}$	crystal input frequency		3	–	35	MHz
$f_{pc(min)}$	minimum phase comparator frequency		–	10	–	kHz
$f_{pc(max)}$	maximum phase comparator frequency		–	750	–	kHz
$T_{amb}$	operating ambient temperature		–30	–	+85	$^{\circ}$ C

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1015AM	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

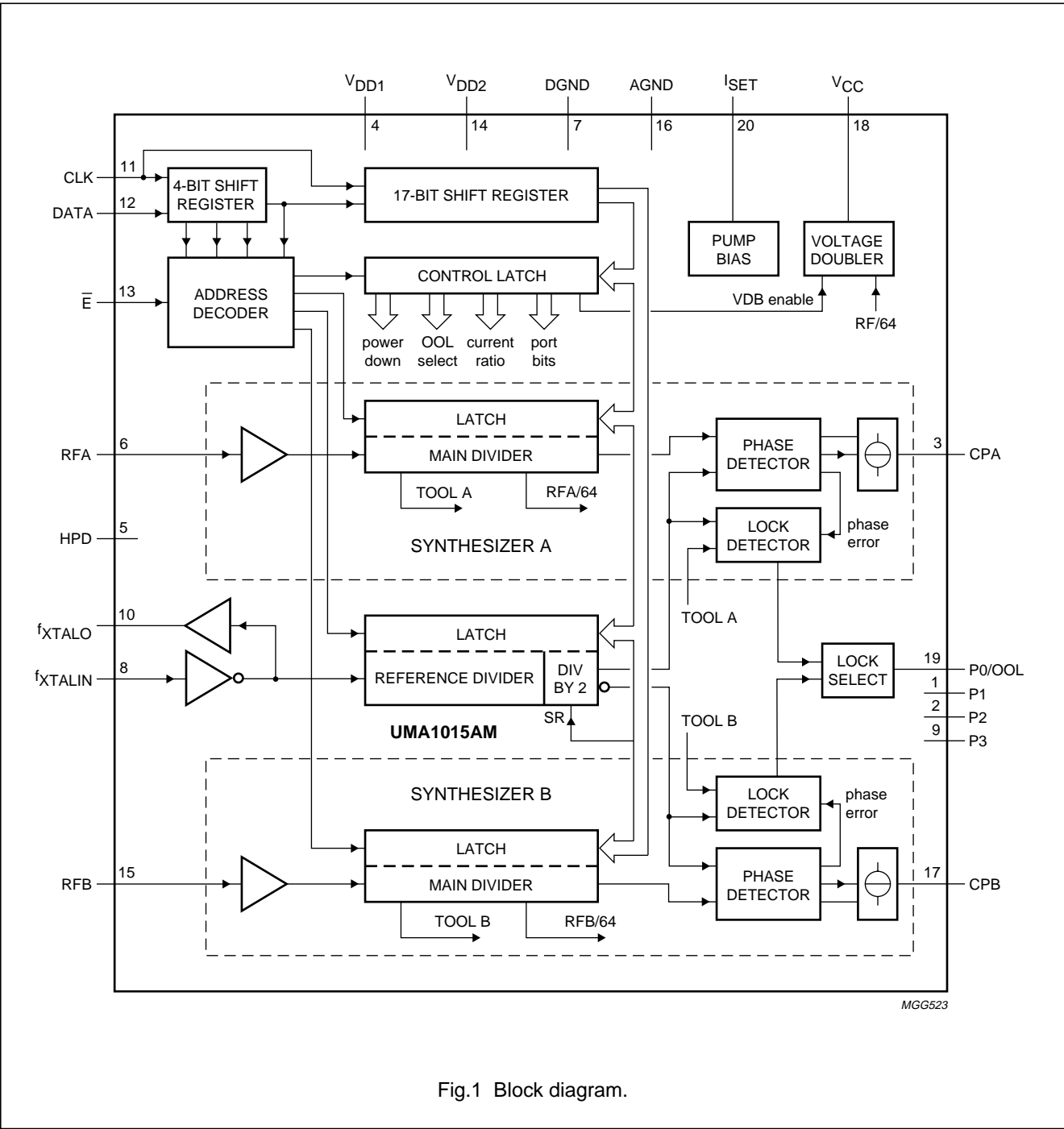


Fig.1 Block diagram.

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### PINNING

SYMBOL	PIN	DESCRIPTION
P1	1	output Port 1
P2	2	output Port 2
CPA	3	charge pump output synthesizer A
V <sub>DD1</sub>	4	digital supply voltage 1
HPD	5	hardware power-down (input LOW = power-down)
RFA	6	RF input synthesizer A
DGND	7	digital ground
f <sub>XTALIN</sub>	8	common crystal frequency input from TCXO
P3	9	output Port 3
f <sub>XTALO</sub>	10	open-drain output of f <sub>XTAL</sub> signal
CLK	11	programming bus clock input
DATA	12	programming bus data input
$\bar{E}$	13	programming bus enable input (active LOW)
V <sub>DD2</sub>	14	digital supply voltage 2
RFB	15	RF input synthesizer B
AGND	16	analog ground to charge pumps
CPB	17	charge pump output synthesizer B
V <sub>CC</sub>	18	analog supply to charge pump; external or voltage doubler output
P0/OOL	19	Port output 0/out-of-lock output
I <sub>SET</sub>	20	regulator pin to set charge pump currents

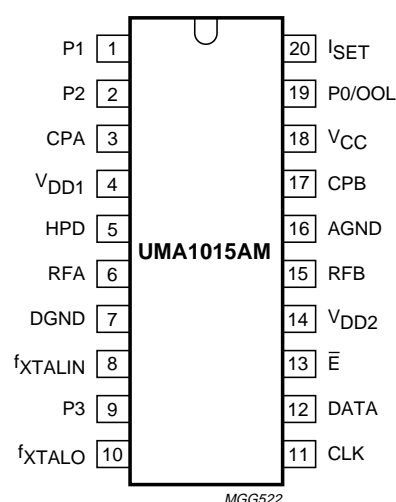


Fig.2 Pin configuration.

### FUNCTIONAL DESCRIPTION

#### Main dividers

Each synthesizer has a fully programmable 17-bit main divider. The RF input drives a pre-amplifier to provide the clock to the first divider bit. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from below 50 mV (RMS) up to 250 mV (RMS), and at frequencies up to 1.1 GHz. The high frequency sections of the divider are implemented using bipolar transistors, while the slower section uses CMOS technology. The range of division ratios is 512 to 131071.

#### Reference divider

There is a common fully programmable 12-bit reference divider for the two synthesizers. The input f<sub>XTALIN</sub> drives a pre-amplifier to provide the clock input for the reference

divider. This clock signal is also inverted and output on pin f<sub>XTALO</sub> (open drain). A crystal connected between f<sub>XTALIN</sub> and f<sub>XTALO</sub> with suitable feedback components can be used to make an oscillator. An extra divide-by-2 block allows a reference comparison frequency for synthesizer B to be half the frequency of synthesizer A. This feature is selectable using the program bit SR. If the programmed reference divider ratio is R then the ratio for each synthesizer is as given in Table 1.

The range for the division ratio R is 8 to 4095. Opposite edges of the divider output are used to drive the phase detectors to ensure that active edges arrive at the phase detectors of each synthesizer at different times. This minimizes the potential for interference between the charge pumps of each loop. The reference divider consists of CMOS devices operating beyond 35 MHz.

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**Table 1** Synthesizer ratio of reference divider

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

### Phase comparators

For each synthesizer, the outputs of the main and reference dividers drive a phase comparator where a charge pump produces phase error current pulses for integration in an external loop filter. The charge pump current is set by an external resistance  $R_{SET}$  at pin  $I_{SET}$ , where a temperature-independent voltage of 1.1 V is generated.  $R_{SET}$  should be between 12 and 60 k $\Omega$ . The charge pump current,  $I_{CP}$ , can be programmed to be either  $(12 \times I_{SET})$  or  $(24 \times I_{SET})$  with a maximum of 2.3 mA. The dead zone, caused by finite switching of current pulses, is cancelled by an internal delay in the phase detector thus giving improved linearity. The charge pump has a separate supply,  $V_{CC}$ , which helps to reduce the interference on the charge pump output from other parts of the circuit.  $V_{CC}$  can be higher than  $V_{DD1}$  if a wider range on the VCO input is required.  $V_{CC}$  must not be less than  $V_{DD1}$ .

### Voltage doubler

If required, there is a voltage doubler on-chip to supply the charge pumps at a higher level than the nominal available supply. The doubler operates from the digital supply  $V_{DD1}$ , and is internally limited to a maximum output of 6 V. An external capacitor is required on pin  $V_{CC}$  for smoothing, the capacitor required to develop the extra voltage is integrated on-chip. To minimize the noise being introduced to the charge pump output from the voltage doubler, the doubler clock is suppressed (provided both loops are in-lock) for the short time that the charge pumps are active. The doubler clock (RF/64) is derived from whichever main divider is operating (synthesizer A has priority). While both synthesizers are powered down (and the doubler is enabled), the doubler clock is supplied by a low-current internal oscillator. The doubler can be disabled by programming the bit  $VDON$  to logic 0, in order to allow an external charge pump supply to be used.

### Out-of-lock indication/output ports

There is a common lock detector on-chip for the synthesizers. The lock condition of each, or both loops, is output via an open-drain transistor which drives pin P0/OOL (when out-of-lock, the transistor is turned on and therefore the output is forced LOW). The lock condition output is software selectable (see Table 4).

An out-of-lock condition is flagged when the phase error is greater than  $T_{OOL}$ , which is approximately 30 ns. The out-of-lock flag is only released after the first reference cycle where the phase error is less than  $T_{OOL}$ . The out-of-lock function can be disabled, via the serial bus, and the pin P0/OOL can be used as a port output. Three other port outputs P1, P2 and P3 (open-drain transistors) are also available.

### Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, CLK and  $\bar{E}$  (enable). The data sent to the device is loaded in bursts framed by  $\bar{E}$ . Programming clock edges are ignored until  $\bar{E}$  goes active LOW. The programmed information is loaded into the addressed latch when  $\bar{E}$  returns inactive (HIGH). This is allowed when CLK is in either state without causing any consequences to the register data. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down of both synthesizers.

However when either synthesizer A or synthesizer B or both are powered-on, the presence of a TCXO signal is required at pin 8 ( $f_{XTALIN}$ ) for correct programming.

### Data format

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are an address field. The address bits are decoded on the rising edge of  $\bar{E}$ . This produces an internal load pulse to store the data in the addressed latch. To ensure that data is correctly loaded on first power-up,  $\bar{E}$  should be held LOW and only taken HIGH after having programmed an appropriate register. To avoid erroneous divider ratios, the pulse is inhibited during the period when data is read by the frequency dividers. This condition is guaranteed by respecting a minimum  $\bar{E}$  pulse width after data transfer. The data format and register bit allocations are shown in Table 2.

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**Table 2** Bit allocation

FIRST		REGISTER BIT ALLOCATION																				LAST			
p1	p2	p3	p4	p5	p6	p7	p8	p9	p10	p11	p12	p13	p14	p15	p16	p17	p18	p19	p20	p21					
dt16	dt15	dt14	dt13	dt12	DATA FIELD							dt4	dt3	dt2	dt1	dt0	ADDRESS								
X	X	VDON	PO	OLA	OLB	CRA	CRB	X	X	sPDA	sPDB	P3	P2	P1	X	X	0	0	0	1					
MA16	SYNTHESIZER A MAIN DIVIDER COEFFICIENT																				MA0	0	1	0	0
0	0	0	0	SR	R11	REFERENCE DIVIDER COEFFICIENT										R0	0	1	0	1					
MB16	SYNTHESIZER B MAIN DIVIDER COEFFICIENT																				MB0	0	1	1	0
RESERVED FOR TEST <sup>(1)</sup>																									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	sPBF	0	0	1	0	0	0				

**Note**

1. The test register should not be programmed with any other values except all zeros for normal operation.

**Table 3** Bit allocation description

SYMBOL	DESCRIPTION
sPDA, sPDB	software power-down for synthesizers A and B (0 = power-down)
sPBF	software power-on for $f_{xtal}$ buffer (1 = buffer on)
P3, P2, P1 and P0	bits output to pins 1, 2, 9 and 19 (1 = high impedance)
VDON	voltage doubler enable (1 = doubler enabled)
OLA, OLB	out-of-lock select; selects signal output to pin 19 (see Table 4)
CRA, CRB	charge pump A/B current to $I_{SET}$ ratio select (see Table 5)
SR	reference frequency ratio select (see Table 6)

**Table 4** Out-of-lock select

OLA	OLB	OUTPUT AT PIN 19
0	0	P0
0	1	lock status of loop B; OOLB
1	0	lock status of loop A; OOLA
1	1	logic OR function of loops A and B

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**Table 5** Charge pump current ratio

CRA/CRB	CURRENT AT PUMP
0	$I_{CP} = 12 \times I_{SET}$
1	$I_{CP} = 24 \times I_{SET}$

**Table 6** Reference division ratio

SR	SYNTHESIZER A	SYNTHESIZER B
0	R	R
1	R	2R

### Power-down modes

The device can be powered down either via pin HPD (active LOW = power-down) or via the serial bus (bits sPDA and sPDB, logic 0 = power-down).

The synthesizers are powered up when both hardware and software Power-down signals are at logic 1. When only one synthesizer is powered down, the functions common to both will be maintained (independent of the state of sPBF). When both synthesizers are powered down, the  $f_{xtal}$  buffer can be maintained in an active state by setting sPBF to logic 1. This will allow any system clock derived from the  $f_{XTALO}$  buffered output to remain on in power-down. Note that sPBF is independent of the state of HPD. When both synthesizers are switched off, the voltage doubler (if enabled) will remain active drawing a reduced current. An internal oscillator will drive the doubler in this situation. If both synthesizers have been in a power-down condition, then when one or both synthesizers are reactivated, the reference and main dividers restart in such a way as to avoid large random phase errors at the phase comparator.

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD1}, V_{DD2}$	DC range of digital power supply voltage with respect to DGND	−0.3	+6.0	V
$V_{CC}$	DC charge pump supply voltage with respect to AGND	−0.3	+6.0	V
$\Delta V_{CC-DD}$	difference in voltage between $V_{CC}$ and $V_{DD1}, V_{DD2}$	−0.3	+6.0	V
$V_n$	DC voltage at pins 1, 2, 5, 6, 8 to 15, 19 and 20 with respect to DGND	−0.3	$V_{DD1} + 0.3$	V
$V_{3, 17}$	DC voltage at pins 3 and 17 with respect to AGND	−0.3	$V_{CC} + 0.3$	V
$\Delta V_{GND}$	difference in voltage between AGND and DGND (these pins should be connected together)	−0.3	+0.3	V
$T_{stg}$	storage temperature	−55	+125	°C
$T_{amb}$	operating ambient temperature	−30	+85	°C

### HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

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## CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.7$  to  $5.5$  V;  $V_{CC} = 2.7$  to  $6.0$  V;  $T_{amb} = 25$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies; (<math>V_{DD1}</math>, <math>V_{DD2}</math> and <math>V_{CC}</math>) voltage doubler disabled, external supply on <math>V_{CC}</math></b>						
$V_{DD1}$ , $V_{DD2}$	digital supply voltage	$V_{DD1} = V_{DD2}$	2.7	–	5.5	V
$I_{DD1} + I_{DD2}$	total digital supply current from $V_{DD1}$ and $V_{DD2}$	$f_{XTAL} = 12.8$ MHz; both synthesizers on; $V_{DD1} = V_{DD2} = 3$ V	–	8.7	–	mA
		$f_{XTAL} = 12.8$ MHz; both synthesizers on; $V_{DD1} = V_{DD2} = 5.5$ V	–	–	12.5	mA
$I_{DDpda}$ , $I_{DDpdb}$	total digital supply current from $V_{DD1}$ and $V_{DD2}$ with one synthesizer in power-down mode	$f_{XTAL} = 12.8$ MHz; one synthesizer powered down; $V_{DD1} = V_{DD2} = 3$ V	–	5.0	–	mA
		$f_{XTAL} = 12.8$ MHz; one synthesizer powered down; $V_{DD1} = V_{DD2} = 5.5$ V	–	–	7.5	mA
$I_{DD(xtal)}$	digital supply current from $V_{DD1}$ with both synthesizers powered down and crystal buffer on	$f_{XTAL} = 12.8$ MHz; $V_{HPD} = 0$ V; sPBF = 1; $V_{DD1} = V_{DD2} = 3$ V	–	0.5	–	mA
		$f_{XTAL} = 12.8$ MHz; $V_{HPD} = 0$ V; sPBF = 1; $V_{DD1} = V_{DD2} = 5.5$ V	–	–	1.15	mA
$I_{DDpd}$	digital supply current in power-down mode	both synthesizers powered down; $V_{HPD} = 0$ V; sPBF = 0	–	–	60	μA
$V_{CC}$	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	6.0	V
$I_{CC}$	charge pump supply current	both synthesizers on and in lock; $f_{ref} = 12.5$ kHz	–	–	25	μA
$I_{CCpd}$	charge pump supply current in power-down mode	both synthesizers powered down	–	–	25	μA
<b>Voltage doubler enabled</b>						
$I_{DD}$	total digital supply current from $V_{DD1}$ and $V_{DD2}$	$f_{XTAL} = 12.8$ MHz; both synthesizers on and in lock; $V_{DD1} = 3$ V; $f_{RF} = 900$ MHz	–	9.2	12	mA
$I_{DDpd}$	total digital supply current in power-down mode from $V_{DD1}$ and $V_{DD2}$	both synthesizers powered down; $V_{DD1} = 3$ V; $V_{HPD} = 0$ V; sPBF = 0	–	0.25	0.4	mA
$V_{CCvd}$	charge pump supply voltage	DC current drawn from $V_{CC} = 50$ μA; $f_{RF} > 100$ MHz	4.2	$2V_{DD1} - 0.6$	6.0	V



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>RF main divider input; RFA and RFB</b>						
$f_{RF}$	RF input frequency		50	–	1 100	MHz
$V_{RF(rms)}$	RF input signal voltage (RMS value; AC coupled)	$R_s = 50 \Omega$ ; $f_{RF} = 400$ to 1 100 MHz	50	–	250	mV
		$R_s = 50 \Omega$ ; $f_{RF} = 80$ to 400 MHz	150	–	400	mV
		$R_s = 50 \Omega$ ; $f_{RF} = 50$ to 80 MHz	225	–	400	mV
$Z_I$	input impedance (real part)	$f_{RF} = 1$ GHz; indicative, not tested	–	300	–	$\Omega$
$C_I$	input capacitance	indicative, not tested	–	1	–	pF
$R_{pm}$	principle main divider ratio		512	–	131 071	
<b>Reference divider input; <math>f_{XTALIN}</math></b>						
$f_{XTALIN}$	reference input frequency from crystal		3	–	35	MHz
$V_{XTALIN(rms)}$	sinusoidal input voltage (RMS value)		100	–	500	mV
$Z_I$	input impedance (real part)	$f_{XTALIN} = 12.8$ MHz; indicative, not tested	–	10	–	k $\Omega$
$C_I$	input capacitance	indicative, not tested	–	1	–	pF
$R_{rd}$	reference divider ratio		8	–	4095	
<b>Charge pump current setting resistor input; <math>I_{SET}</math></b>						
$V_{SET}$	voltage output on $I_{SET}$	$R_{SET} = 12$ to 60 k $\Omega$	–	1.1	–	V
<b>Charge pump outputs; CPA and CPB</b>						
$I_{cp}$	charge pump sink or source current	$R_{SET} = 15$ k $\Omega$ ; CRA/CRB = logic 1; $I_{cp} = I_{SET} \times 24$ ; $V_{cp} = 0.4$ V to $V_{CC} - 0.5$ V	1.3	1.75	2.3	mA
		$R_{SET} = 15$ k $\Omega$ ; CRA/CRB = logic 0; $I_{cp} = I_{SET} \times 12$ ; $V_{cp} = 0.4$ V to $V_{CC} - 0.5$ V	0.7	0.9	1.2	mA
$I_{LI}$	charge pump off leakage current	$V_{cp} = 0.4$ V to $V_{CC} - 0.5$ V	–5	$\pm 1$	+5	nA
<b>Logic input signal levels; DATA, CLK, <math>\bar{E}</math> and HPD</b>						
$V_{IH}$	HIGH level input voltage	at logic 1	$0.7V_{DD1}$	–	$V_{DD1} + 0.3$	V
$V_{IL}$	LOW level input voltage	at logic 0	–0.3	–	$0.3V_{DD1}$	V
$I_{bias}$	input bias currents	at logic 1 or logic 0	–5	–	+5	$\mu$ A
$C_I$	input capacitance	indicative, not tested	–	1	–	pF
<b>Port outputs/Out-of-lock; P0/OOL, P1, P2, P3 and <math>f_{XTALO}</math> - open drain outputs</b>						
$V_{OL}$	LOW level output voltage	$I_{sink} < 0.4$ mA	–	–	0.4	V

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SERIAL TIMING CHARACTERISTICS

$V_{DD1} = 3\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
$t_r, t_f$	input rise and fall times	–	10	40	ns
$T_{cy}$	clock period	100	–	–	ns
Enable programming; $\bar{E}$					
$t_{START}$	delay to rising clock edge	40	–	–	ns
$t_{END}$	delay from last falling clock edge	–20	–	–	ns
$t_W$	minimum inactive pulse width	4000	–	–	ns
$t_{SU;\bar{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

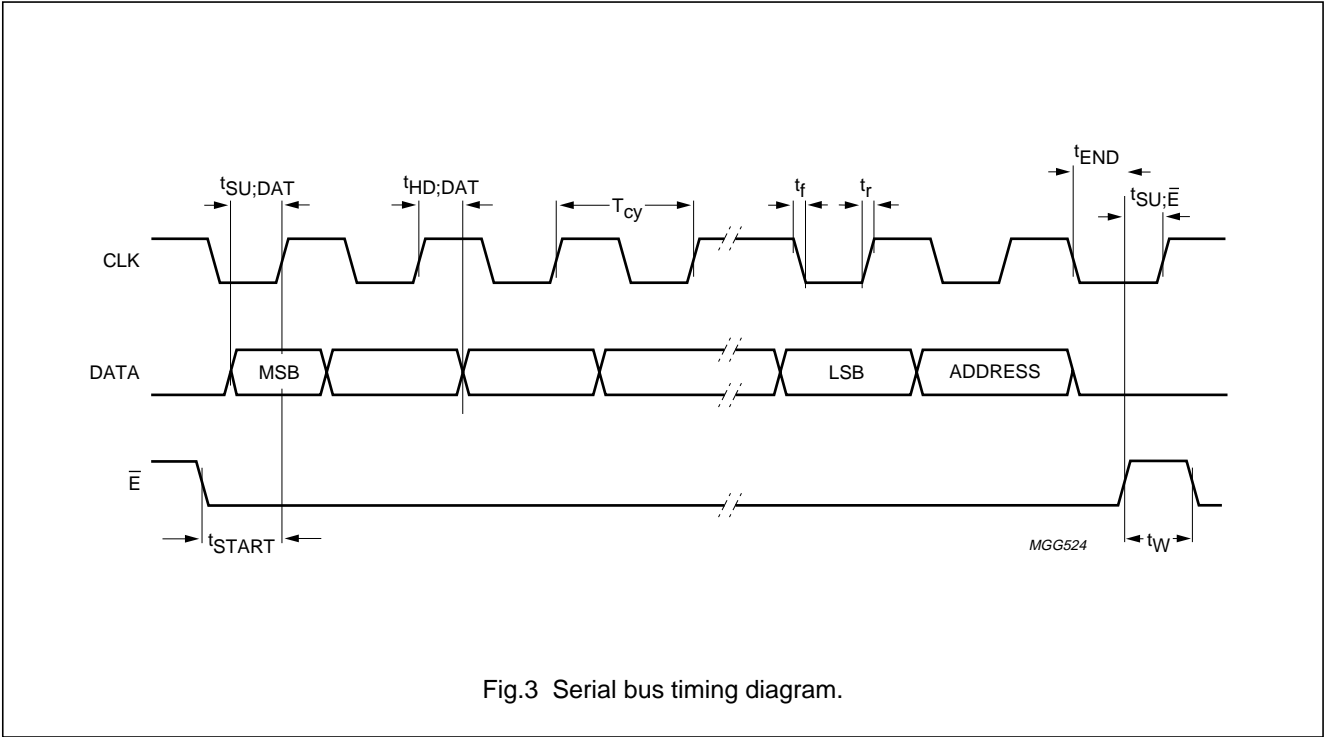
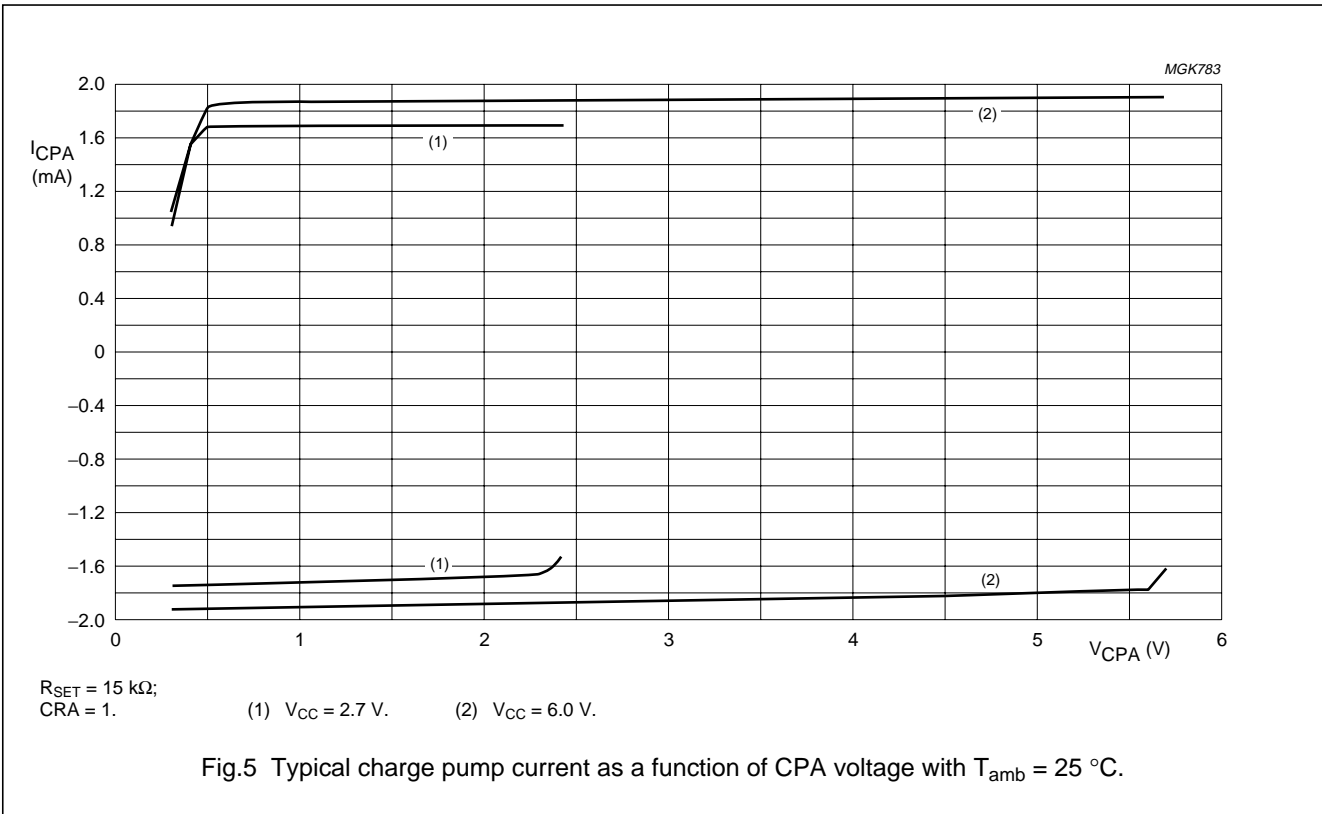
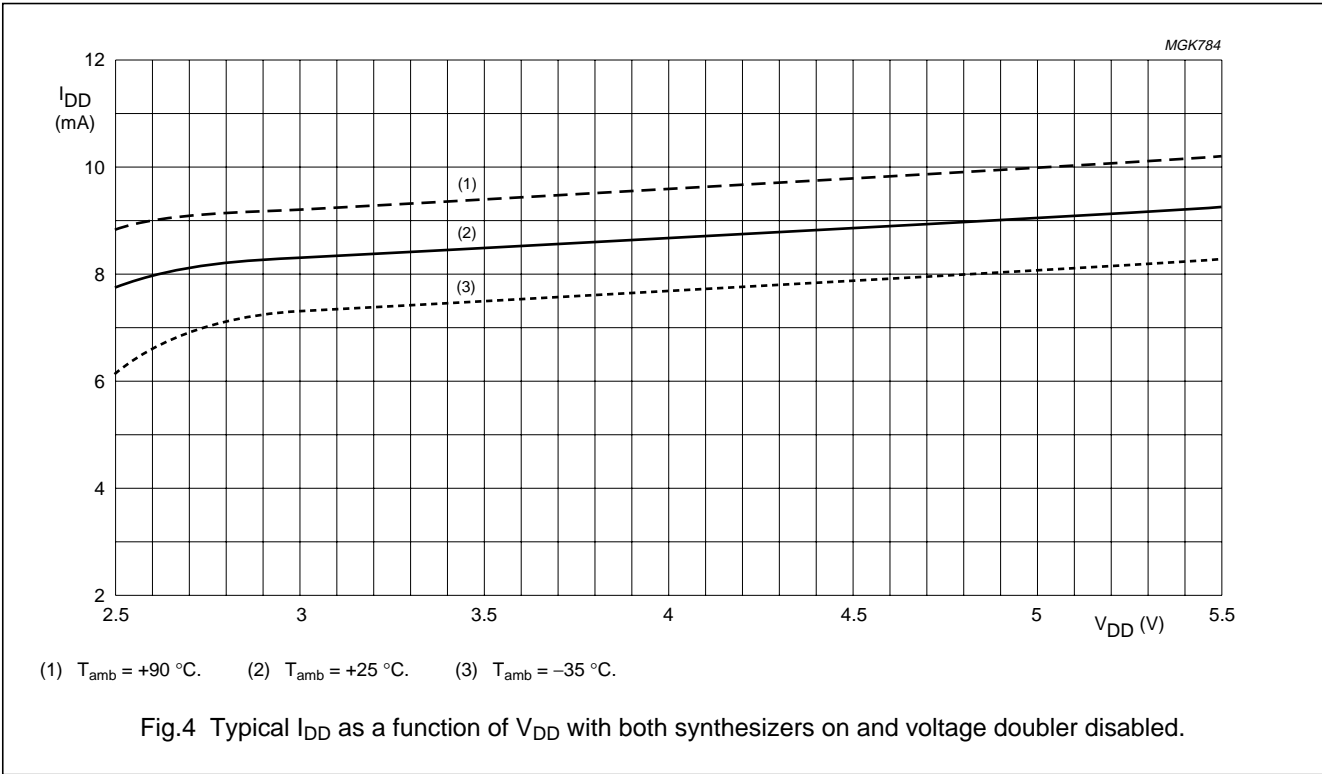


Fig.3 Serial bus timing diagram.

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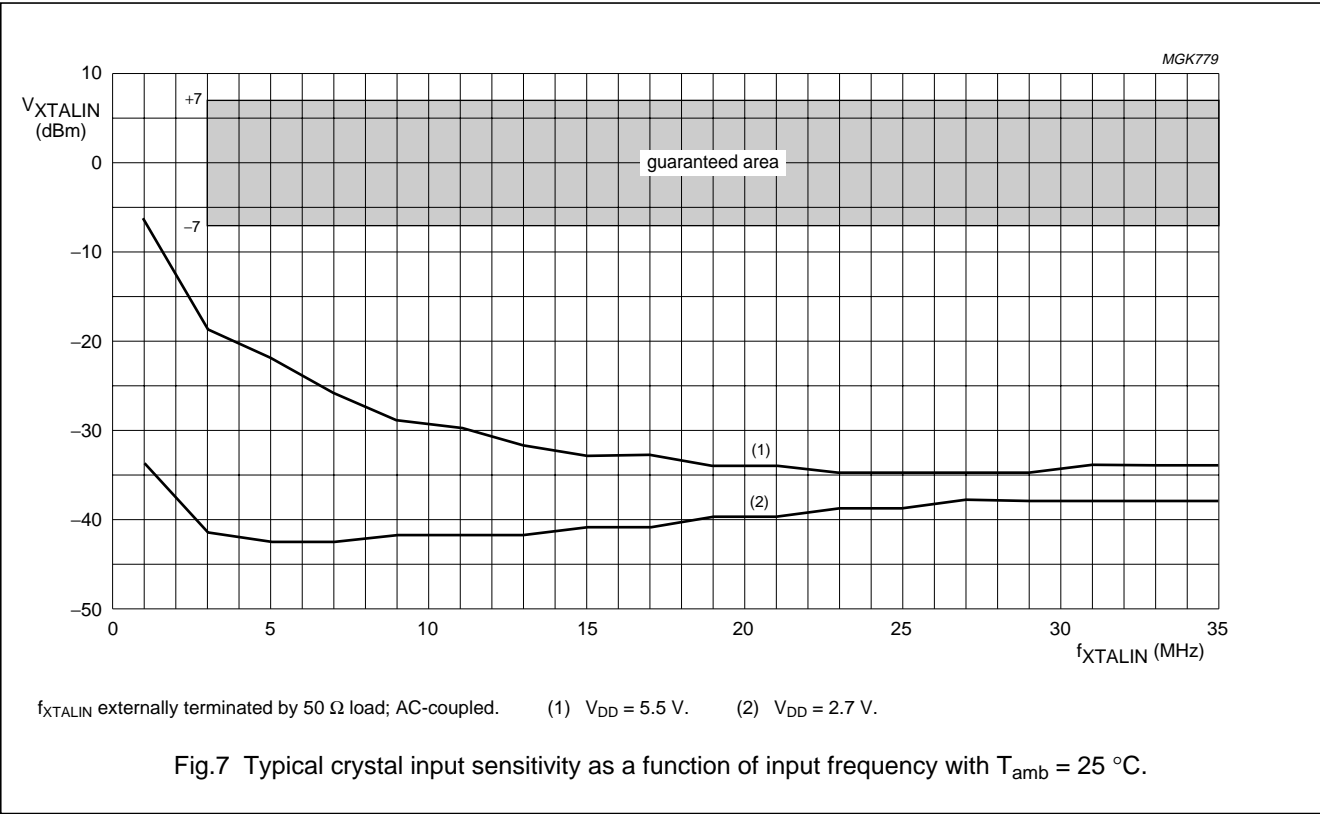
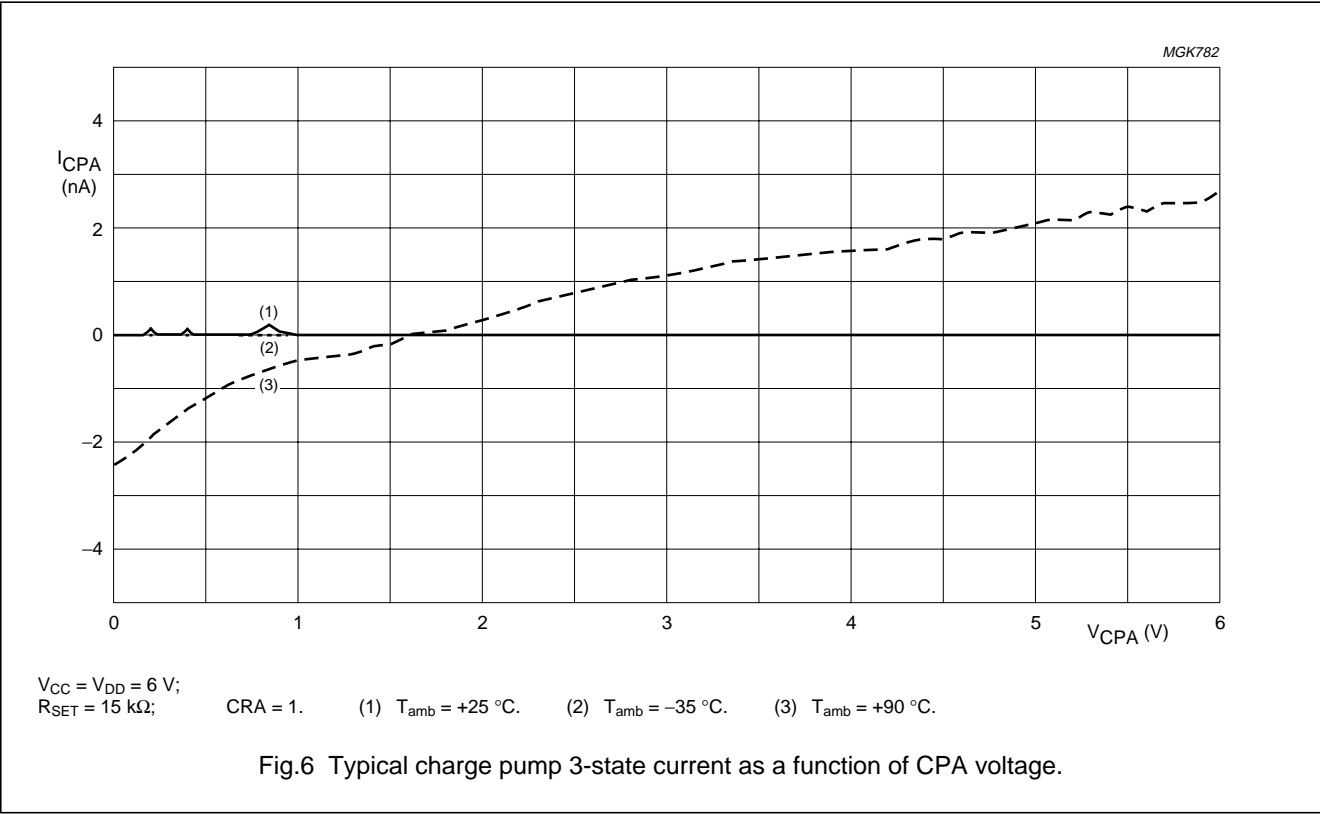
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TYPICAL PERFORMANCE CHARACTERISTICS



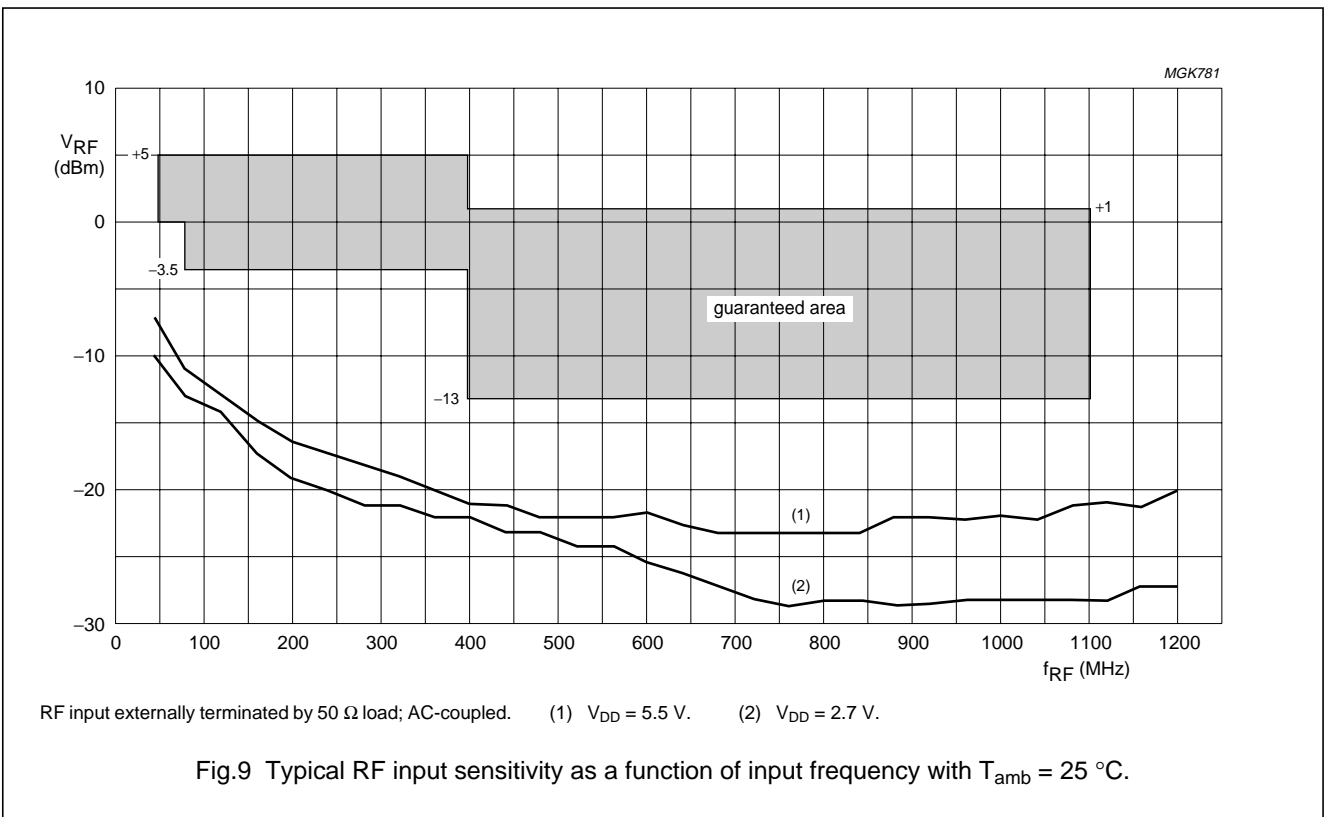
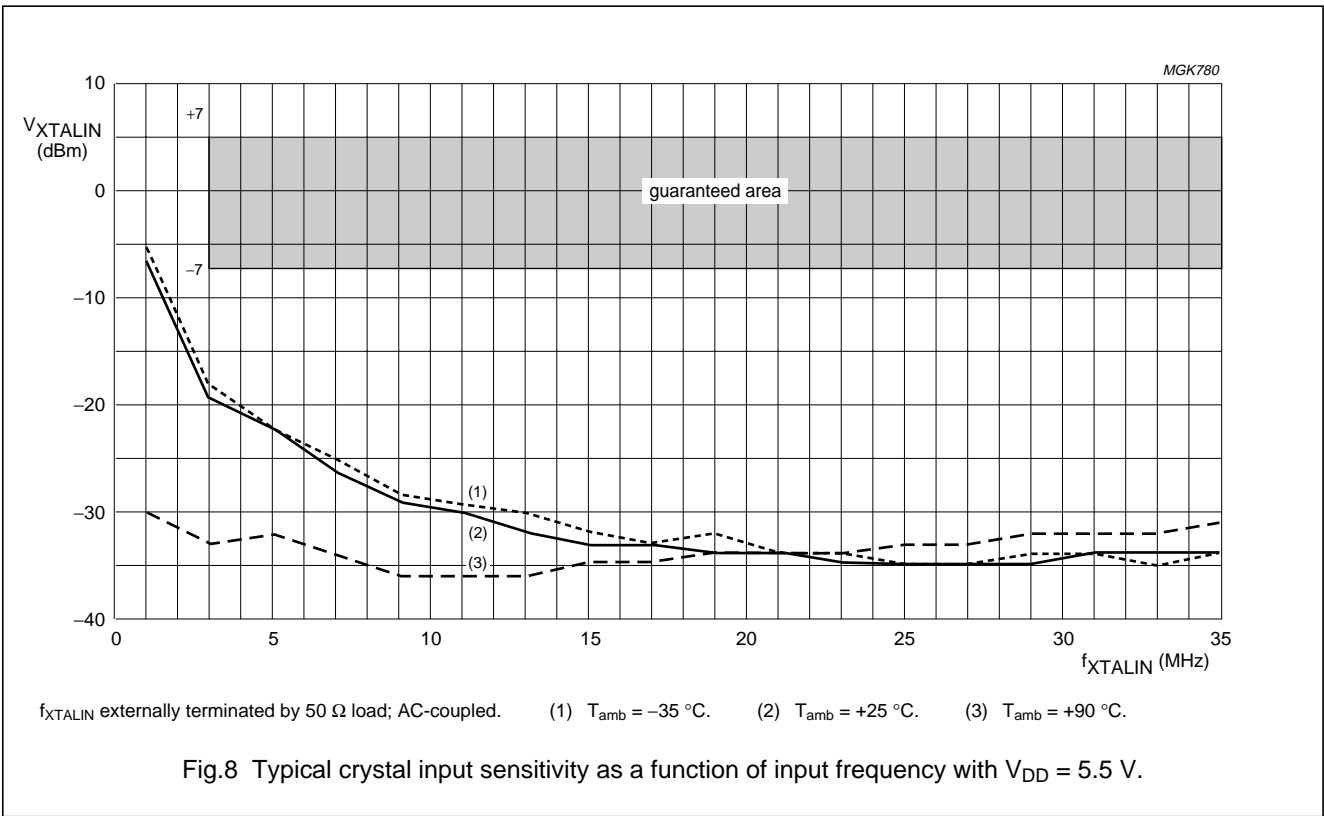
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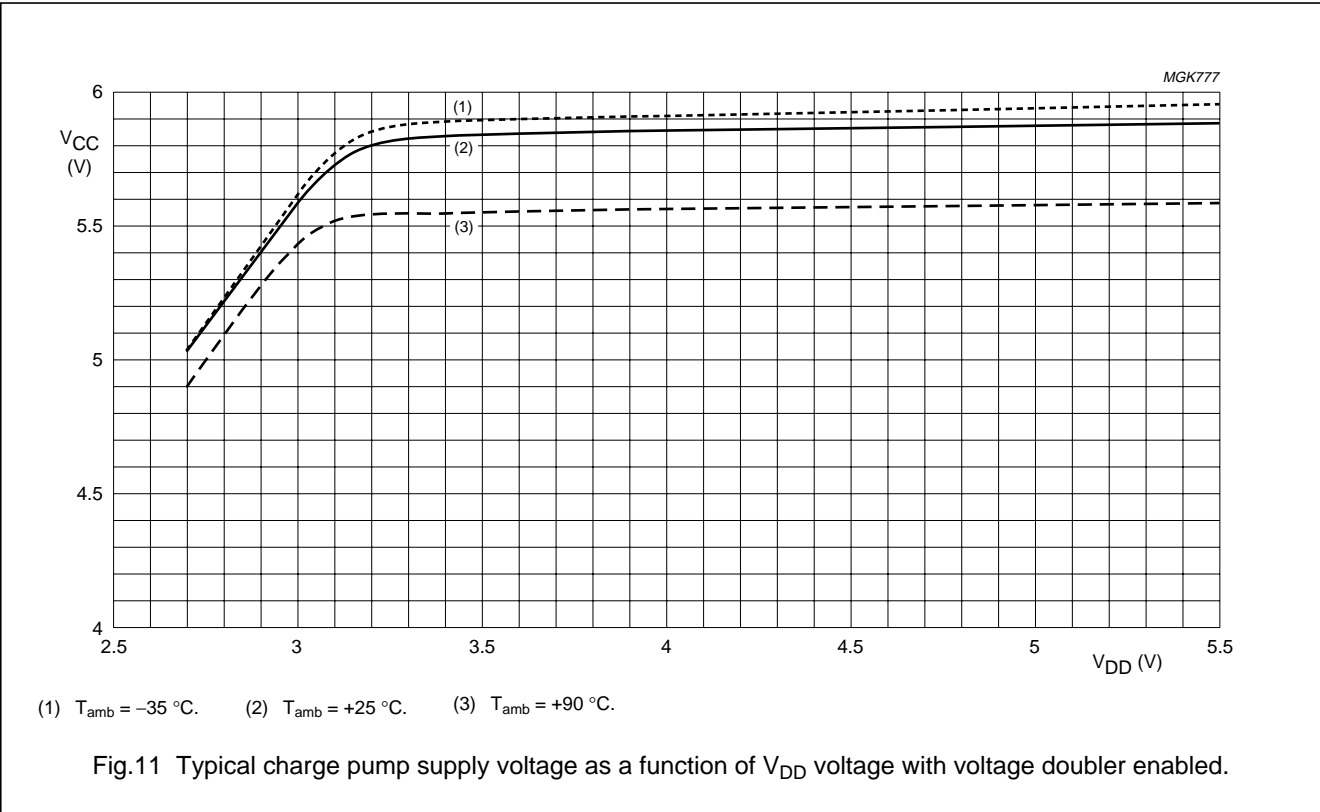
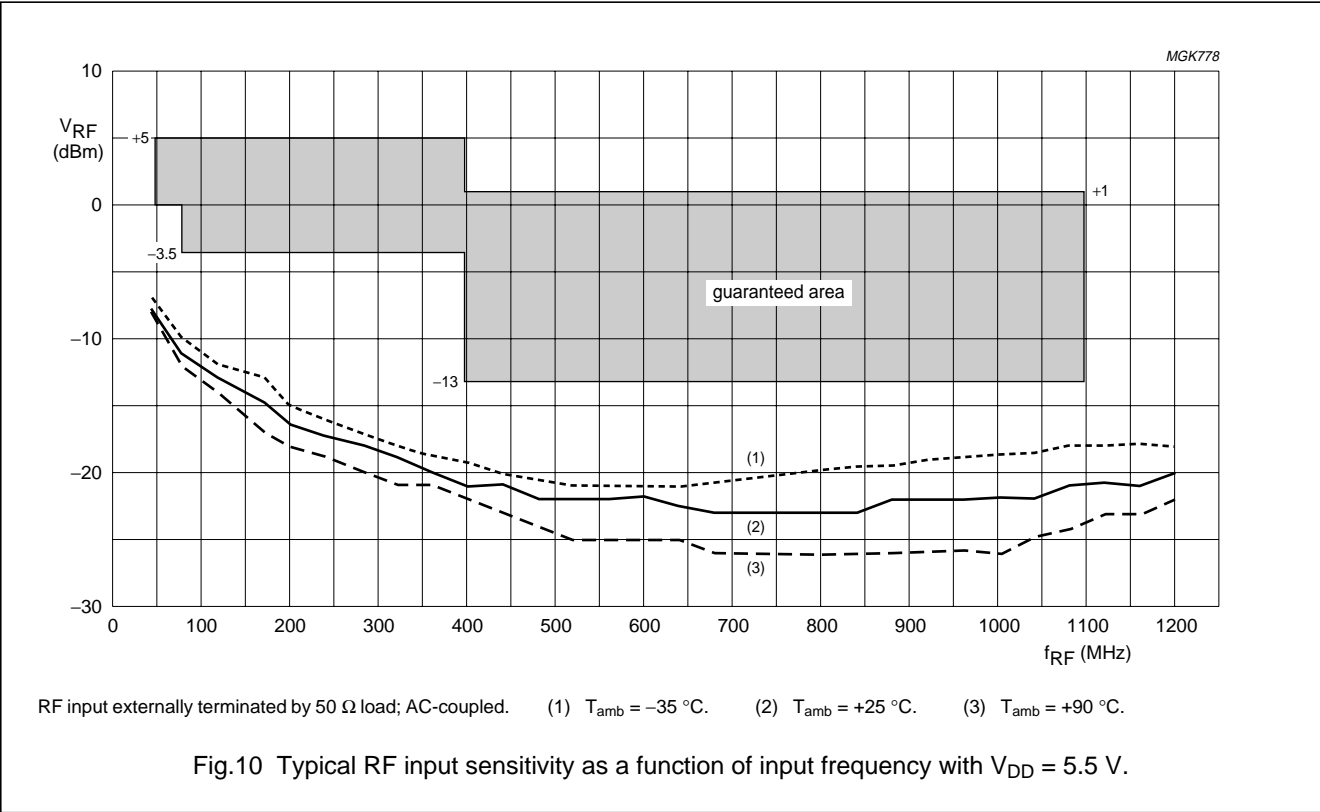
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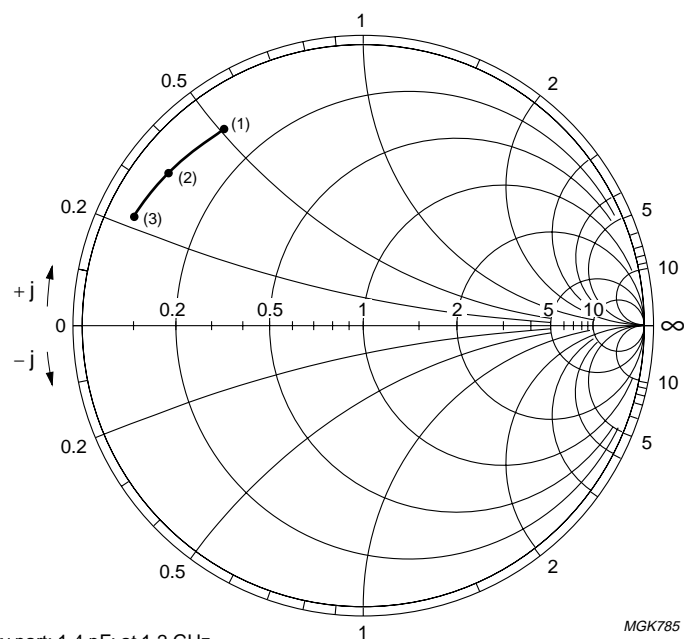
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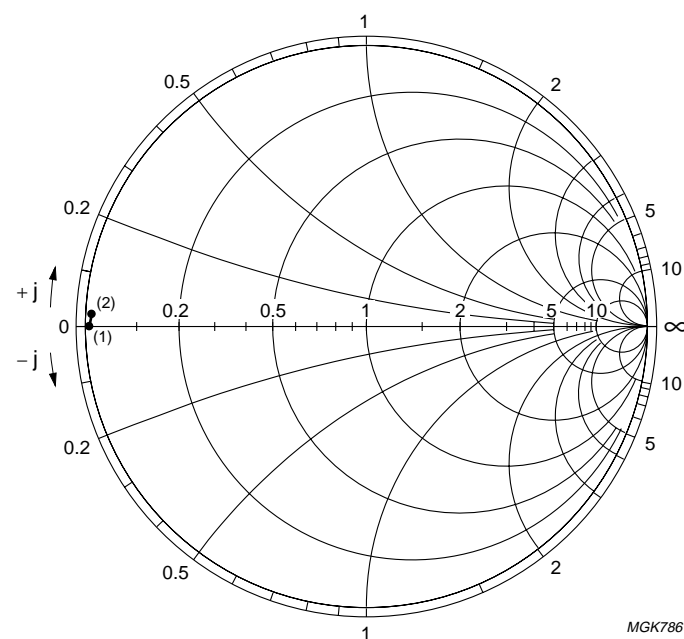
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- (1) Real part: 500  $\Omega$ ; imaginary part: 1.4 pF; at 1.2 GHz.  
 (2) Real part: 800  $\Omega$ ; imaginary part: 1.1 pF; at 1.0 GHz. (3) Real part: 830  $\Omega$ ; imaginary part: 0.9 pF; at 800 MHz.

Fig.12 Typical RF input admittance (IC powered on).



- (1) Real part: 7.8 k $\Omega$ ; imaginary part: 0.9 pF; at 3 MHz. (2) Real part: 9.8 k $\Omega$ ; imaginary part: 1.0 pF; at 35 MHz.

Fig.13 Typical crystal input admittance (IC powered on).

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## APPLICATION INFORMATION

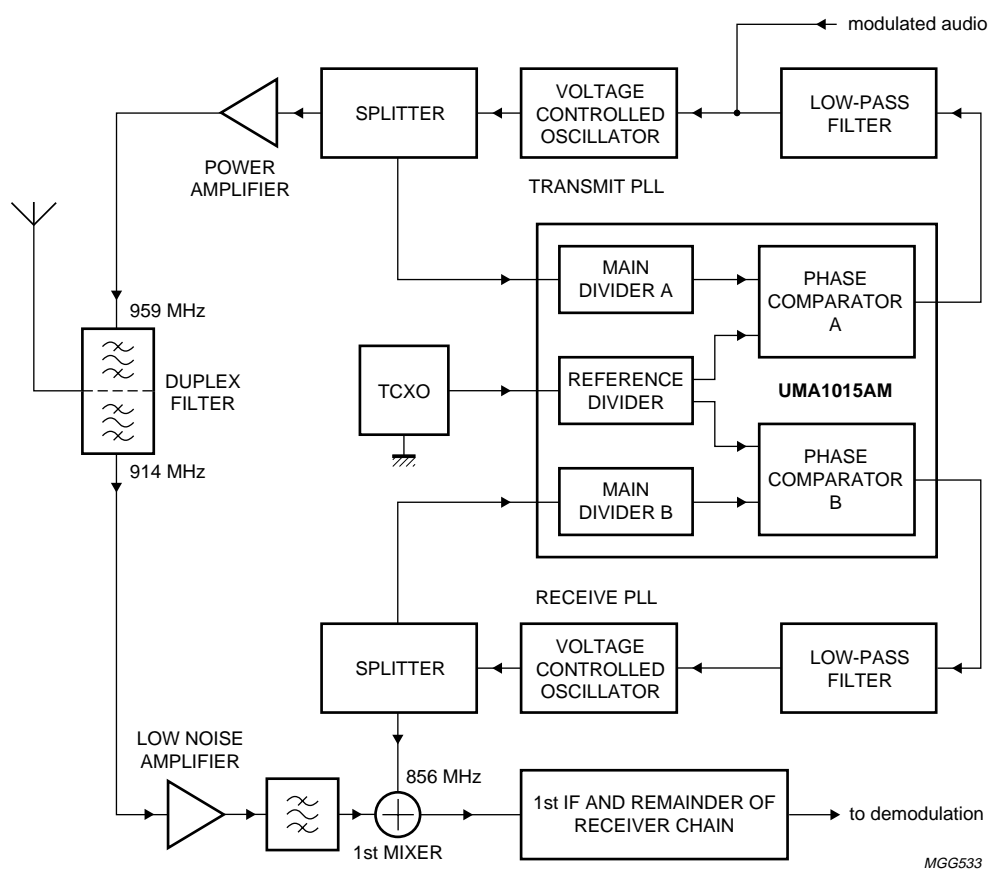


Fig.14 Typical application block diagram.



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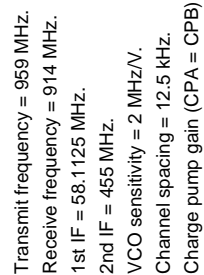


Fig.15 Typical CT1 application.

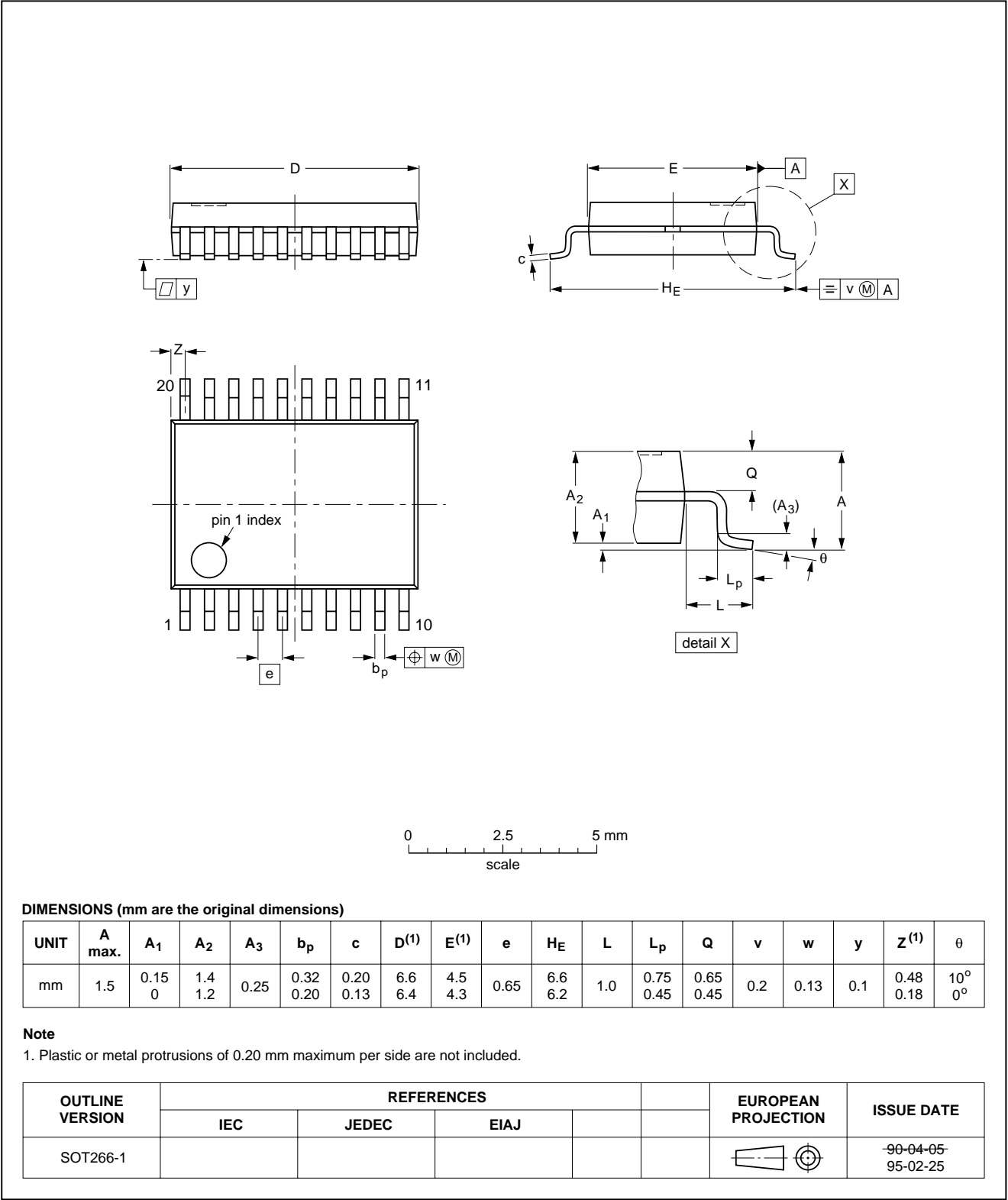
Low-power dual frequency synthesizer  
for radio communications

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PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1



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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.**

**Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

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**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

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**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
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**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615800, Fax. +358 9 61580920

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

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Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

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254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,  
Tel. +91 22 493 8541, Fax. +91 22 493 0966

**Indonesia:** see Singapore

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
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**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

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20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

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**Middle East:** see Italy

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**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

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2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51,  
04552-903 São Paulo, SÃO PAULO - SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 829 1849

**Spain:** Balmes 22, 08007 BARCELONA,  
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**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
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**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,  
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

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**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
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**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
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