NEC

COMPOUND FIELD EFFECT POWER TRANSISTOR

μPA1560

N-CHANNEL POWER MOS FET ARRAY
SWITCHING
INDUSTRIAL USE

DESCRIPTION

The μPA1560 is N-Channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

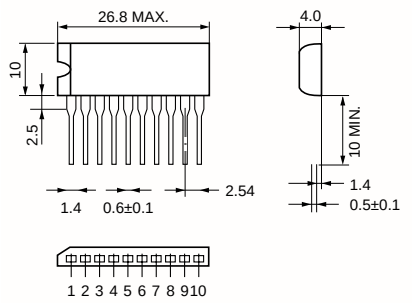
FEATURES

- Full mold package with 4 circuits
- 4 V driving is possible
- Low on-state resistance
  $R_{DS(on)1}$ = 165 mΩ MAX. (V_{GS} = 10 V, I_D = 1.5 A)
  $R_{DS(on)2}$ = 200 mΩ MAX. (V_{GS} = 4 V, I_D = 1.5 A)
- Low input capacitance
  C_{iss} = 600 pF TYP.

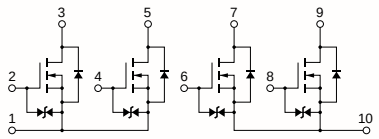
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1560H	10-pin SIP

PACKAGE DRAWING (Unit : mm)



EQUIVALENT CIRCUIT



ELECTRODE CONNECTION
2, 4, 6, 8 : Gate
3, 5, 7, 9 : Drain
1, 10 : Source

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	120	V
Gate to Source Voltage (V_{DS} = 0 V)	$V_{GSS(AC)}$	±20	V
Gate to Source Voltage (V_{DS} = 0 V)	$V_{GSS(DC)}$	+ 20, –10	V
Drain Current (DC)	$I_{D(DC)}$	±3.0	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±12	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	28	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	3.7	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to + 150	°C
Single Avalanche Current Note2	I_{AS}	3.0	A
Single Avalanche Energy Note2	E_{AS}	0.9	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Starting T_{ch} = 25 °C, V_{DD} = 60 V, R_G = 25 Ω, V_{GS} = 20 V → 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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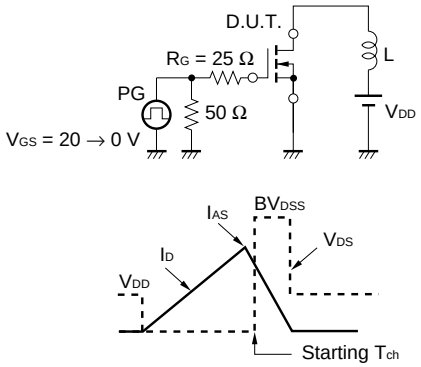
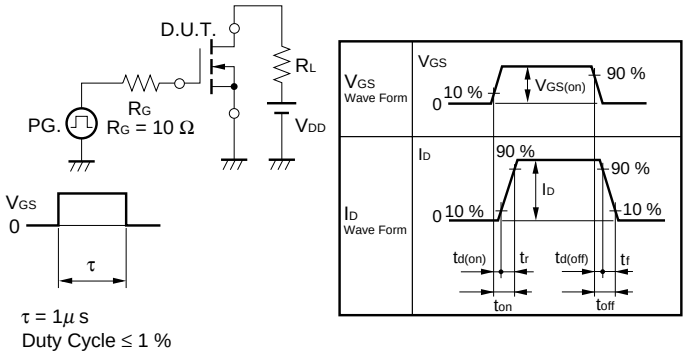
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 1.5 A		130	165	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.0 V, I_D = 1.5 A		145	200	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1.0 mA	1.0	1.8	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 1.5 A	2	4.5		S
Drain Leakage Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V		600		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		160		pF
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz		70		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 1.5 A		35		ns
Rise Time	t_r	$V_{GS(on)}$ = 10 V		80		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 60 V		700		ns
Fall Time	t_f	R_L = 30 Ω		250		ns
Total Gate Charge	Q_G	I_D = 3.0 A		28		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 96 V		2.5		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		9		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 3.0 A, V_{GS} = 0 V		0.9		V
Reverse Recovery Time	t_{rr}	I_F = 3.0 A, V_{GS} = 0 V		160		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		280		nC

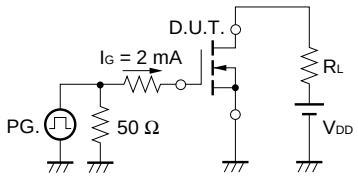
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



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