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# COMPOUND FIELD EFFECT POWER TRANSISTOR

# $\mu$ PA1576

## N-CHANNEL POWER MOS FET ARRAY

## SWITCHING TYPE

### DESCRIPTION

The  $\mu$ PA1576 is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

### FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance
  - $I_{D(pulse)} = \pm 6$  A
  - $R_{DS(on)} \leq 1.2 \Omega$  MAX. ( $V_{GS} = 10$  V)
  - $R_{DS(on)} \leq 1.5 \Omega$  MAX. ( $V_{GS} = 4$  V)
- 2.54 mm Pitch (0.1 inch)

### ORDERING INFORMATION

Part Number	Package	Quality Grade
$\mu$ PA1576H	10 pin SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

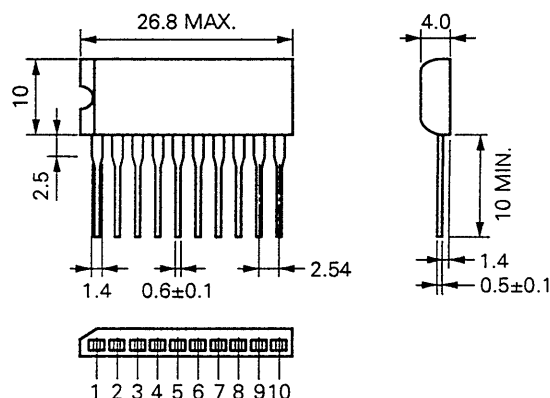
### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	100	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 2.0$	A/unit
Drain Current (pulse)	$I_{D(pulse)}^*$	$\pm 6.0$	A/unit
Total Power Dissipation (4 circuits)			
	$<T_c = 25^\circ\text{C}> P_{T1}$	28	W
Total Power Dissipation (4 circuits)			
	$<T_a = 25^\circ\text{C}> P_{T2}$	3.5	W
Storage Temperature	$T_{stg}$	$-55$ to $+150$	$^\circ\text{C}$
Junction Temperature	$T_j$	150	$^\circ\text{C}$

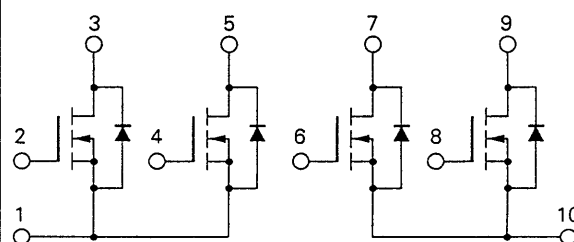
\*  $PW \leq 300 \mu\text{s}$ , Duty Cycle  $\leq 10\%$

### PACKAGE DIMENSIONS

(in millimeters)

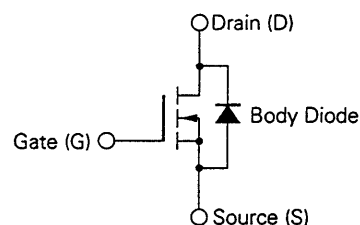


### CONNECTION DIAGRAM



### PIN No.

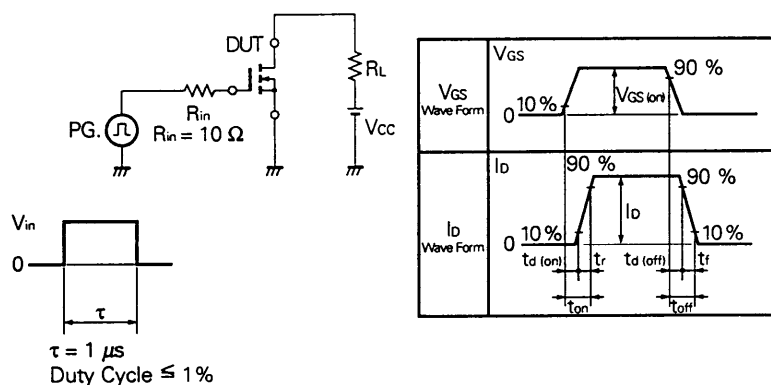
2, 4, 6, 8	Gate (G)
3, 5, 7, 9	Drain (D)
1, 10	Source (S)



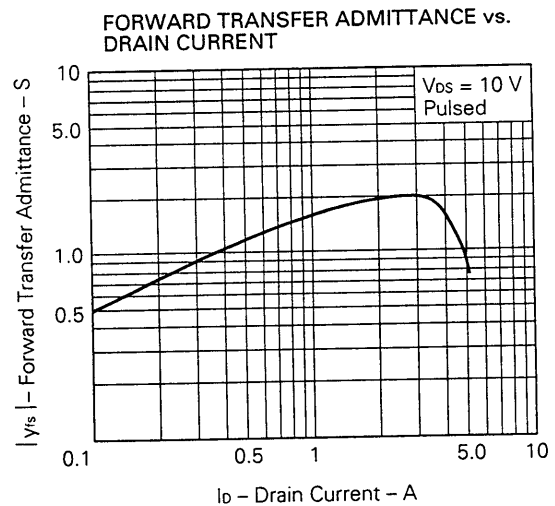
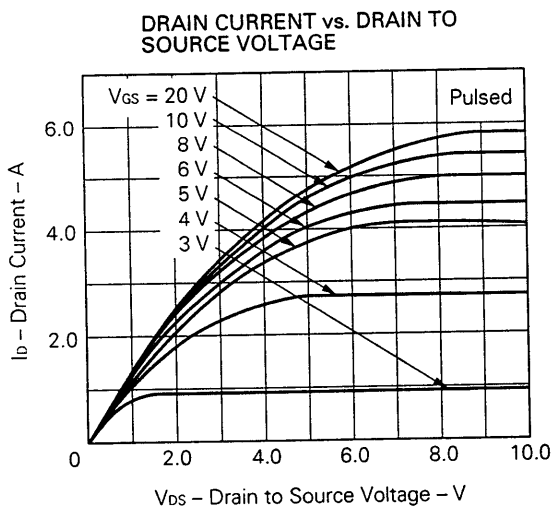
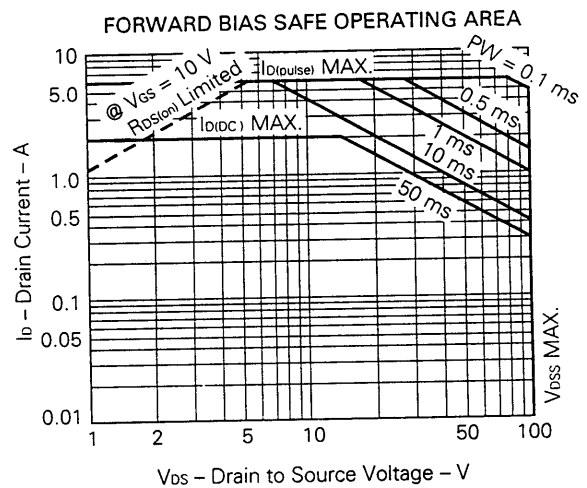
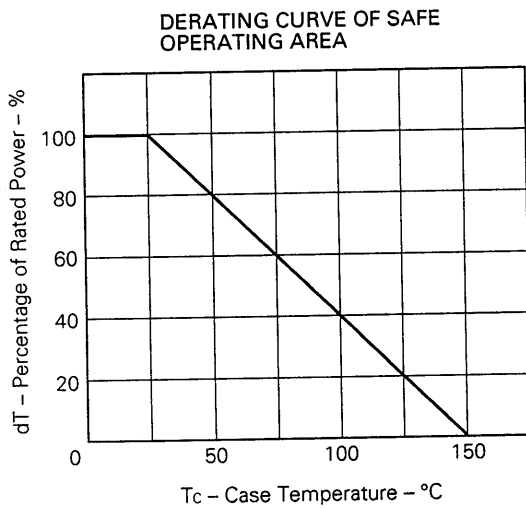
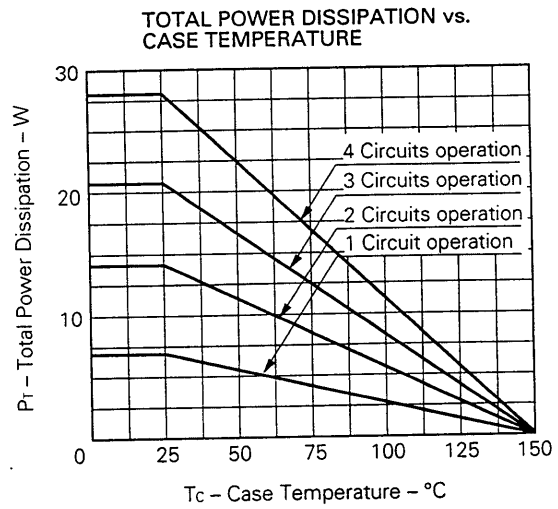
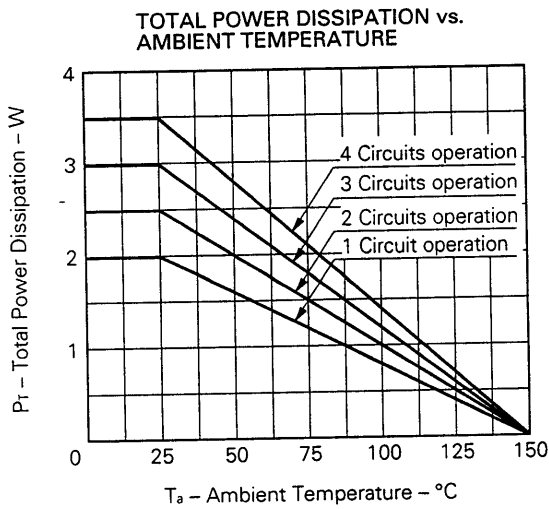
ELECTRICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	$I_{\text{DSS}}$			10	$\mu\text{A}$	$V_{\text{DS}} = 100\text{ V}$ , $V_{\text{GS}} = 0$
Gate to Source Leakage Current	$I_{\text{GSS}}$			$\pm 100$	nA	$V_{\text{GS}} = \pm 20\text{ V}$ , $V_{\text{DS}} = 0$
Gate to Source Cutoff Voltage	$V_{\text{GS(off)}}$	1.0		2.5	V	$V_{\text{DS}} = 10\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$
Forward Transfer Admittance	$ y_{\text{fs}} $	0.5	1.6		S	$V_{\text{DS}} = 10\text{ V}$ , $I_{\text{D}} = 1\text{ A}$
Drain to Source On-state Resistance	$R_{\text{DS(on)1}}$		0.8	1.2	$\Omega$	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 1\text{ A}$
Drain to Source On-state Resistance	$R_{\text{DS(on)2}}$		1.0	1.5	$\Omega$	$V_{\text{GS}} = 4\text{ V}$ , $I_{\text{D}} = 1.0\text{ A}$
Input Capacitance	$C_{\text{iss}}$		200		pF	$V_{\text{DS}} = 10\text{ V}$ $V_{\text{GS}} = 0$ $f = 1.0\text{ MHz}$
Output Capacitance	$C_{\text{oss}}$		70		pF	
Reverse Transfer Capacitance	$C_{\text{rss}}$		15		pF	
Turn-On Delay Time	$t_{\text{d(on)}}$		45		ns	$I_{\text{D}} = 1\text{ A}$ $V_{\text{GS}} = 10\text{ V}$ $V_{\text{CC}} = 50\text{ V}$ $R_{\text{L}} = 50\ \Omega$ , $R_{\text{in}} = 10\ \Omega$ See Fig. 1
Rise Time	$t_{\text{r}}$		40		ns	
Turn-Off Delay Time	$t_{\text{d(off)}}$		450		ns	
Fall Time	$t_{\text{f}}$		110		ns	

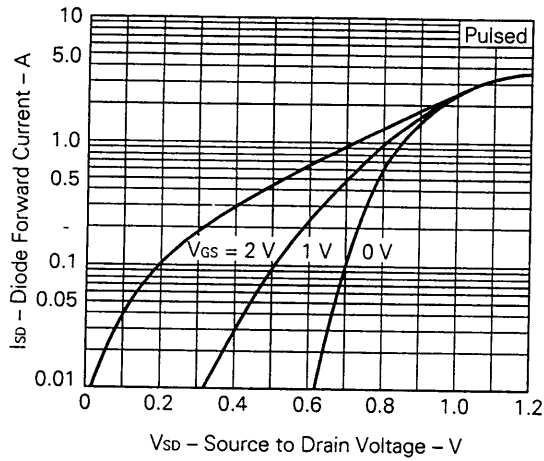
Fig. 1 Switching Time Test Circuit



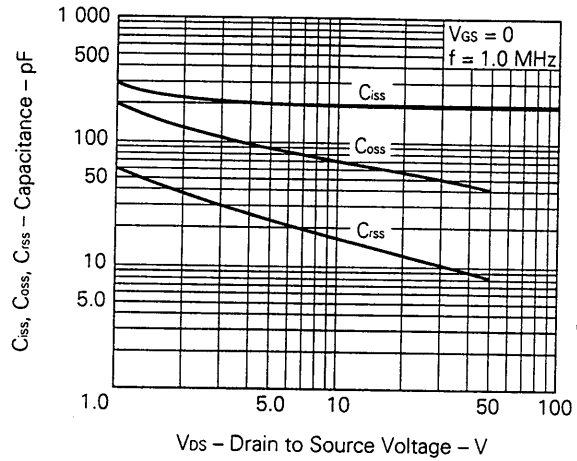
TYPICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )



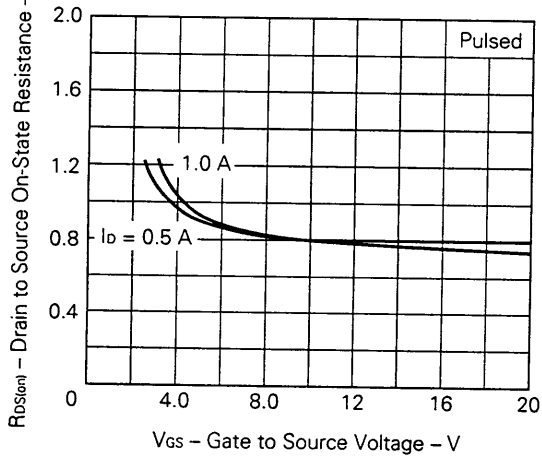
SOURCE TO DRAIN DIODE  
FORWARD VOLTAGE



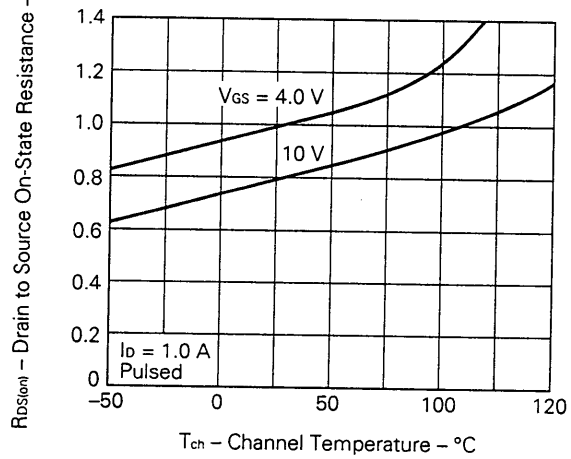
CAPACITANCE vs. DRAIN TO  
SOURCE VOLTAGE



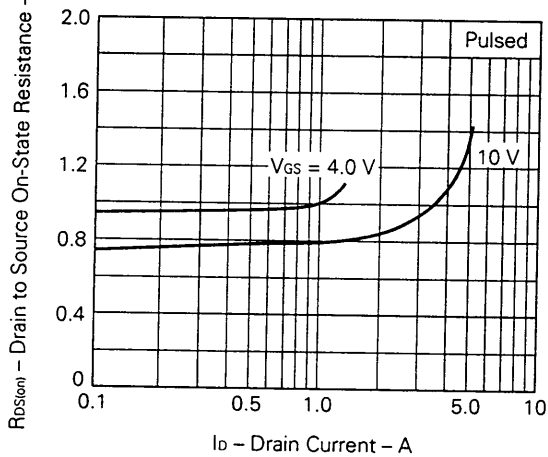
DRAIN TO SOURCE ON-STATE RESISTANCE  
vs. GATE TO SOURCE VOLTAGE



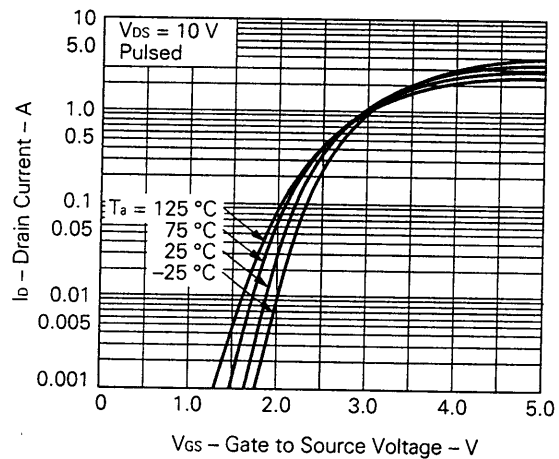
DRAIN TO SOURCE ON-STATE RESISTANCE  
vs. CHANNEL TEMPERATURE



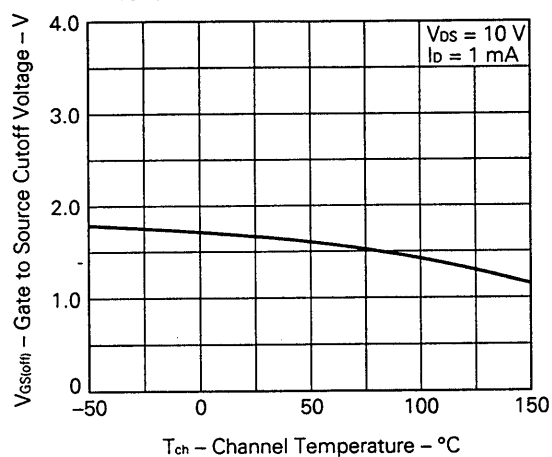
DRAIN TO SOURCE ON-STATE RESISTANCE  
vs. DRAIN CURRENT



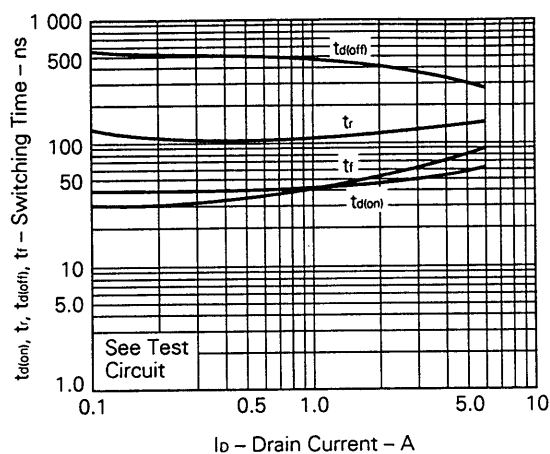
TRANSFER CHARACTERISTICS



GATE TO SOURCE CUTOFF VOLTAGE  
vs. CHANNEL TEMPERATURE



SWITCHING TIME vs. DRAIN CURRENT



## Reference

Document name	Document No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Appication circuit using Power MOS FET	TEA-1035

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