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N-CHANNEL POWER MOS FET ARRAY
SWITCHING TYPE

DESCRIPTION

The μ PA1576 is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance
 $I_D(\text{pulse}) = \pm 6 \text{ A}$
 $R_{DS(\text{on})} \leq 1.2 \Omega \text{ MAX. (}V_{GS} = 10 \text{ V)}$
 $R_{DS(\text{on})} \leq 1.5 \Omega \text{ MAX. (}V_{GS} = 4 \text{ V)}$
- 2.54 mm Pitch (0.1 inch)

ORDERING INFORMATION

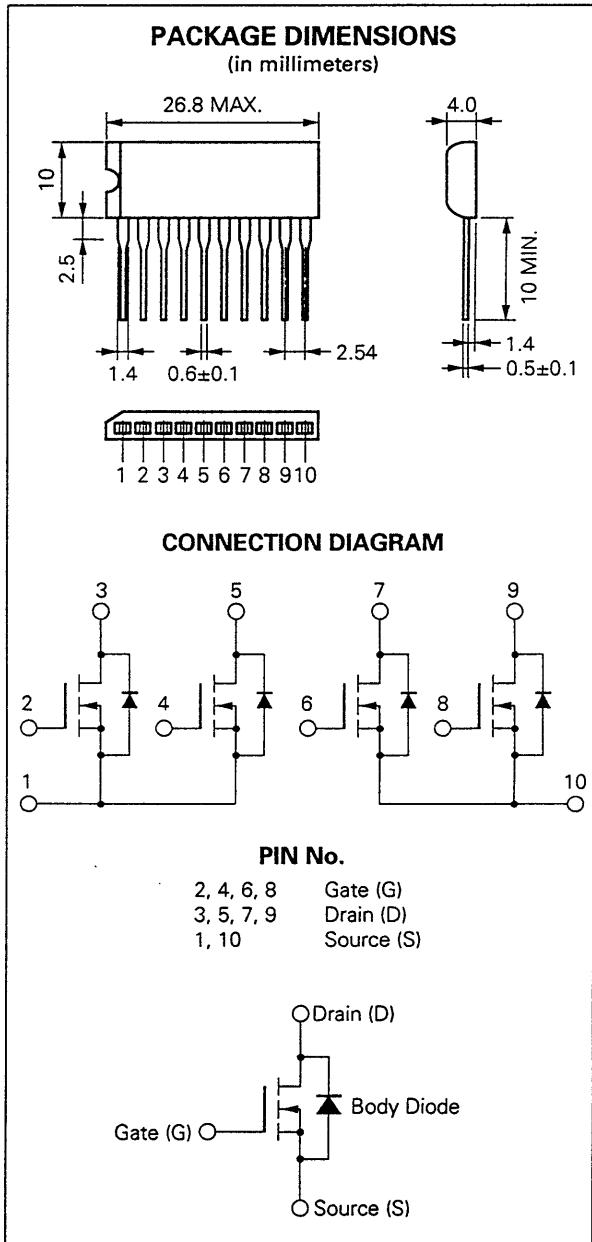
Part Number	Package	Quality Grade
μ PA1576H	10 pin SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_D(\text{DC})$	± 2.0	A/unit
Drain Current (pulse)	$I_D(\text{pulse})^*$	± 6.0	A/unit
Total Power Dissipation (4 circuits)			
$< T_c = 25^\circ\text{C} > P_{T1}$	28	W	
Total Power Dissipation (4 circuits)			
$< T_a = 25^\circ\text{C} > P_{T2}$	3.5	W	
Storage Temperature	T_{stg}	-55 to +150	°C
Junction Temperature	T_j	150	°C

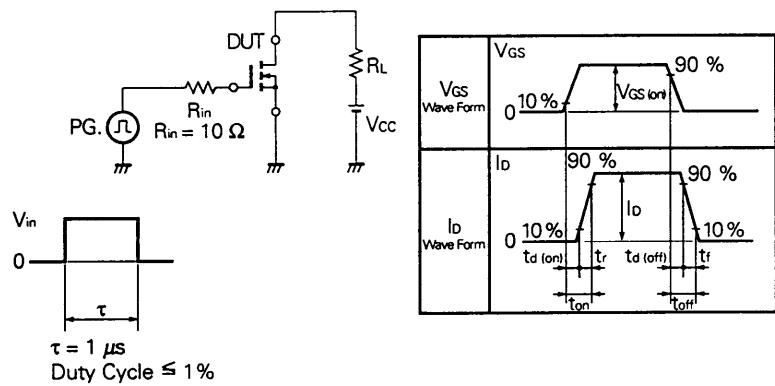
* $PW \leq 300 \mu\text{s}$, Duty Cycle $\leq 10\%$

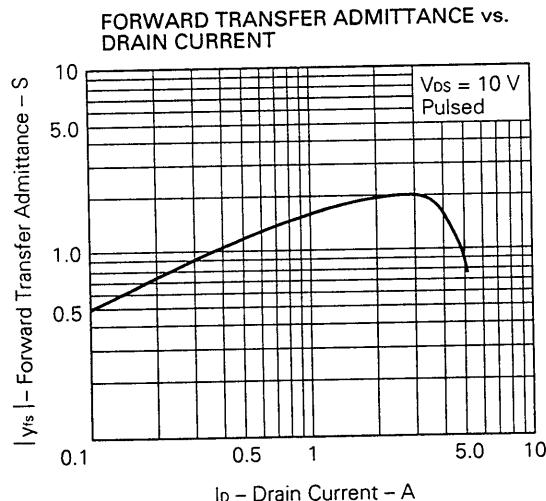
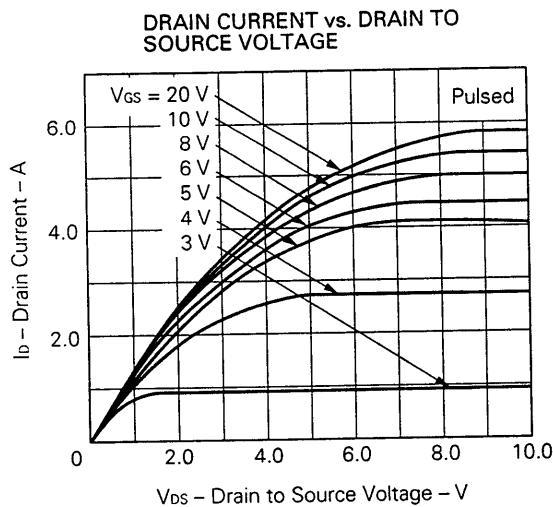
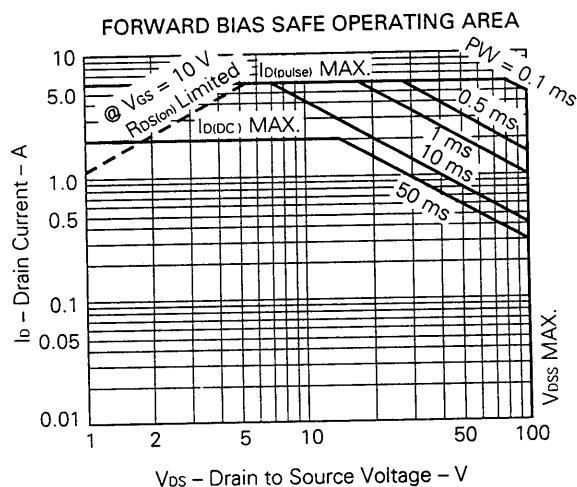
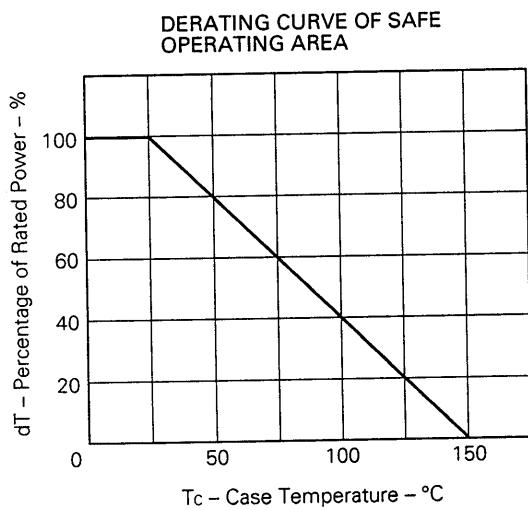
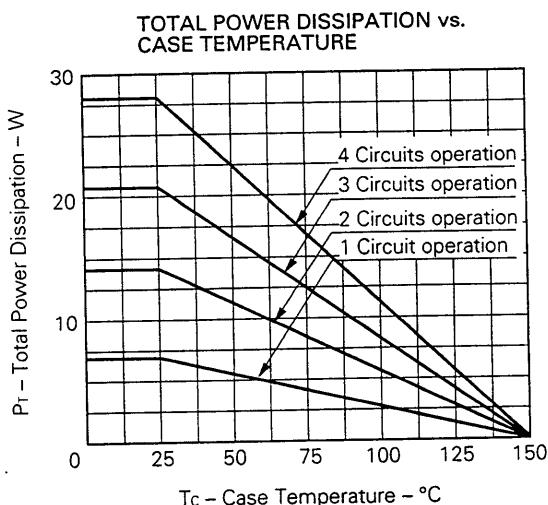
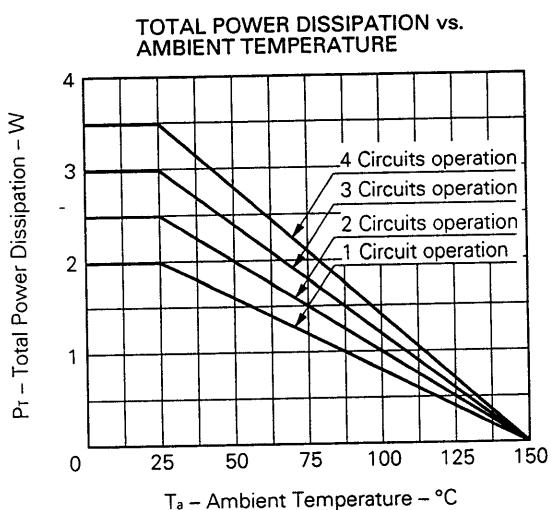


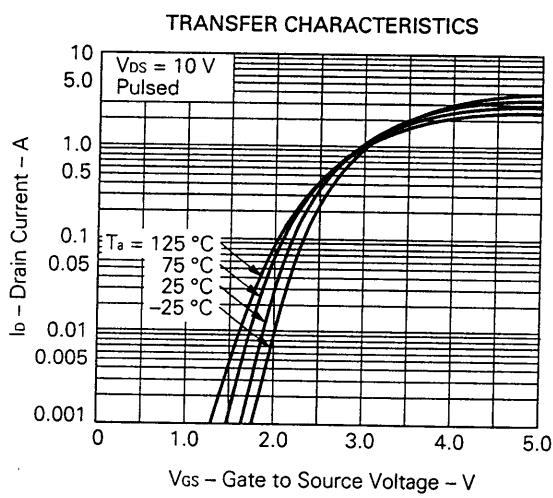
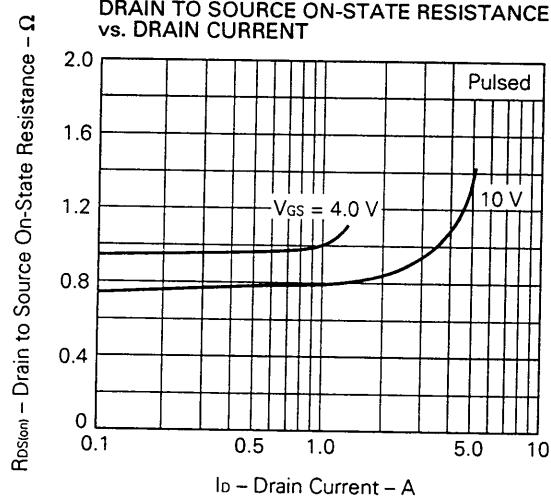
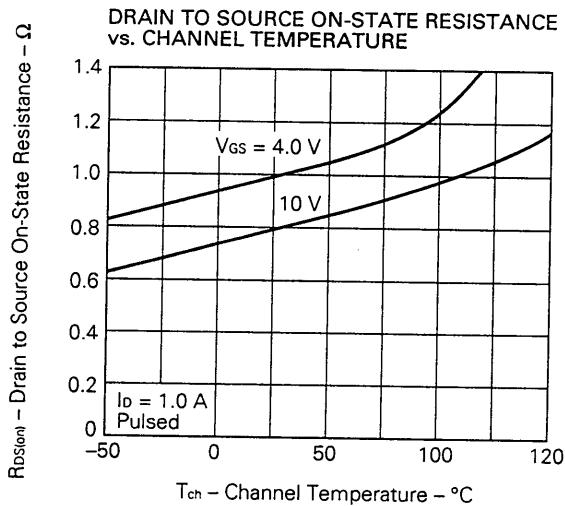
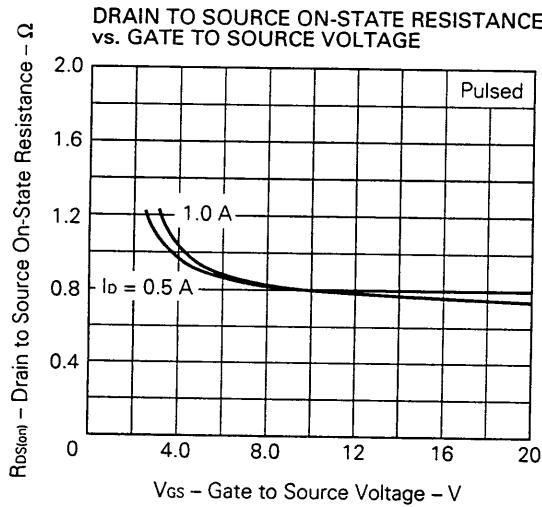
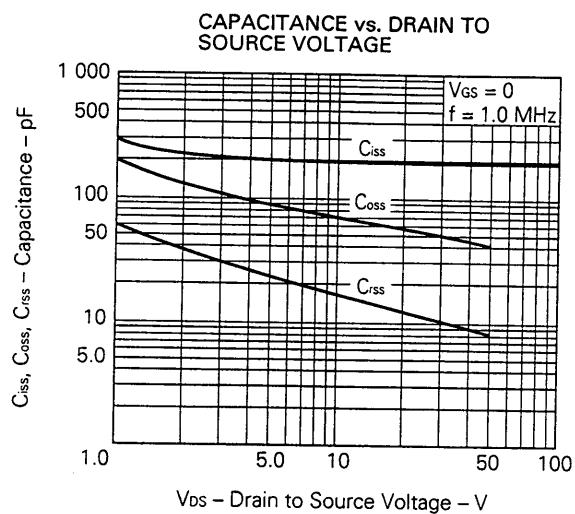
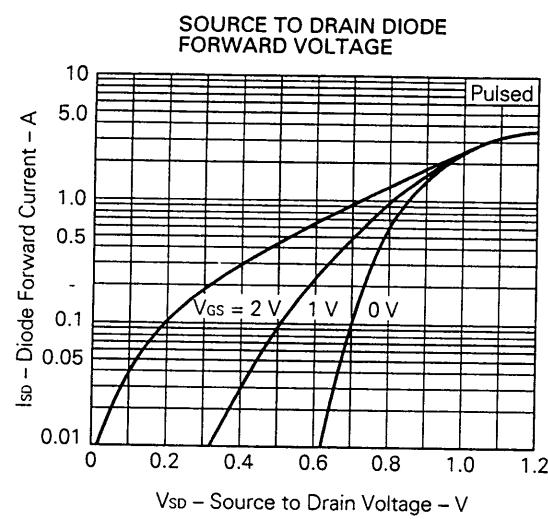
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ C$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	I_{DSS}			10	μA	$V_{DS} = 100 V, V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			± 100	nA	$V_{GS} = \pm 20 V, V_{DS} = 0$
Gate to Source Cutoff Voltage	V_{GSOFF}	1.0		2.5	V	$V_{DS} = 10 V, I_D = 1 mA$
Forward Transfer Admittance	$ Y_{FS} $	0.5	1.6		S	$V_{DS} = 10 V, I_D = 1 A$
Drain to Source On-state Resistance	$R_{DS(on)1}$		0.8	1.2	Ω	$V_{GS} = 10 V, I_D = 1 A$
Drain to Source On-state Resistance	$R_{DS(on)2}$		1.0	1.5	Ω	$V_{GS} = 4 V, I_D = 1.0 A$
Input Capacitance	C_{iss}		200		pF	$V_{DS} = 10 V$ $V_{GS} = 0$ $f = 1.0 \text{ MHz}$
Output Capacitance	C_{oss}		70		pF	
Reverse Transfer Capacitance	C_{rss}		15		pF	
Turn-On Delay Time	$t_{d(on)}$		45		ns	
Rise Time	t_r		40		ns	$I_D = 1 A$ $V_{GS} = 10 V$ $V_{CC} = 50 V$ $R_L = 50 \Omega, R_{in} = 10 \Omega$ See Fig. 1
Turn-Off Delay Time	$t_{d(off)}$		450		ns	
Fall Time	t_f		110		ns	

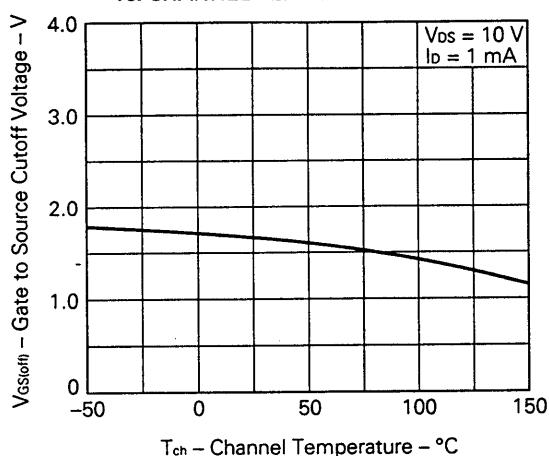
Fig. 1 Switching Time Test Circuit



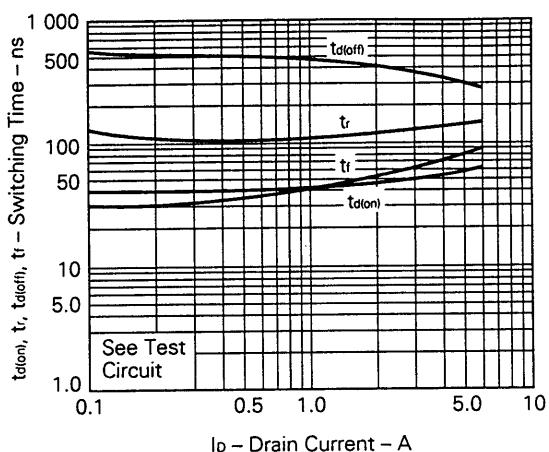
TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)



GATE TO SOURCE CUTOFF VOLTAGE
vs. CHANNEL TEMPERATURE



SWITCHING TIME vs. DRAIN CURRENT



Reference

Document name	Document No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Appication circuit using Power MOS FET	TEA-1035

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