NEC

DATA SHEET

MOS FIELD EFFECT POWER TRANSISTORS

μPA1700A

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

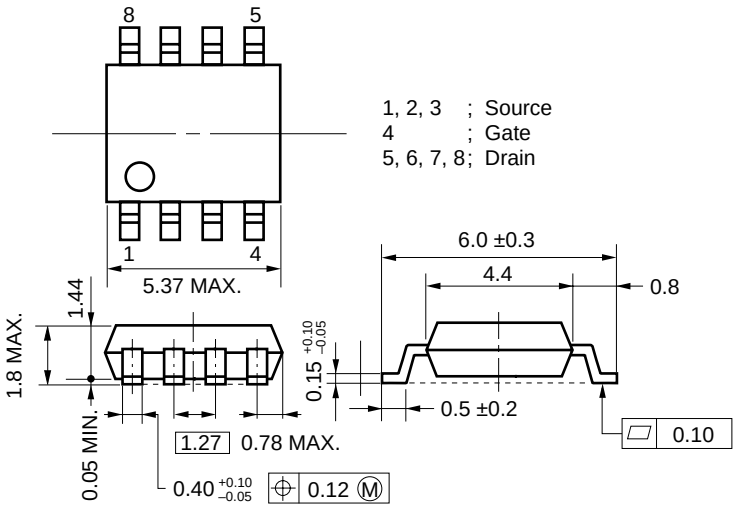
This product is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management of notebook computers.

FEATURES

- Low On-Resistance
  $R_{DS(on)1}$ = 27 mΩ Max. (V_{GS} = 10 V, I_D = 3.5 A)
  $R_{DS(on)2}$ = 50 mΩ Max. (V_{GS} = 4 V, I_D = 3.5 A)
- Low Input Capacitance
  C_{iss} = 820 pF Typ.
- Built-in G-S Protection Diode
- Small and Surface Mount Package
  (Power SOP8)

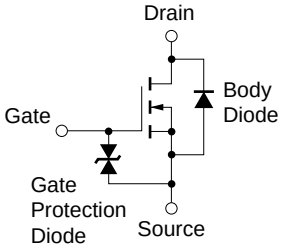
PACKAGE DIMENSIONS

(in millimeter)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, all terminals are connected)

Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±7.0	A
Drain Current (pulse)[Note 1]	$I_{D(pulse)}$	±28	A
Total Power Dissipation (T_A = 25 °C)[Note 2]	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C



Notes **1.** PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. Mounted on ceramic substrate of 1200 mm² × 1.7 mm

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

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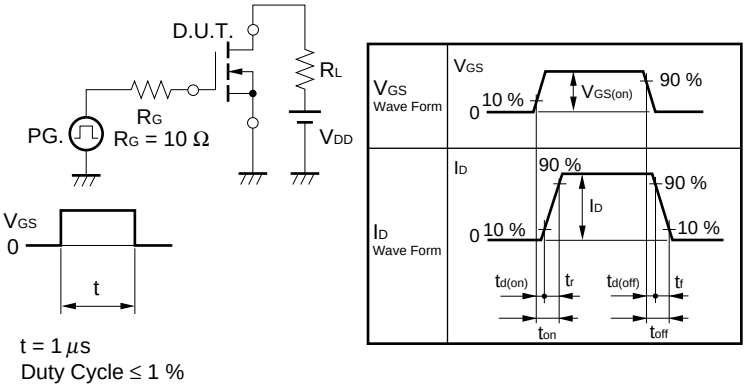
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, all terminals are connected)

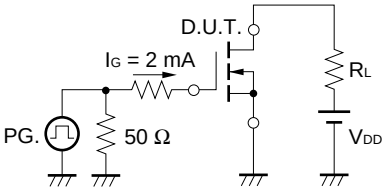
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 3.5 A		18	27	mΩ
	$R_{DS(on)2}$	V_{GS} = 4 V, I_D = 3.5 A		28	50	mΩ
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 3.5 A	5.0	9.0		S
Drain Leakage Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz		820		pF
Output Capacitance	C_{oss}			350		pF
Reverse Transfer Capacitance	C_{rss}			160		pF
Turn-On Delay Time	$t_{d(on)}$	I_D = 3.5 A $V_{GS(on)}$ = 10 V V_{DD} = 15 V R_G = 10 Ω		18		ns
Rise Time	t_r			98		ns
Turn-Off Delay Time	$t_{d(off)}$			57		ns
Fall Time	t_f			32		ns
Total Gate Charge	Q_G	I_D = 7.0 A V_{DD} = 24 V V_{GS} = 10 V		20		nC
Gate to Source Charge	Q_{GS}			2.4		nC
Gate to Drain Charge	Q_{GD}			5.6		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 7.0 A, V_{GS} = 0		0.79		V
Reverse Recovery Time	t_{rr}	I_F = 7.0 A, V_{GS} = 0 di/dt = 100 A/μs		36		ns
Reverse Recovery Charge	Q_{rr}			35		nC

Test Circuit 1 Switching Time

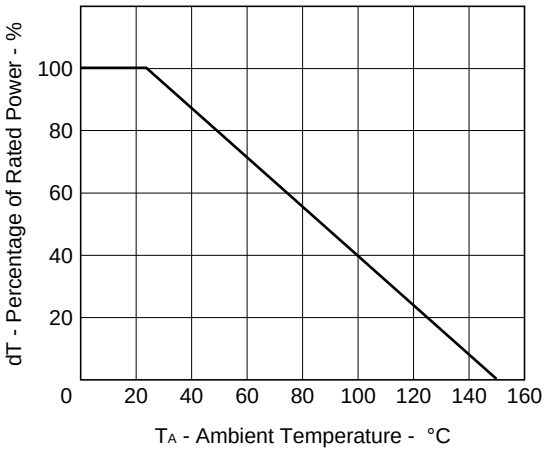


t = 1 μs
Duty Cycle ≤ 1 %

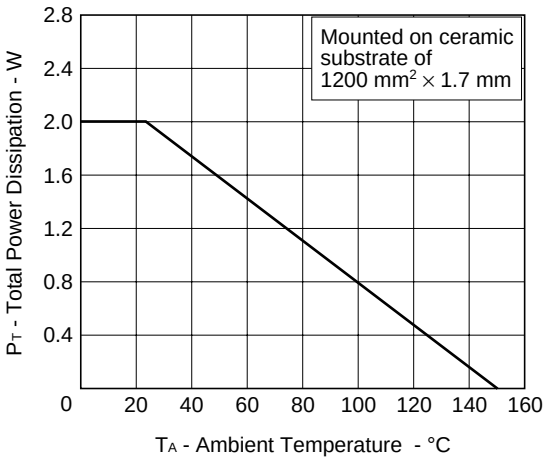
Test Circuit 2 Gate Charge



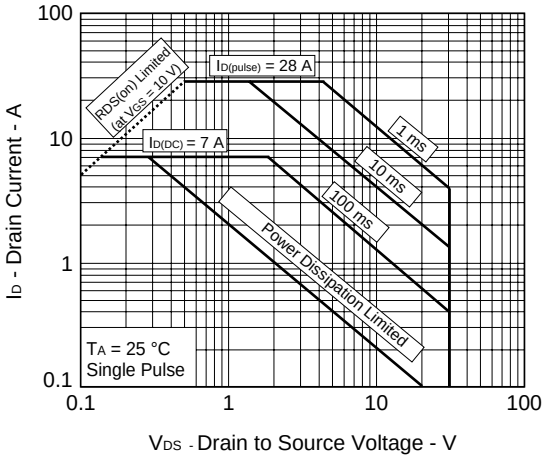
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

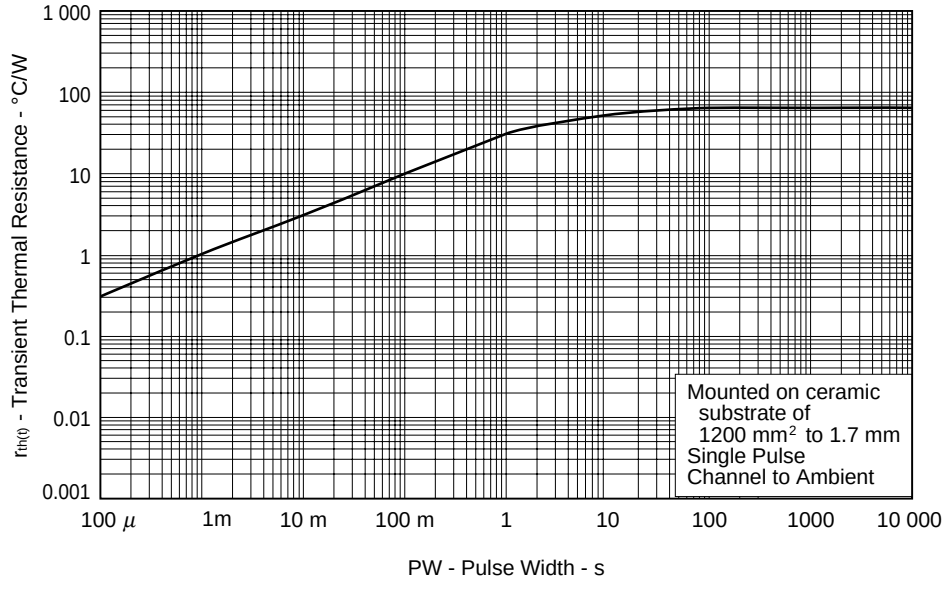


FORWARD BIAS SAFE OPERATING AREA

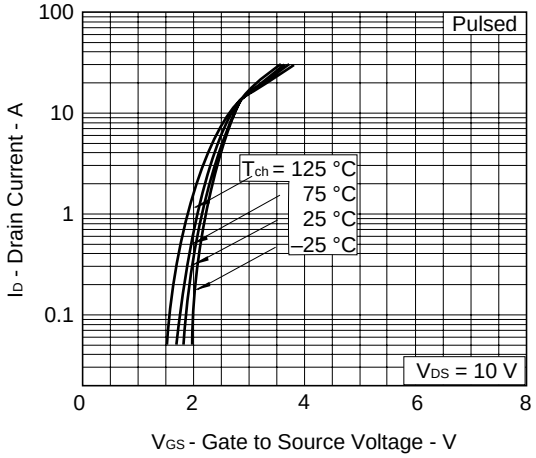


Note
Mounted on ceramic substrate of 1200 mm^2 × 1.7 mm

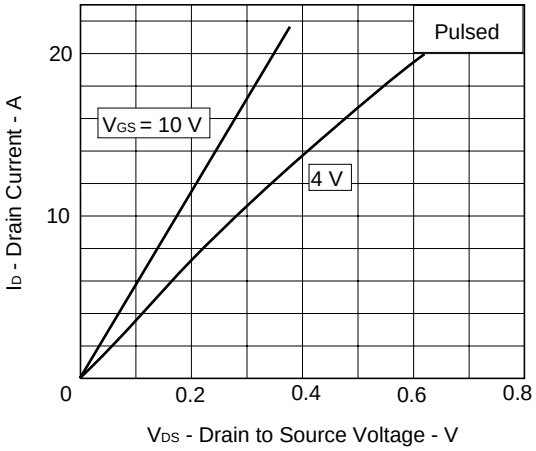
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



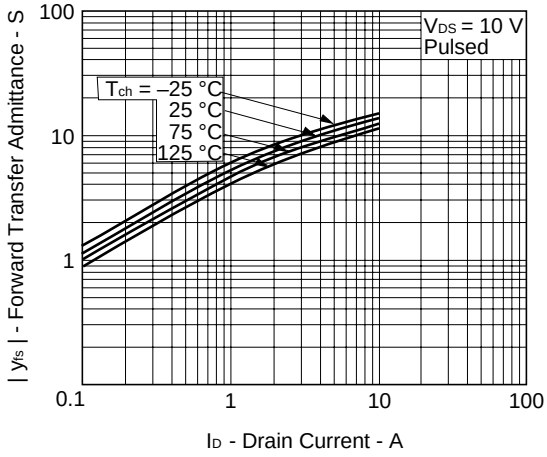
FORWARD TRANSFER CHARACTERISTICS



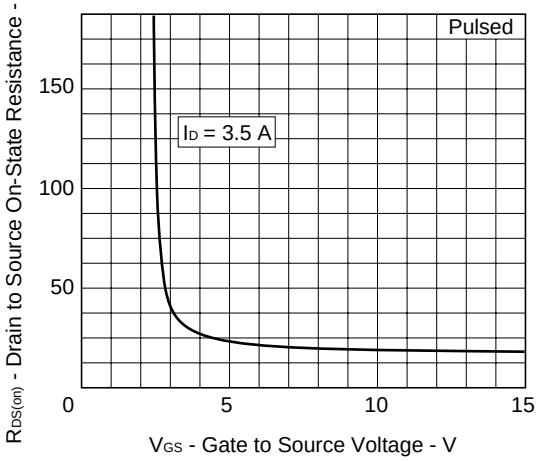
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



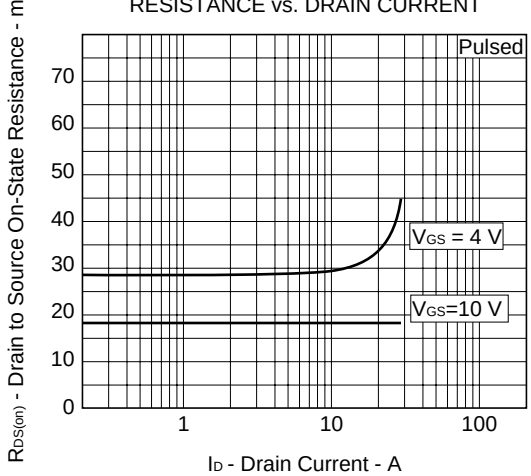
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



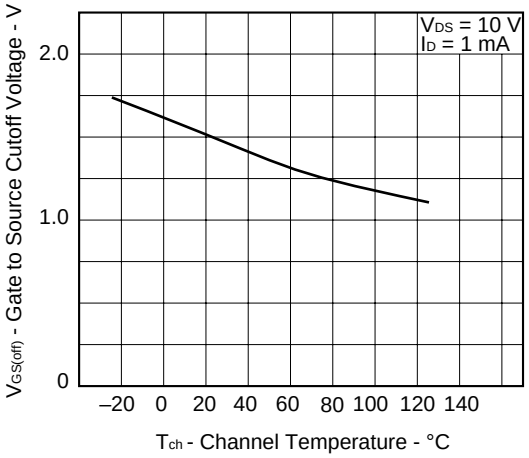
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



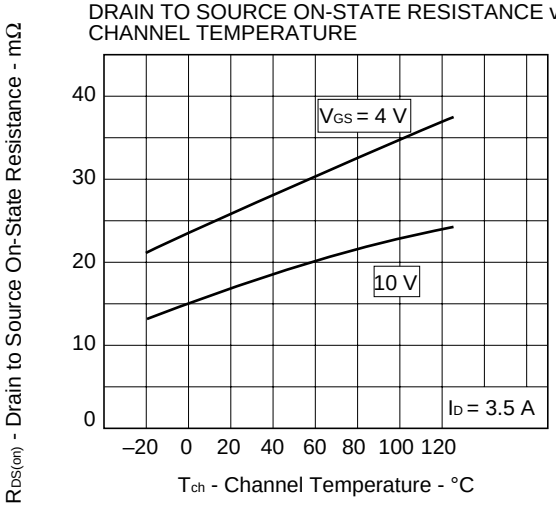
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



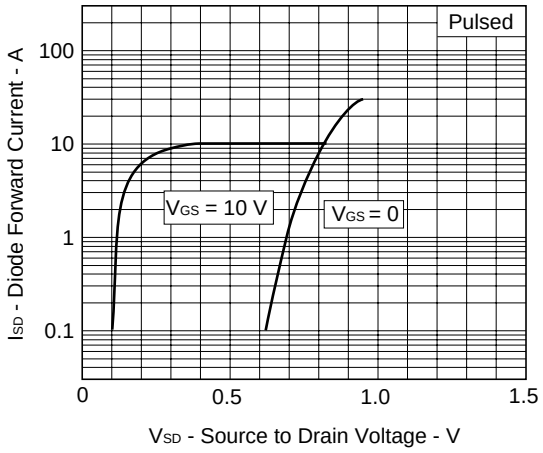
GATE TO SOURCE CUTOFF VOLTAGE vs.
CHANNEL TEMPERATURE



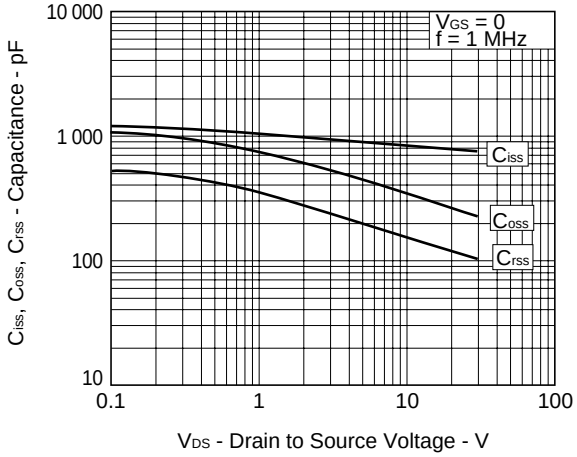
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



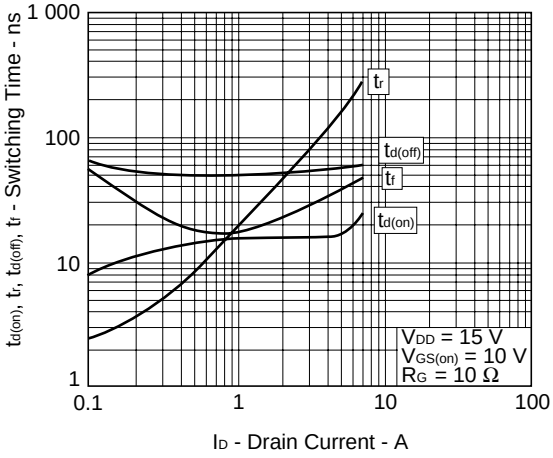
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



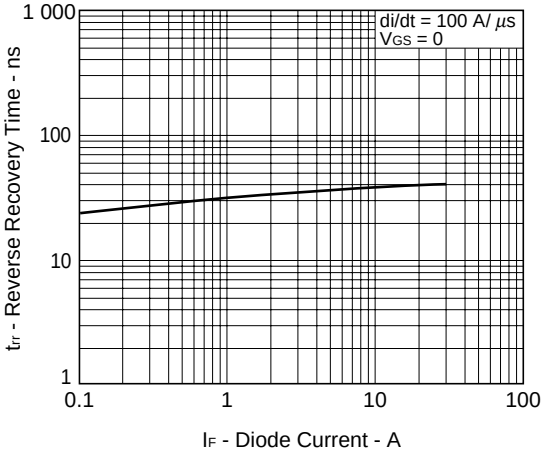
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



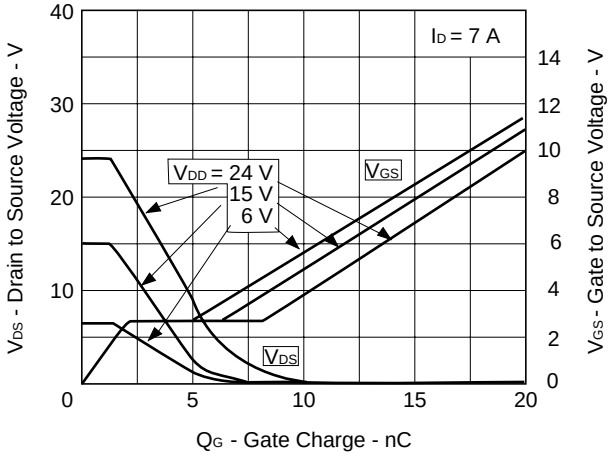
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	C11745E
Quality grade on NEC semiconductor devices	C11531E
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

[MEMO]

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