

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

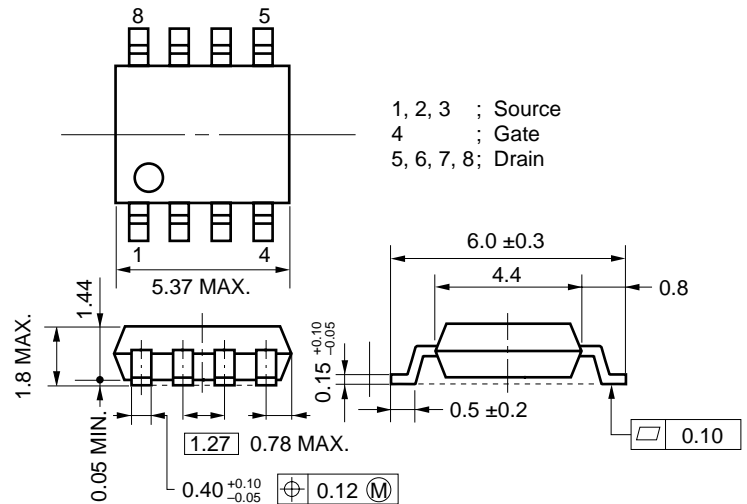
DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management of notebook computers.

FEATURES

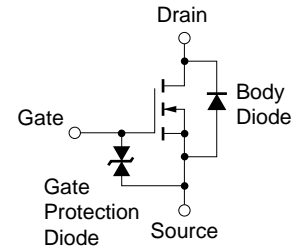
- Low On-Resistance
 $R_{DS(on)1} = 27 \text{ m}\Omega \text{ Max. (} V_{GS} = 10 \text{ V, } I_D = 3.5 \text{ A)}$
 $R_{DS(on)2} = 50 \text{ m}\Omega \text{ Max. (} V_{GS} = 4 \text{ V, } I_D = 3.5 \text{ A)}$
- Low Input Capacitance
 $C_{iss} = 820 \text{ pF Typ.}$
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

PACKAGE DIMENSIONS
(in millimeter)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$, all terminals are connected)

Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±7.0	A
Drain Current (pulse) ^{Note 1}	$I_{D(pulse)}$	±28	A
Total Power Dissipation ($T_A = 25 \text{ }^\circ\text{C}$) ^{Note 2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$



- Notes**
1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1 \%$
 2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 1.7 \text{ mm}$

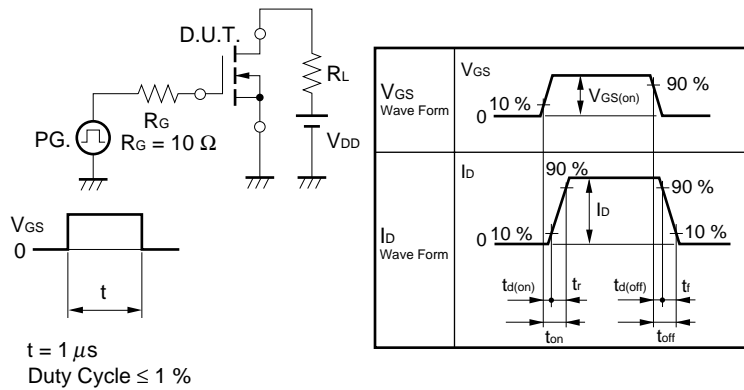
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

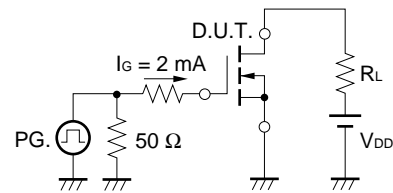
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, all terminals are connected)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 3.5 A		18	27	mΩ
	R _{DS(on)2}	V _{GS} = 4 V, I _D = 3.5 A		28	50	mΩ
Gate to Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 3.5 A	5.0	9.0		S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0			±10	μA
Input Capacitance	C _{iSS}	V _{DS} = 10 V		820		pF
Output Capacitance	C _{oSS}	V _{GS} = 0		350		pF
Reverse Transfer Capacitance	C _{rSS}	f = 1 MHz		160		pF
Turn-On Delay Time	t _{d(on)}	I _D = 3.5 A		18		ns
Rise Time	t _r	V _{GS(on)} = 10 V		98		ns
Turn-Off Delay Time	t _{d(off)}	V _{DD} = 15 V		57		ns
Fall Time	t _f	R _G = 10 Ω		32		ns
Total Gate Charge	Q _G	I _D = 7.0 A		20		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 24 V		2.4		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		5.6		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 7.0 A, V _{GS} = 0		0.79		V
Reverse Recovery Time	t _{rr}	I _F = 7.0 A, V _{GS} = 0		36		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		35		nC

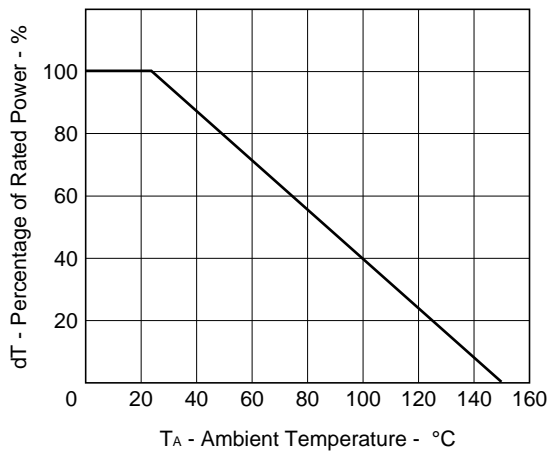
Test Circuit 1 Switching Time



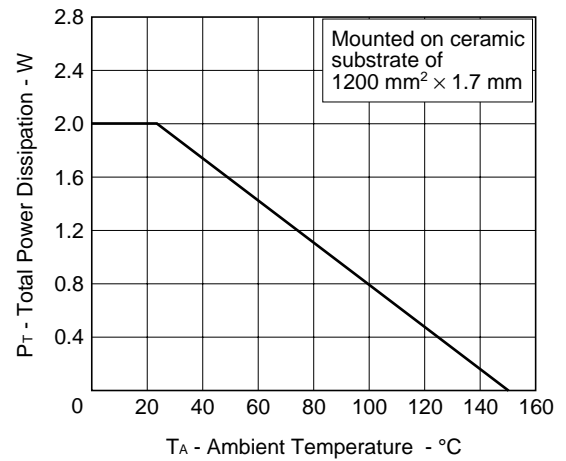
Test Circuit 2 Gate Charge



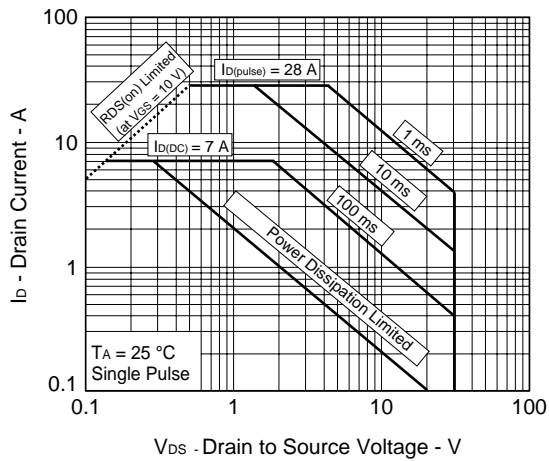
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

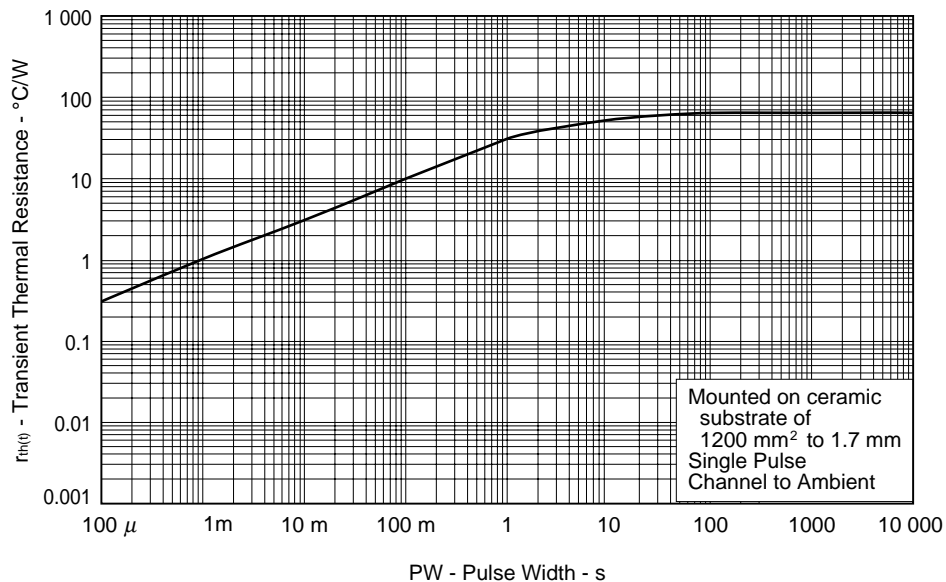


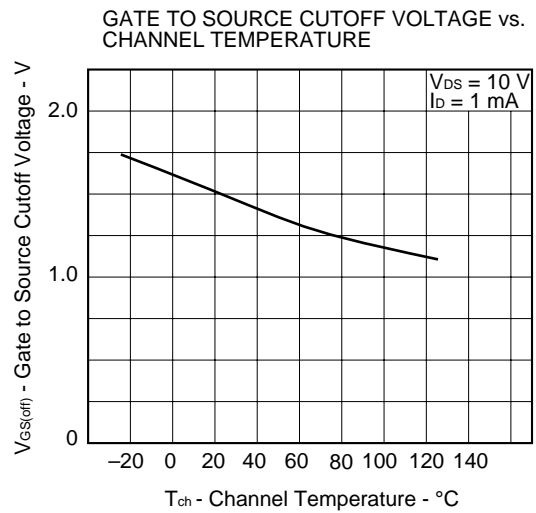
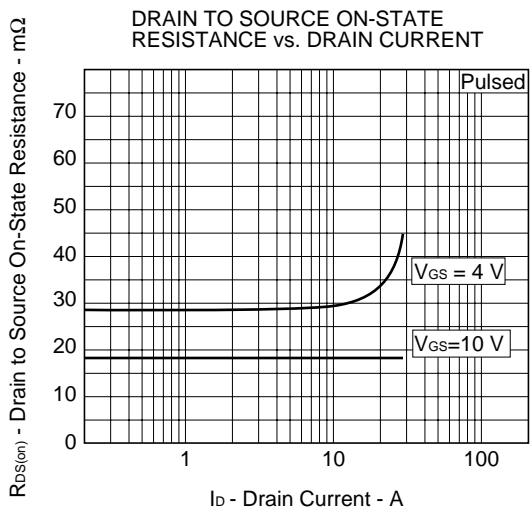
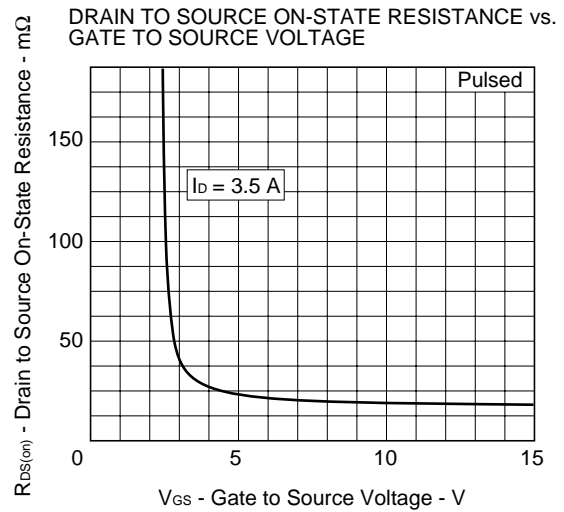
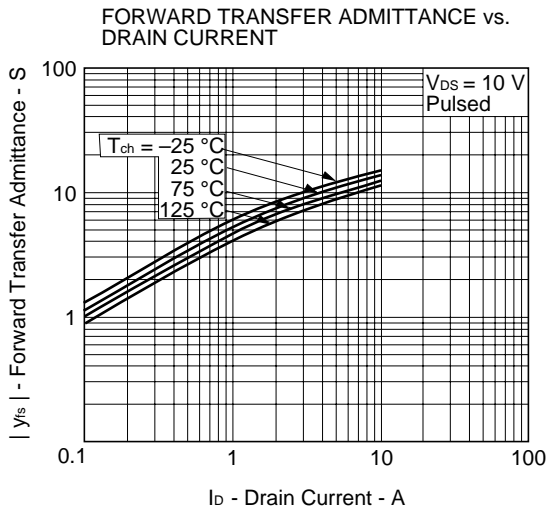
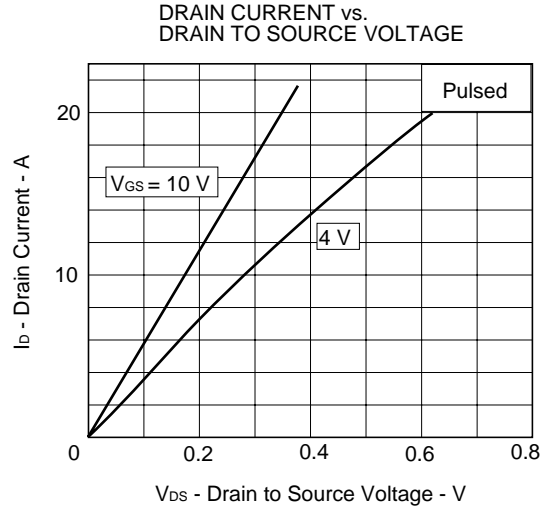
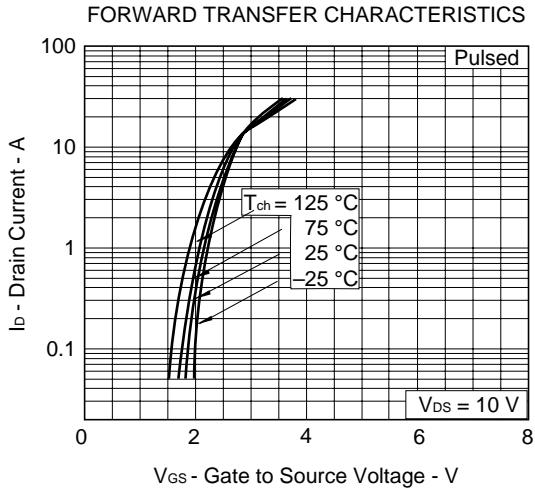
FORWARD BIAS SAFE OPERATING AREA

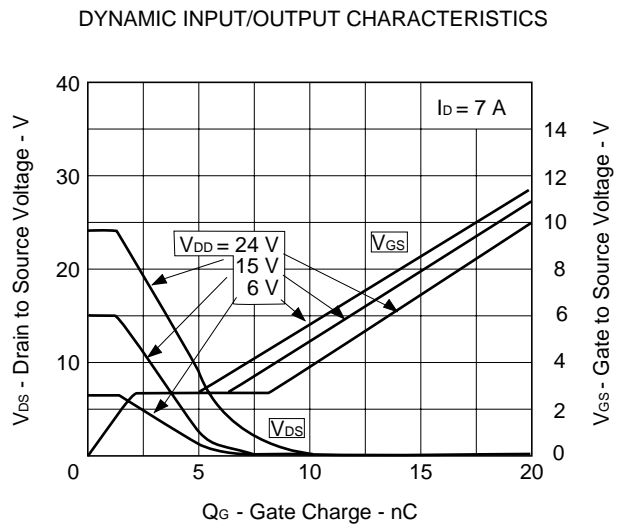
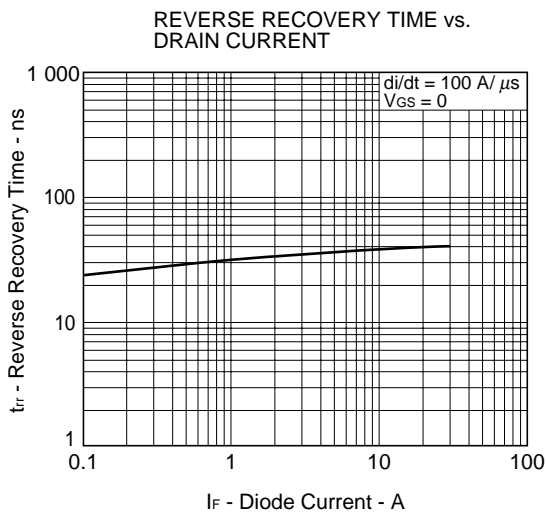
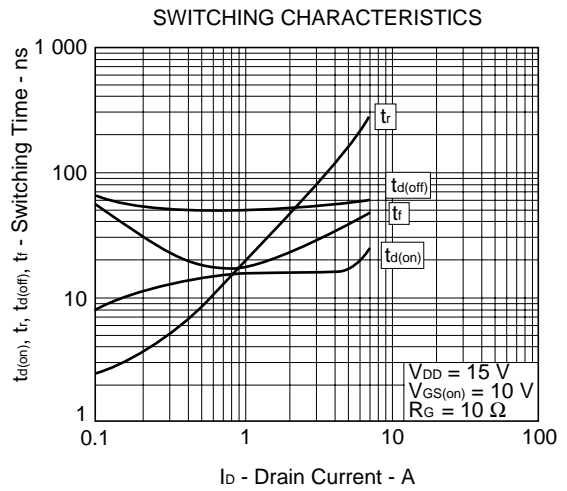
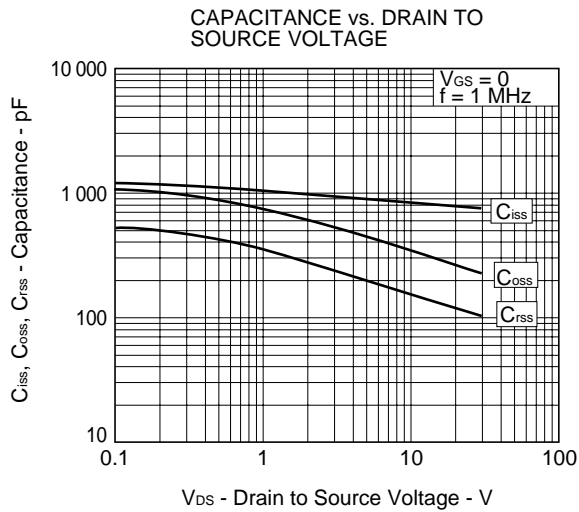
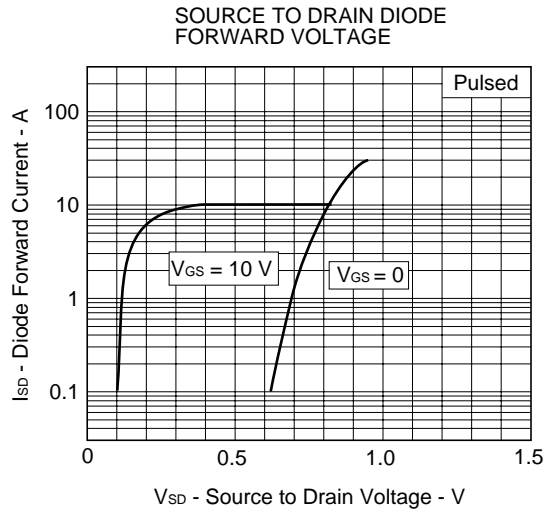
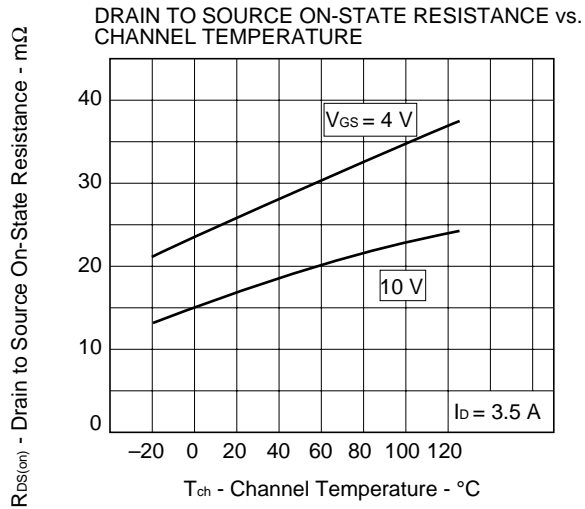


Note
Mounted on ceramic substrate of 1200 mm² x 1.7 mm

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH







REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	C11745E
Quality grade on NEC semiconductor devices	C11531E
Semiconductor device mounting technology manual	C10535E
Semiconductor device package manual	C10943X
Guide to quality assurance for semiconductor devices	MEI-1202
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037

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Anti-radioactive design is not implemented in this product.