

# MOS FIELD EFFECT TRANSISTOR

## $\mu$ PA1709

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

This product is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management switch.

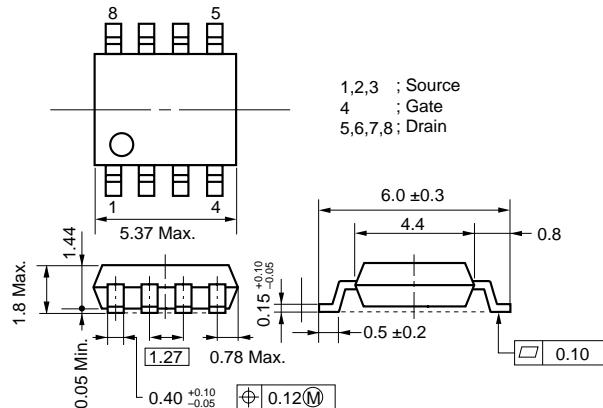
#### FEATURES

- Low on-resistance  
 $R_{DS(on)1} = 9.3 \text{ m}\Omega$  (TYP.) ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 4.5 \text{ A}$ )  
 $R_{DS(on)2} = 13.8 \text{ m}\Omega$  (TYP.) ( $V_{GS} = 4.5 \text{ V}$ ,  $I_D = 4.5 \text{ A}$ )
- Low  $C_{iss}$  :  $C_{iss} = 1850 \text{ pF}$  (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

#### ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA1709G	Power SOP8

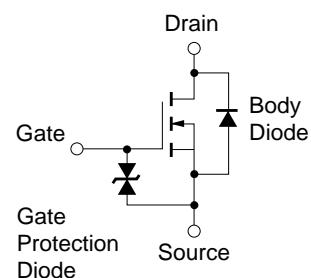
#### PACKAGE DRAWING (Unit : mm)



#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , All terminals are connected.)

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	40	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 25$	V
Drain Current (DC)	$I_D(\text{DC})$	$\pm 9.0$	A
Drain Current (pulse) <sup>Note1</sup>	$I_D(\text{pulse})$	$\pm 36$	A
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>Note2</sup>	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to + 150	$^\circ\text{C}$

#### EQUIVARENT CIRCUIT



**Notes 1.** PW  $\leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1 \%$

2. Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 0.7 \text{ mm}$

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD.

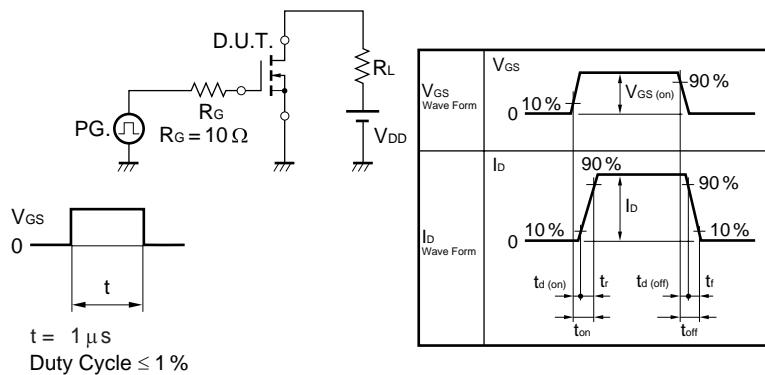
When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

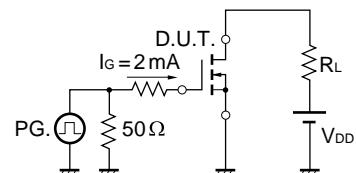
## ELECTRICAL CHARACTERISTICS (TA = 25 °C, All terminals are connected.)

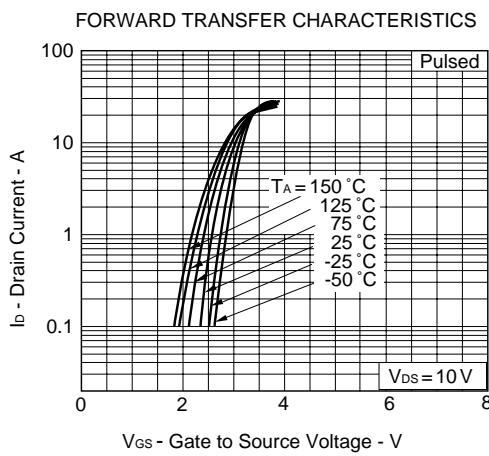
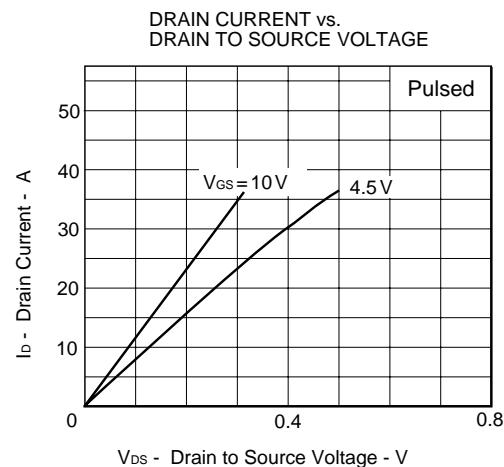
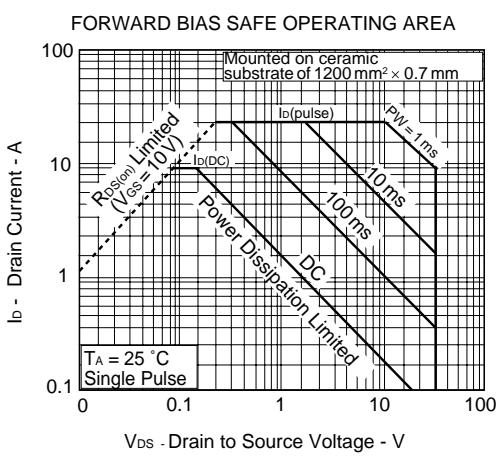
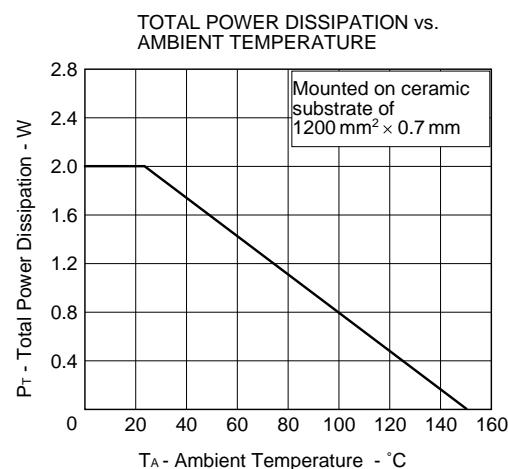
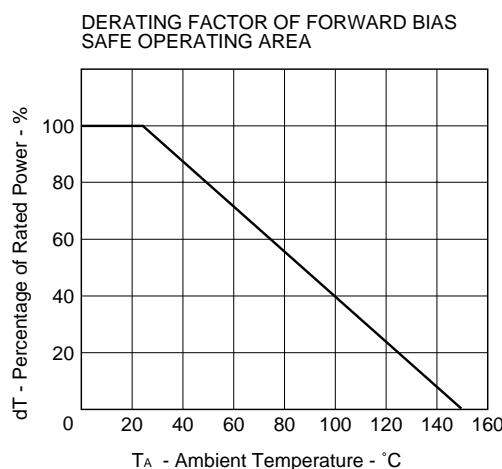
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 4.5 A		9.3	12.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.5 A		13.8	20.0	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 4.5 A	8.0	14		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GS</sub>	V <sub>GS</sub> = ±25 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V V <sub>GS</sub> = 0 V f = 1 MHz		1850		pF
Output Capacitance	C <sub>oss</sub>			790		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			330		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 4.5 A V <sub>GS(on)</sub> = 10 V V <sub>DD</sub> = 20 V R <sub>G</sub> = 10 Ω		27		ns
Rise Time	t <sub>r</sub>			95		ns
Turn-off Delay Time	t <sub>d(off)</sub>			110		ns
Fall Time	t <sub>f</sub>			70		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 9.0 A V <sub>DD</sub> = 32 V V <sub>GS</sub> = 10 V		43.0		nC
Gate to Source Charge	Q <sub>GS</sub>			6.0		nC
Gate to Drain Charge	Q <sub>GD</sub>			14.0		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 9.0 A, V <sub>GS</sub> = 0 V		0.78		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 9.0 A, V <sub>GS</sub> = 0 V di/dt = 100 A/μs		47		ns
Reverse Recovery Charge	Q <sub>rr</sub>			44		nC

## TEST CIRCUIT 1 SWITCHING TIME

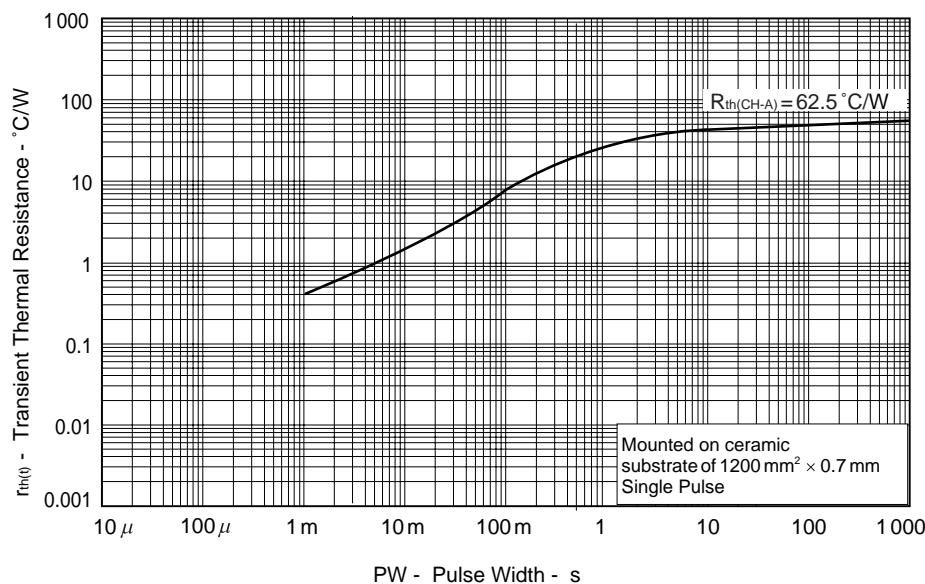


## TEST CIRCUIT 2 GATE CHARGE

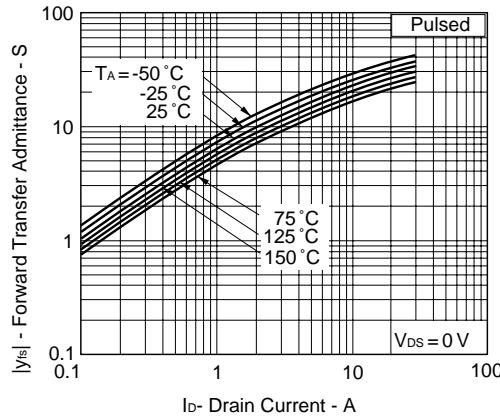


TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

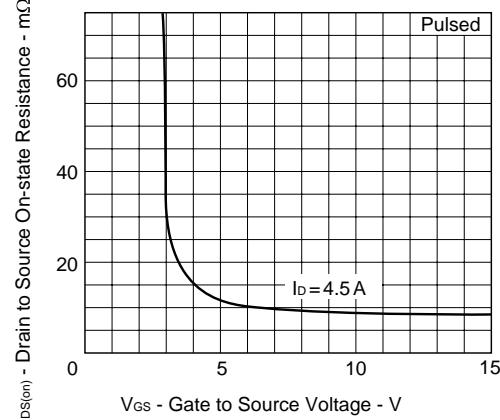
## TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



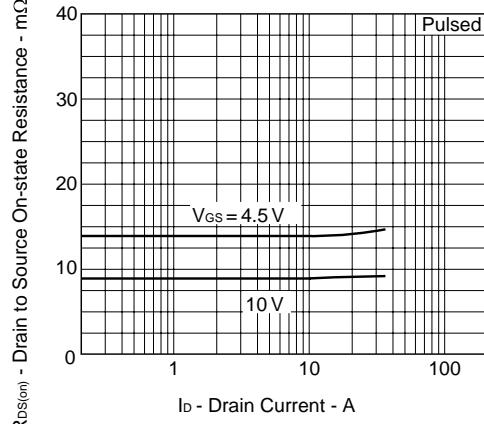
## FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



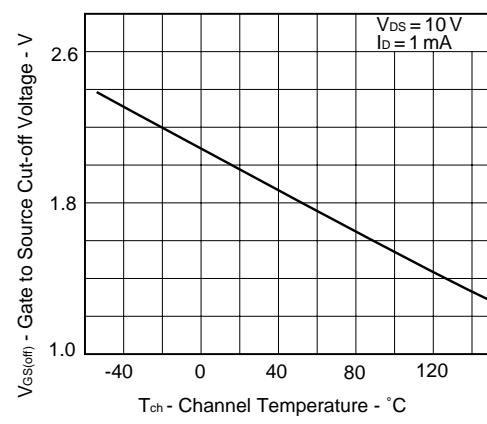
## DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

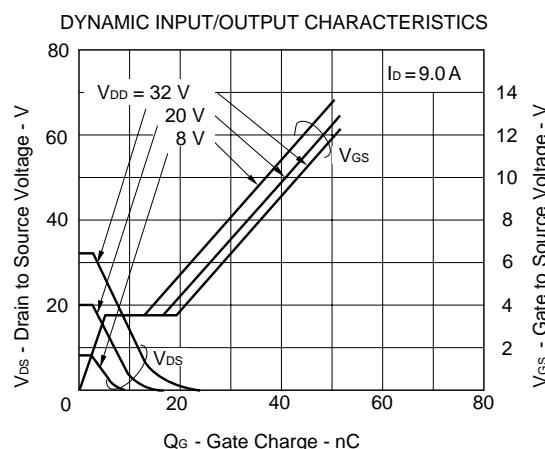
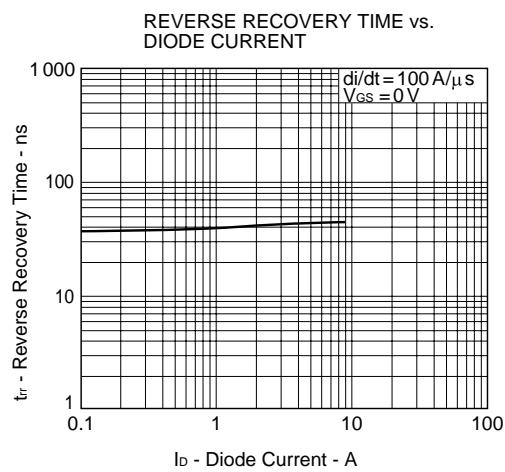
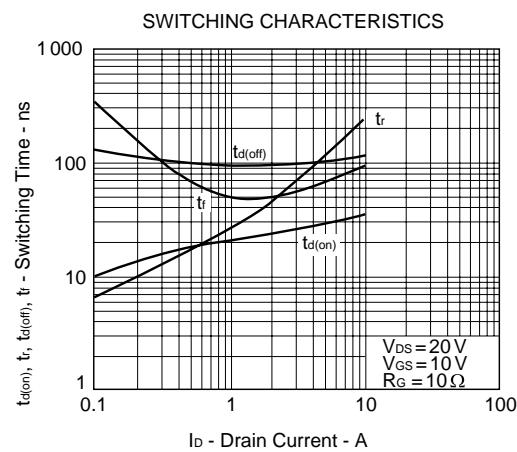
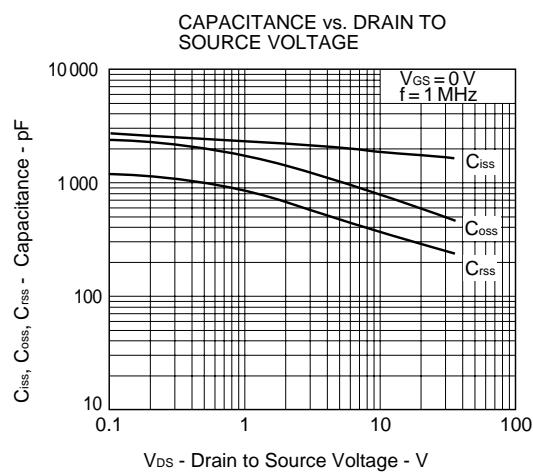
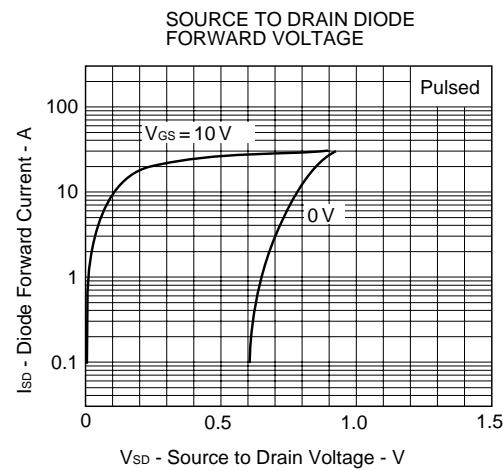
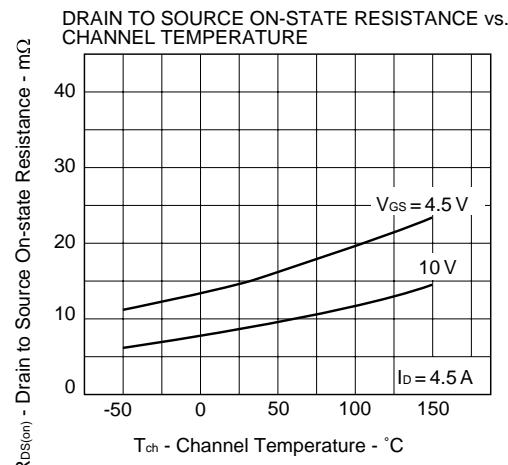


## DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



## GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE





**[MEMO]**

**[MEMO]**

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Anti-radioactive design is not implemented in this product.