NEC

DATA SHEET

# MOS FIELD EFFECT TRANSISTOR
# μPA1741TP

## SWITCHING
## N-CHANNEL POWER MOS FET

### DESCRIPTION

The μPA1741TP is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

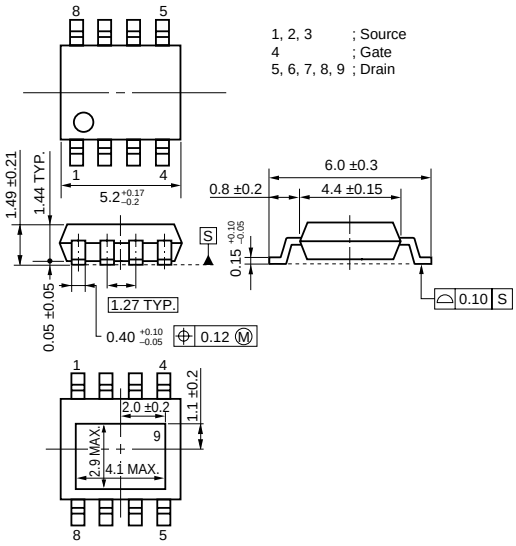
### FEATURES

- High voltage: $V_{DSS}$ = 250 V
- Gate voltage rating: ±30 V
- Low on-state resistance
  $R_{DS(on)}$ = 0.79 Ω MAX. ($V_{GS}$ = 10 V, $I_D$ = 2.5 A)
- Low input capacitance
  $C_{iss}$ = 340 pF TYP. ($V_{DS}$ = 10 V, $V_{GS}$ = 0 V)
- Built-in gate protection diode
- Small and surface mount package (Power HSOP8)

### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| μPA1741TP | Power HSOP8 |

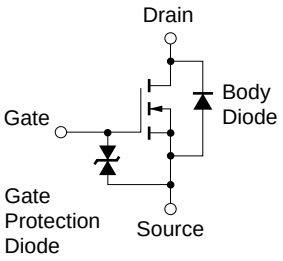
### PACKAGE DRAWING (Unit: mm)




### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C, unless otherwise noted. All terminals are connected.)

| | | | |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0 V) | $V_{DSS}$ | 250 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) | $V_{GSS}$ | ±30 | V |
| Drain Current (DC) ($T_C$ = 25°C) | $I_{D(DC)}$ | ±5.0 | A |
| Drain Current (pulse) Note1 | $I_{D(pulse)}$ | ±15 | A |
| Total Power Dissipation ($T_C$ = 25°C) | $P_{T1}$ | 21 | W |
| Total Power Dissipation ($T_A$ = 25°C) Note2 | $P_{T2}$ | 1 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | °C |
| Single Avalanche Current Note3 | $I_{AS}$ | 5.0 | A |
| Single Avalanche Energy Note3 | $E_{AS}$ | 2.5 | mJ |
| Repetitive Avalanche Current Note4 | $I_{AR}$ | 5.0 | A |
| Repetitive Pulse Avalanche Energy Note4 | $E_{AR}$ | 2.5 | mJ |

### EQUIVALENT CIRCUIT




**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%
**2.** Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm
**3.** Starting $T_{ch}$ = 25°C, $V_{DD}$ = 125 V, $R_G$ = 25 Ω, L = 100 μH, $V_{GS}$ = 20 → 0 V
**4.** $T_{ch(peak)}$ ≤ 150°C, L = 100 μH

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.



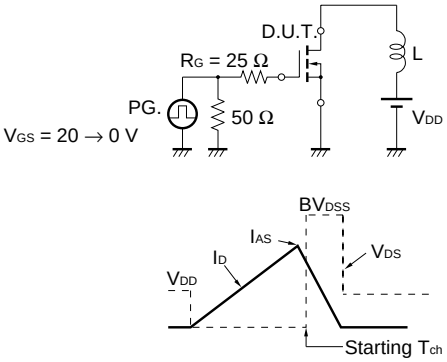
Document No. G16373EJ1V0DS00 (1st edition)
Date Published April 2003 NS CP(K)
Printed in Japan

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C, unless otherwise noted. All terminals are connected.)

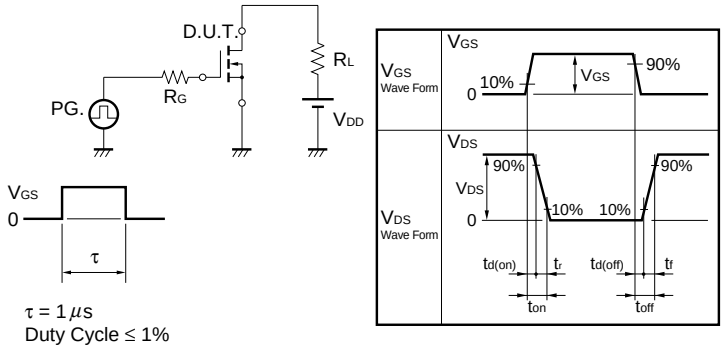
| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 250 V, $V_{GS}$ = 0 V | | | 10 | μA |
| Gate Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±30 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| Gate Cut-off Voltage | $V_{GS(off)}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 2.5 | 3.5 | 4.5 | V |
| Forward Transfer Admittance **Note** | $\|y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 2.5 A | 2 | 3.5 | | S |
| Drain to Source On-state Resistance **Note** | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 2.5 A | | 0.63 | 0.79 | Ω |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V | | 340 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | | 70 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 30 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$ = 125 V, $I_D$ = 2.5 A | | 11 | | ns |
| Rise Time | $t_r$ | $V_{GS}$ = 10 V | | 8 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $R_G$ = 10 Ω | | 20 | | ns |
| Fall Time | $t_f$ | | | 6 | | ns |
| Total Gate Charge | $Q_G$ | $V_{DD}$ = 200 V | | 11 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{GS}$ = 10 V | | 2 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $I_D$ = 5.0 A | | 5.5 | | nC |
| Body Diode Forward Voltage **Note** | $V_{F(S-D)}$ | $I_F$ = 5.0 A, $V_{GS}$ = 0 V | | 0.9 | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = 5.0 A, $V_{GS}$ = 0 V | | 120 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 100 A/μs | | 400 | | nC |

**Note** Pulsed: PW ≤ 800 μs, Duty Cycle ≤ 2%

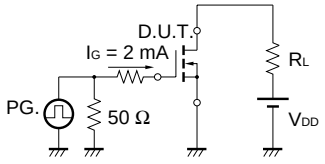
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**




**TEST CIRCUIT 2 SWITCHING TIME**

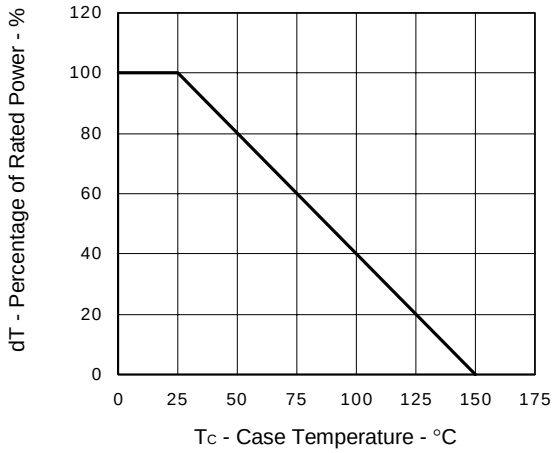



**TEST CIRCUIT 3 GATE CHARGE**

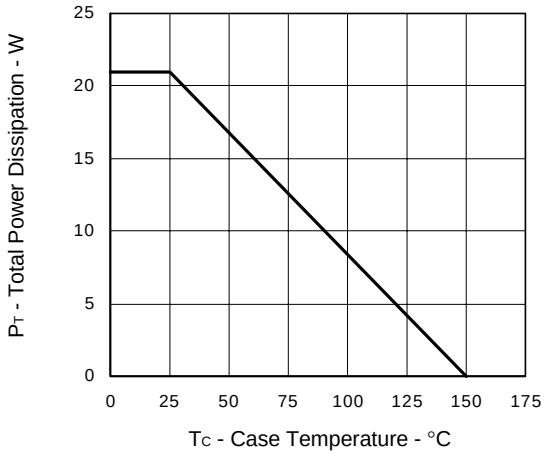


## TYPICAL CHARACTERISTICS ($T_A$ = 25°C)

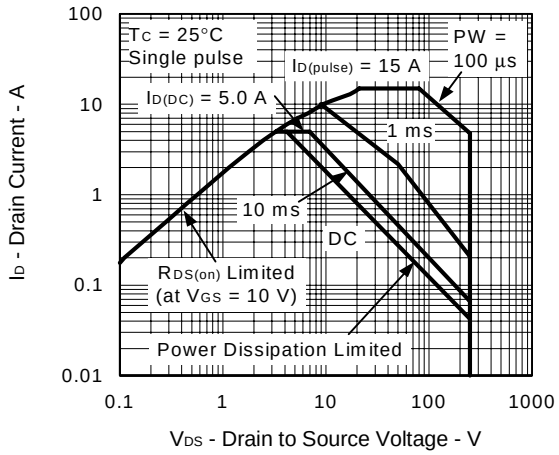
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



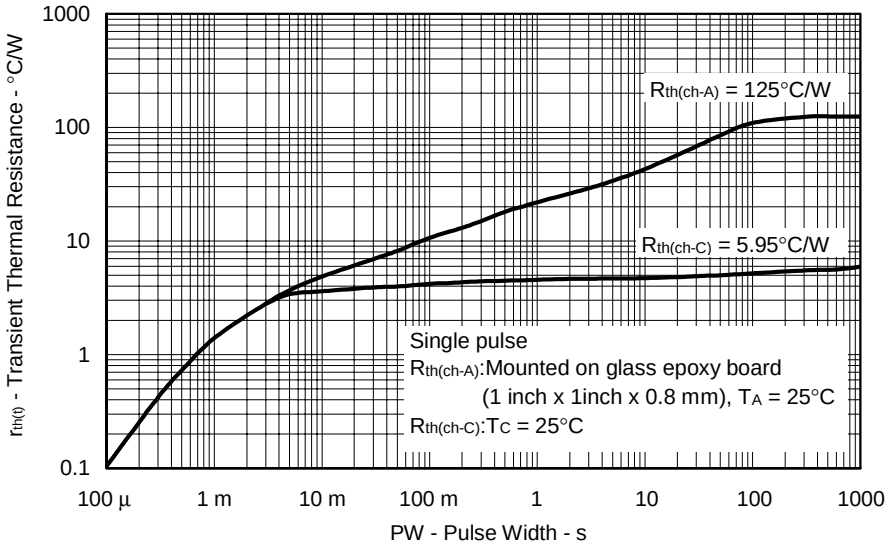

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



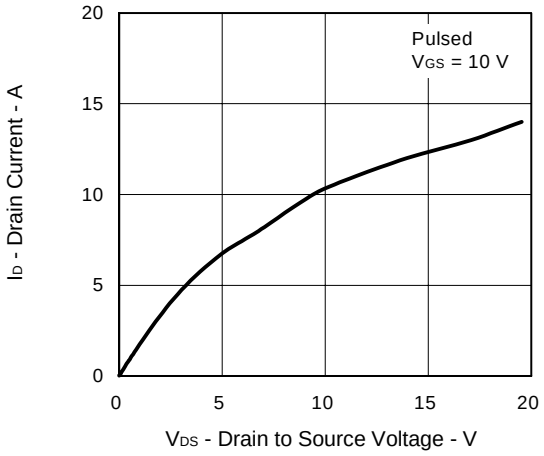

FORWARD BIAS SAFE OPERATING AREA



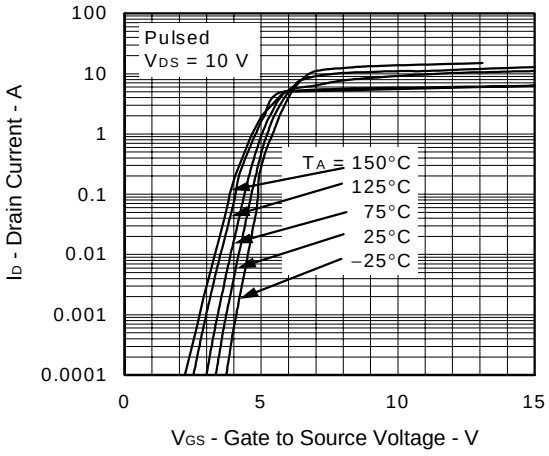

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



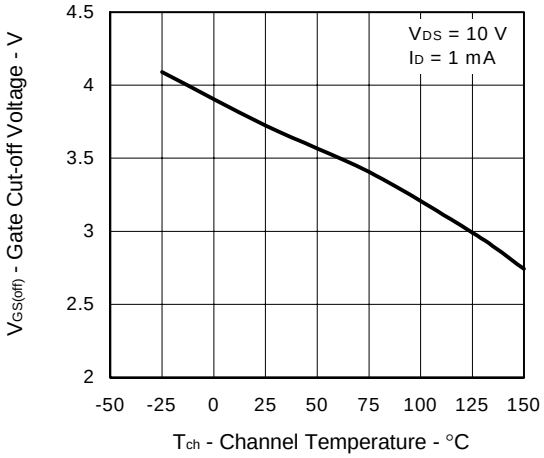
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



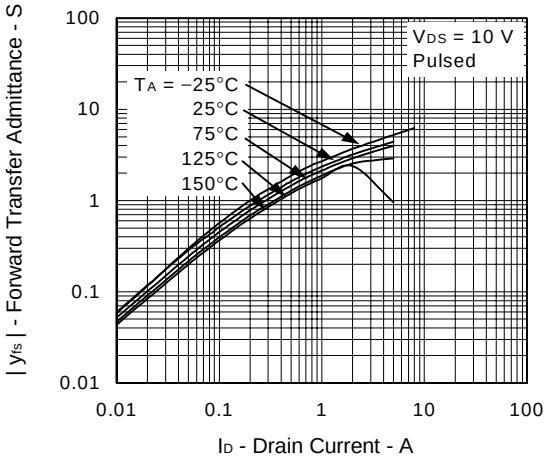

FORWARD TRANSFER CHARACTERISTICS



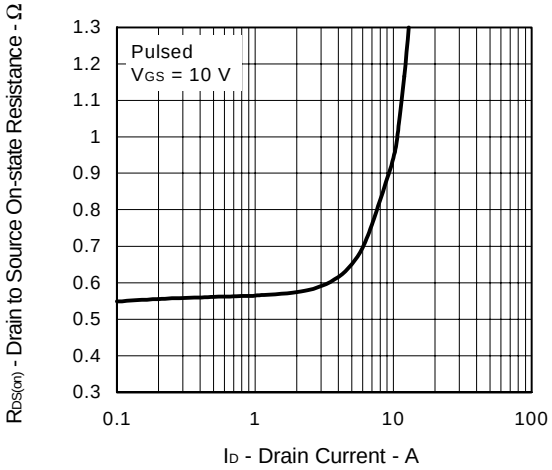

GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



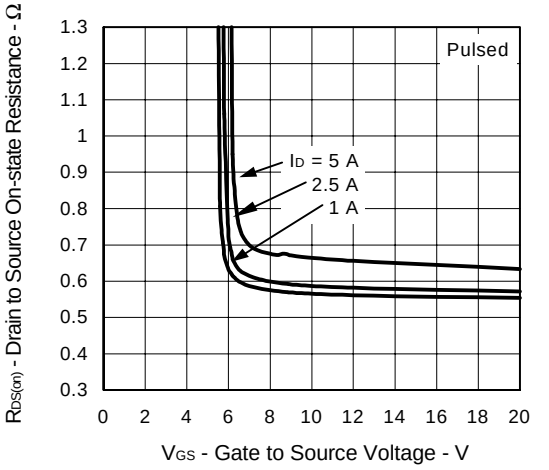

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



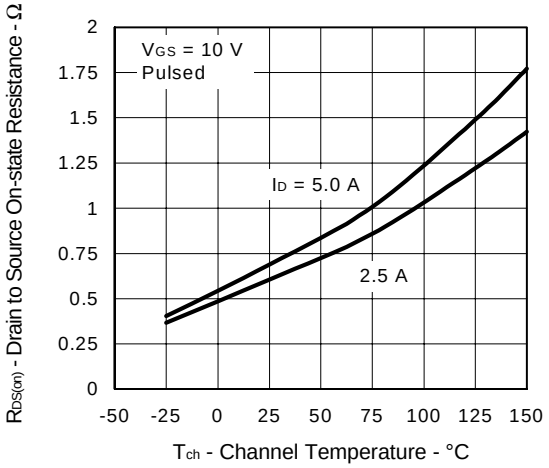

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



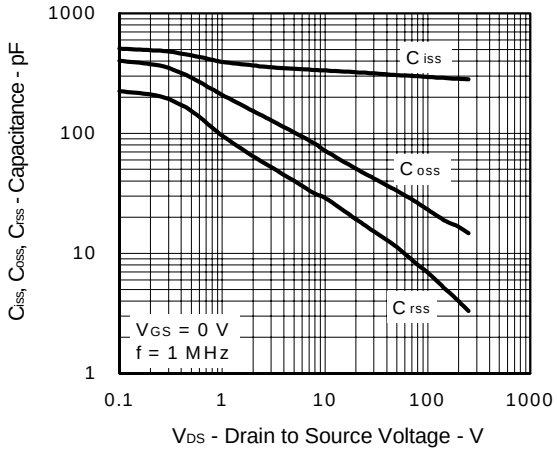

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



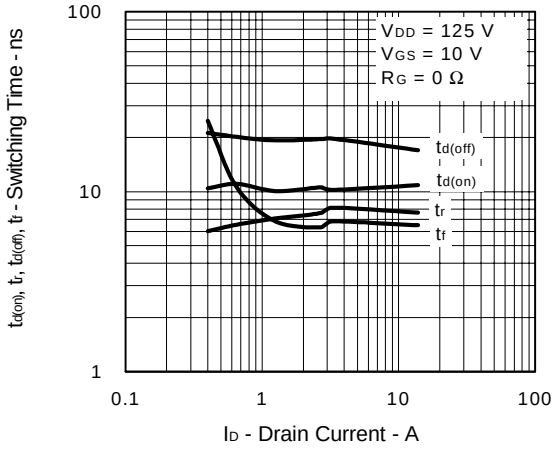
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



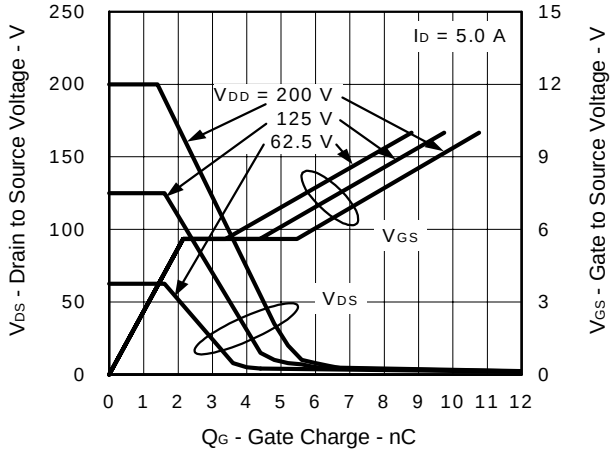

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



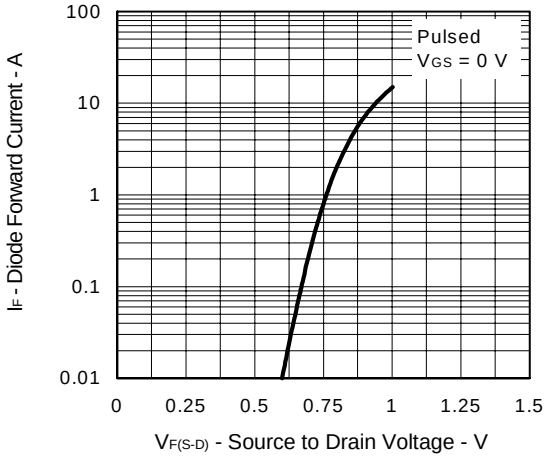

SWITCHING CHARACTERISTICS



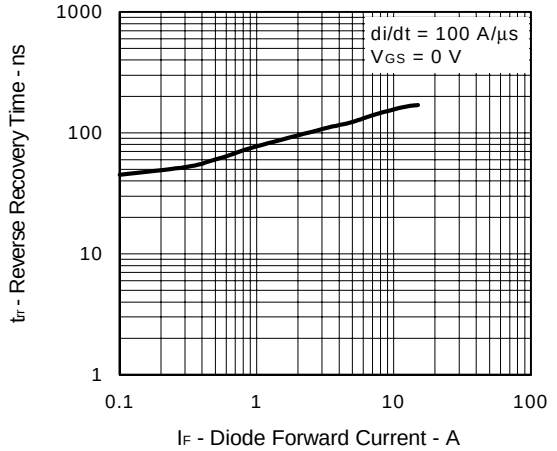

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



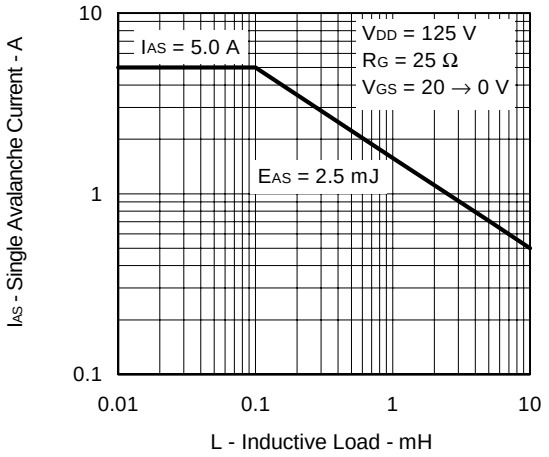

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



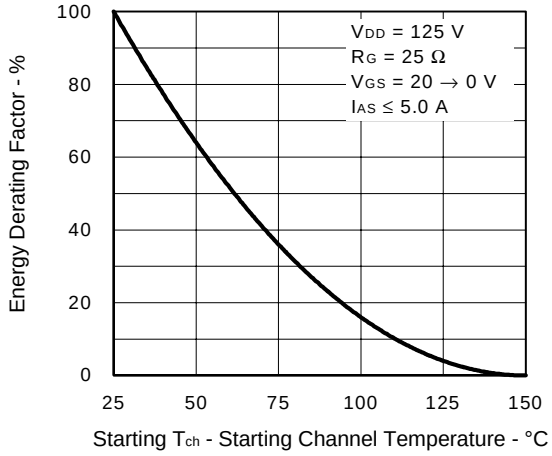

REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD




SINGLE AVALANCHE ENERGY
DERATING FACTOR



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