

**SWITCHING
N-CHANNEL POWER MOS FET**

DESCRIPTION

The μ PA1744TP is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

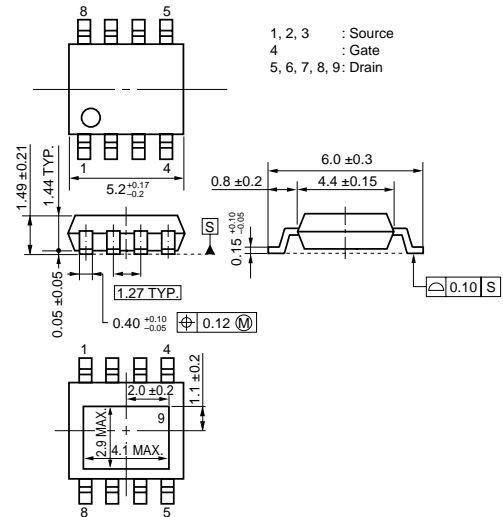
FEATURES

- Low on-state resistance
 $R_{DS(on)} = 30 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 10 \text{ V}$, $I_D = 5.0 \text{ A}$)
- Low input capacitance
 $C_{iss} = 3400 \text{ pF TYP.}$ ($V_{DS} = 10 \text{ V}$, $V_{GS} = 0 \text{ V}$)
- Built-in gate protection diode
- Small and surface mount package (Power HSOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1744TP	Power HSOP8

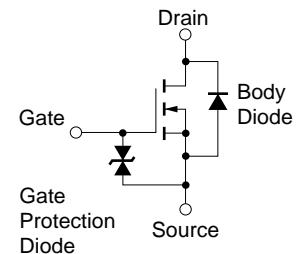
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, Unless otherwise noted, all terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	100	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 10	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 30	A
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T1}	39	W
Total Power Dissipation ($T_A = 25^\circ\text{C}$) ^{Note2}	P_{T2}	3.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	10	A
Single Avalanche Energy ^{Note3}	E_{AS}	10	mJ

EQUIVALENT CIRCUIT



Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm

3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$, $L = 100 \mu\text{H}$

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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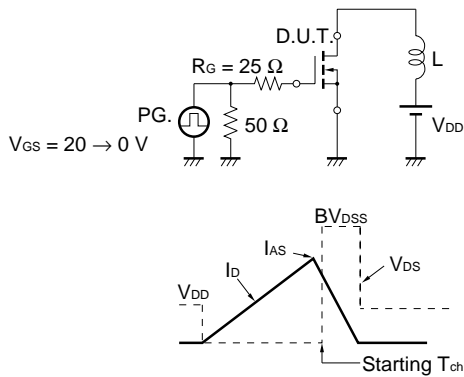
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ELECTRICAL CHARACTERISTICS (TA = 25°C, Unless otherwise noted, all terminals are connected.)

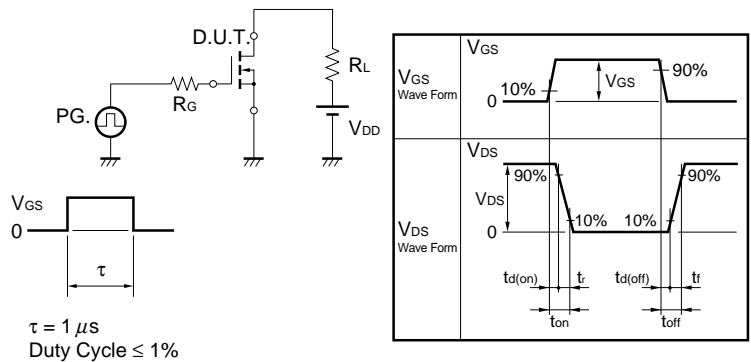
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			10	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = 10\text{ V}, I_D = 1\text{ mA}$	2.5	3.0	3.5	V
Forward Transfer Admittance ^{Note}	$ y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 5.0\text{ A}$	7	14		S
Drain to Source On-state Resistance ^{Note}	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5.0\text{ A}$		23	30	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V}$		3400		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$		390		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		200		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 5.0\text{ A}$		22		ns
Rise Time	t_r	$V_{GS} = 10\text{ V}$		10		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 10\ \Omega$		55		ns
Fall Time	t_f			7		ns
Total Gate Charge	Q_G	$V_{DD} = 80\text{ V}$		66		nC
Gate to Source Charge	Q_{GS}	$V_{GS} = 10\text{ V}$		12		nC
Gate to Drain Charge	Q_{GD}	$I_D = 10\text{ A}$		22		nC
Body Diode Forward Voltage ^{Note}	$V_{F(S-D)}$	$I_F = 10\text{ A}, V_{GS} = 0\text{ V}$		0.8		V
Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, V_{GS} = 0\text{ V}$		65		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 100\text{ A}/\mu\text{s}$		170		nC

Note Pulsed: $PW \leq 350\ \mu\text{s}$, Duty Cycle $\leq 2\%$

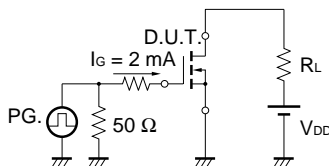
TEST CIRCUIT 1 AVALANCHE CAPABILITY



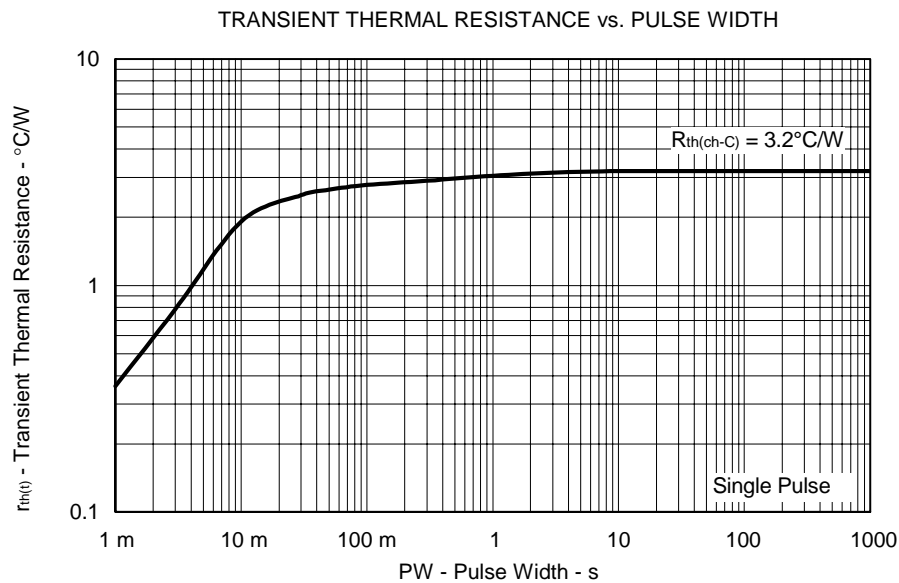
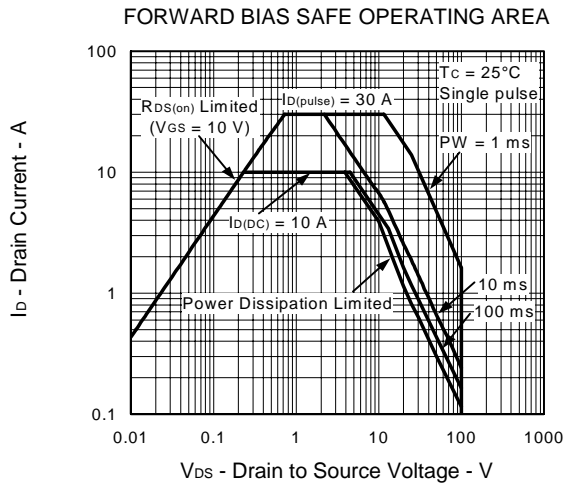
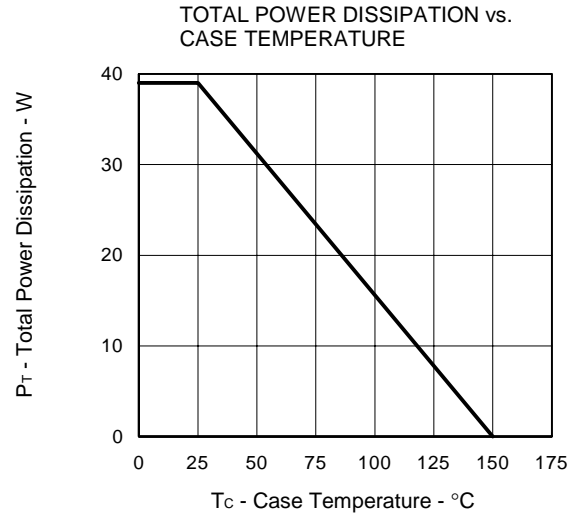
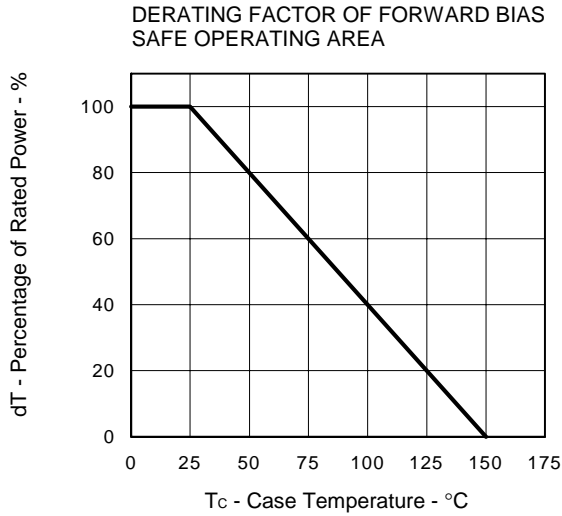
TEST CIRCUIT 2 SWITCHING TIME



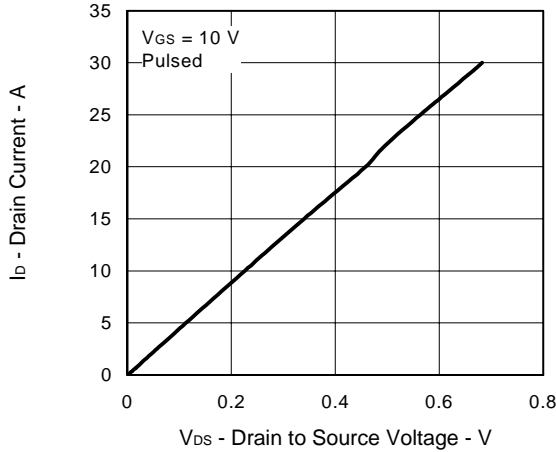
TEST CIRCUIT 3 GATE CHARGE



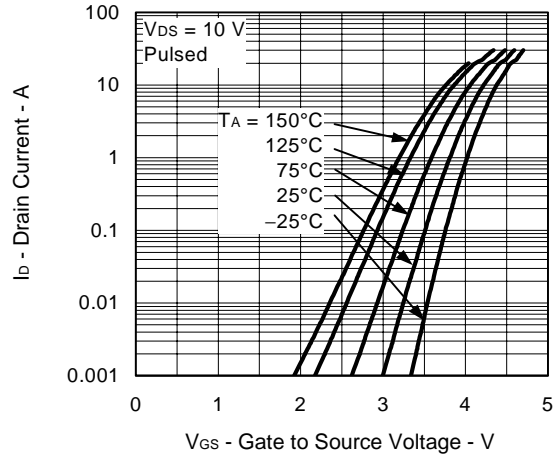
TYPICAL CHARACTERISTICS (T_A = 25°C, Unless otherwise noted, all terminals are connected.)



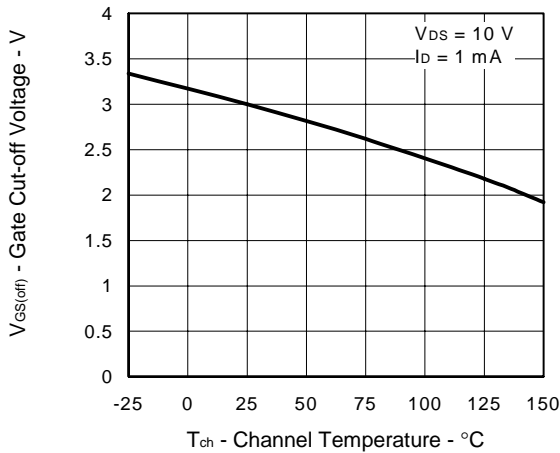
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



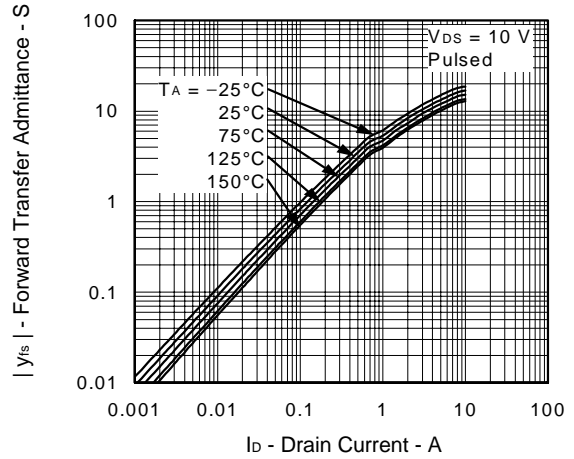
FORWARD TRANSFER CHARACTERISTICS



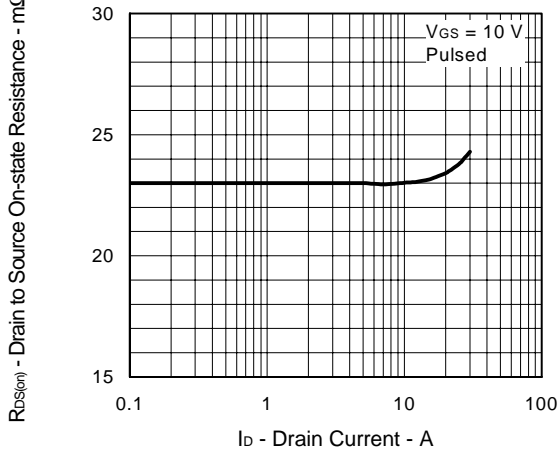
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



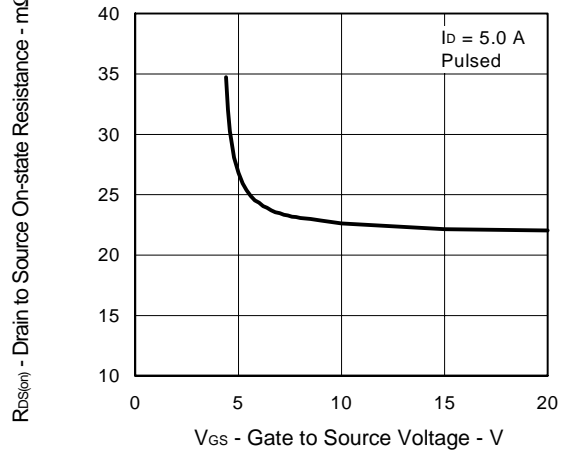
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



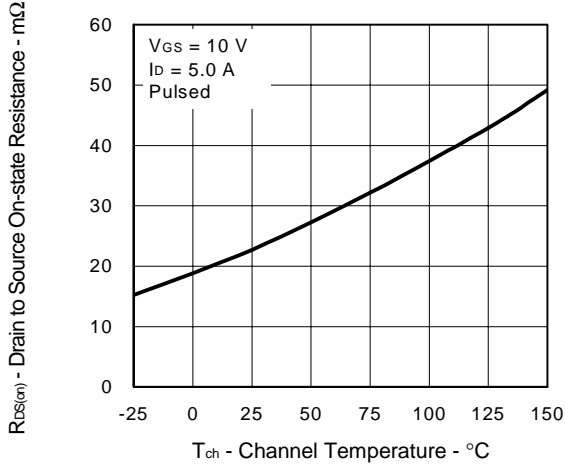
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



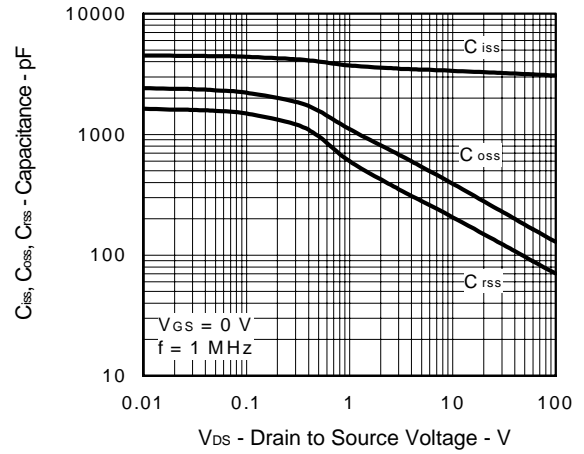
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



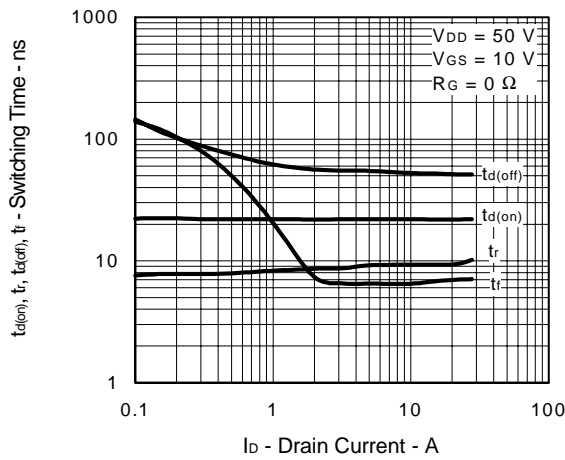
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



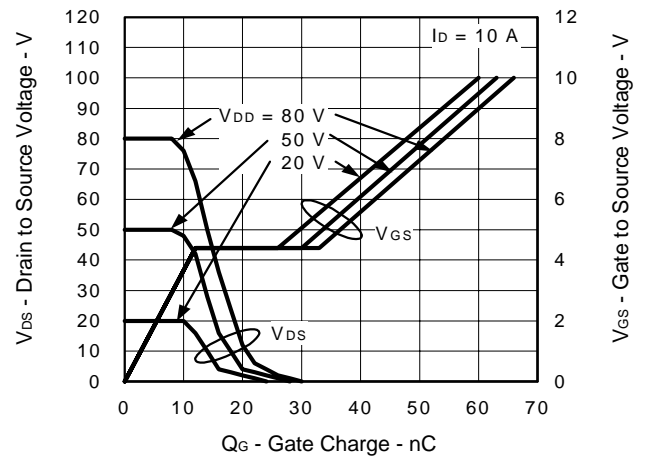
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



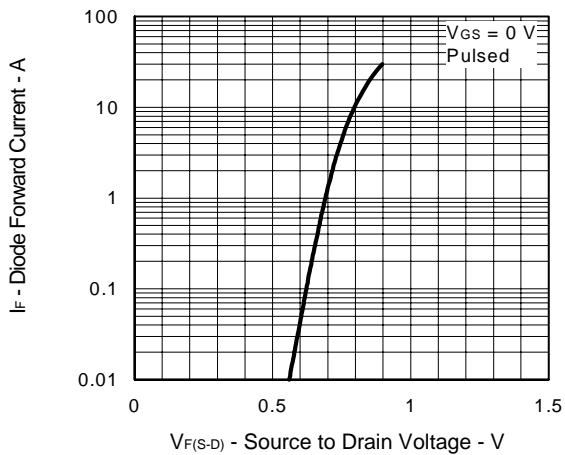
SWITCHING CHARACTERISTICS



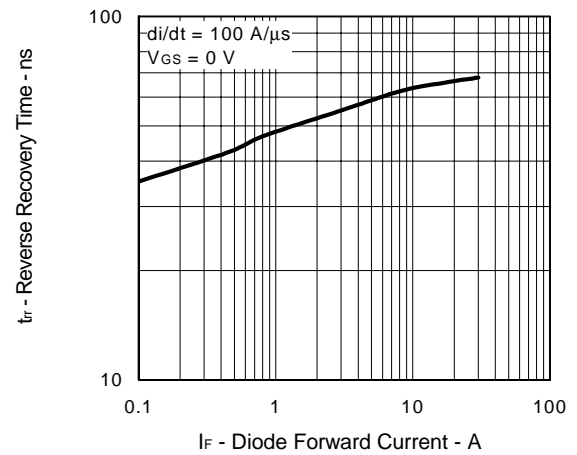
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



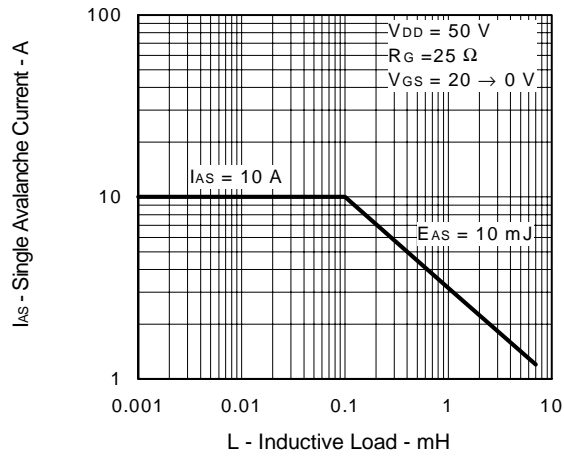
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



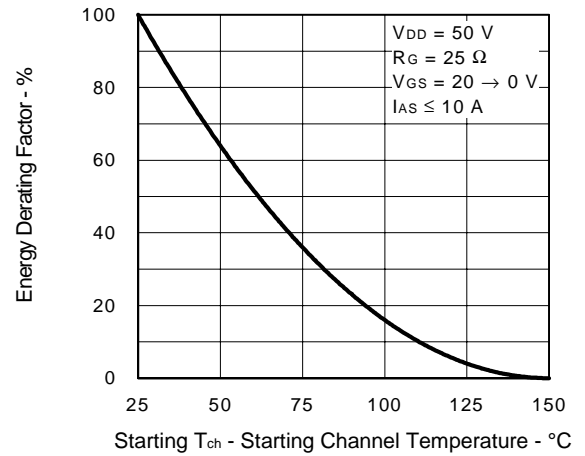
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY
DERATING FACTOR



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