

NEC

MOS FIELD EFFECT TRANSISTOR

μ PA1840

N-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μ PA1840 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1840GR-9JG	Power TSSOP8

FEATURES

- High voltage rating $V_{DS} = 200\text{ V}$
- Power TSSOP8 package (Single circuit)
- Gate voltage rating $\pm 30\text{ V}$
- Low on-state resistance
 $R_{DS(on)} = 0.5\ \Omega\text{ MAX.}$ ($V_{GS} = 10\text{ V}$, $I_D = 1.5\text{ A}$)
- Low input capacitance
 $C_{iss} = 320\text{ pF TYP.}$ ($V_{DS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$)
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0\text{ V}$)	V_{DS}	200	V
Gate to Source Voltage ($V_{DS} = 0\text{ V}$)	V_{GS}	± 30	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 2.2	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 8.8	A
Total Power Dissipation ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes 1. $PW \leq 10\ \mu\text{s}$, Duty Cycle $\leq 1\%$

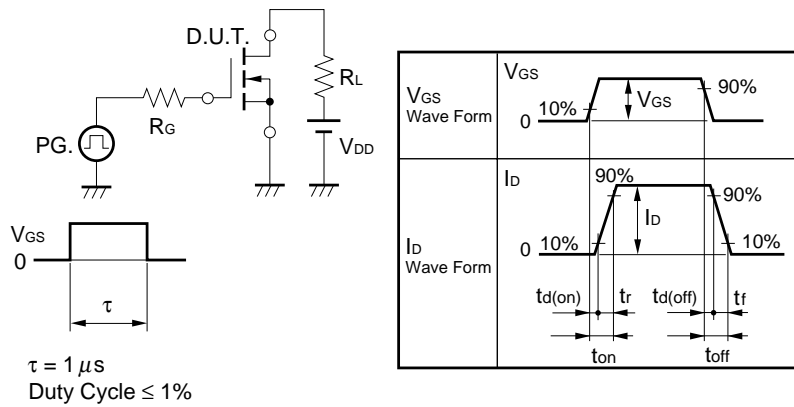
2. Mounted on ceramic substrate of $5000\text{ mm}^2 \times 1.1$

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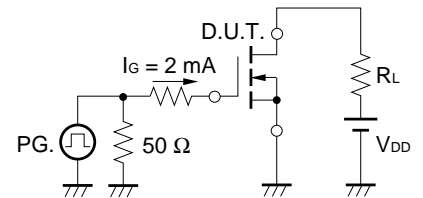
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V			100	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5		4.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 1.5 A	1.0	2.0		S
Drain to Source On-state Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 1.5 A		0.37	0.5	Ω
Input Capacitance	C _{iss}	V _{DS} = 10 V		320		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		96		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		55		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 100 V, I _D = 1.5 A		14		ns
Rise Time	t _r	V _{GS} = 10 V		13		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		30		ns
Fall Time	t _f			13		ns
Total Gate Charge	Q _G	V _{DD} = 160 V		16		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		2.3		nC
Gate to Drain Charge	Q _{GD}	I _D = 2.2 A		9.0		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 2.2 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 2.2 A, V _{GS} = 0 V		150		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 50 A/μs		0.4		μC

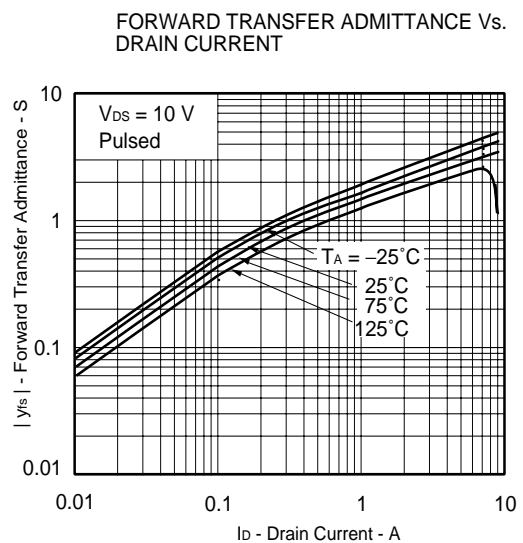
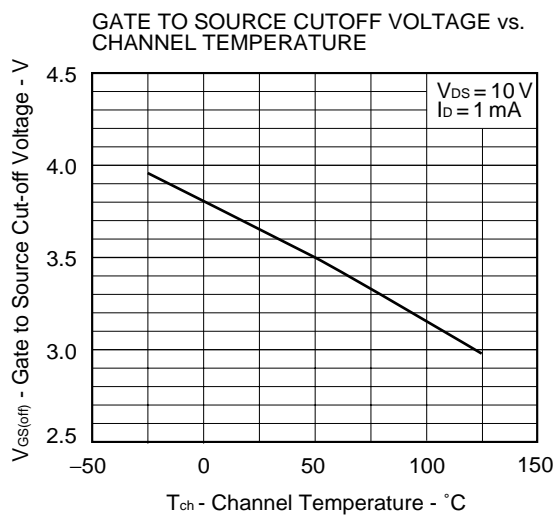
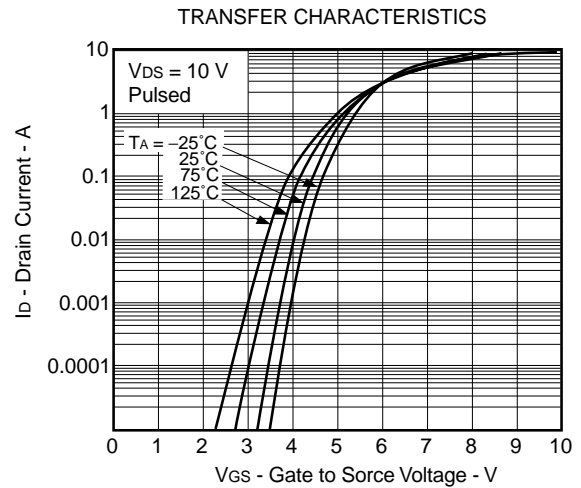
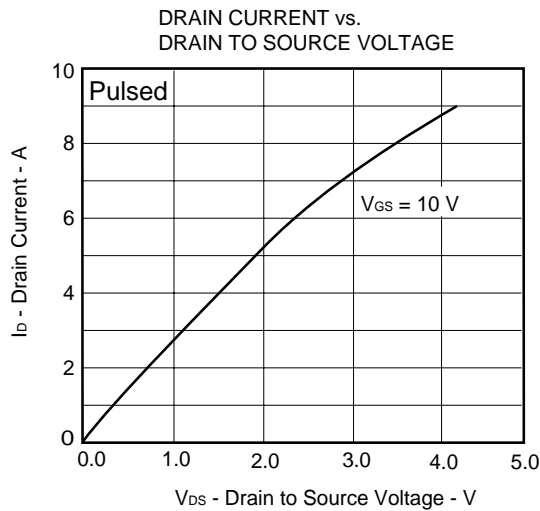
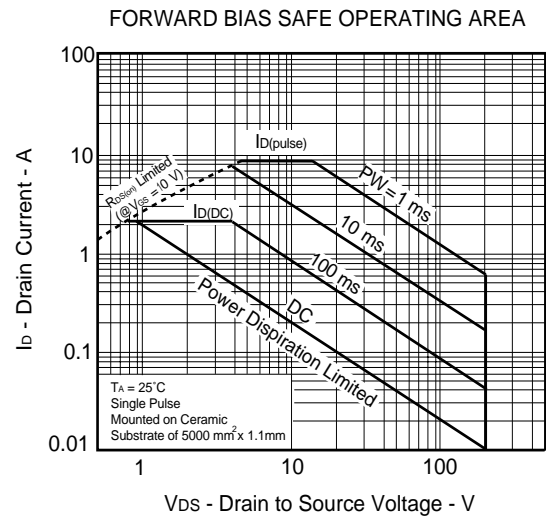
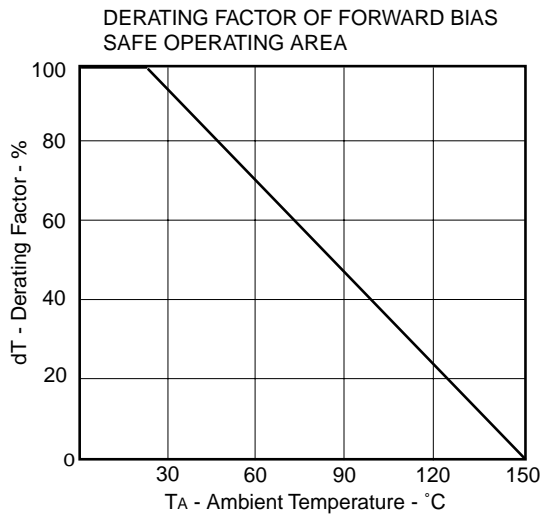
TEST CIRCUIT 1 SWITCHING TIME

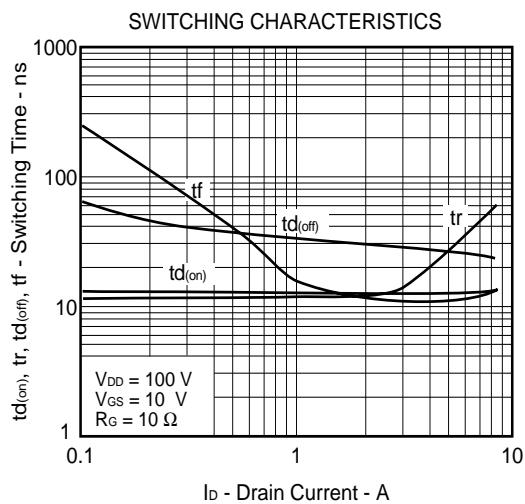
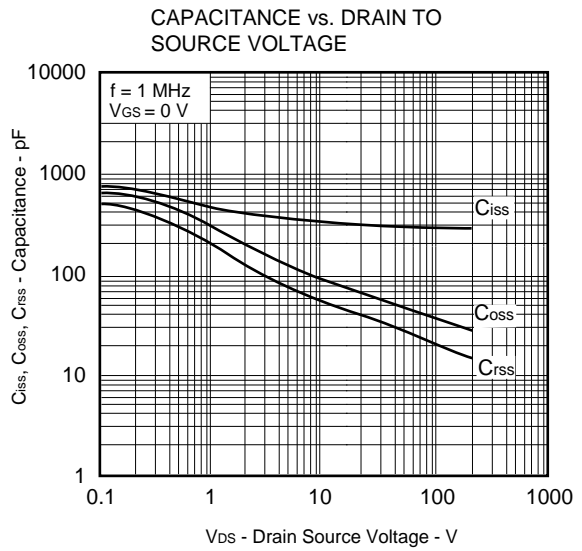
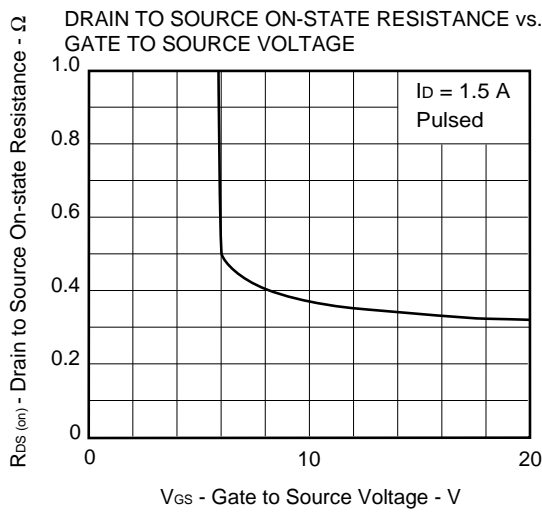
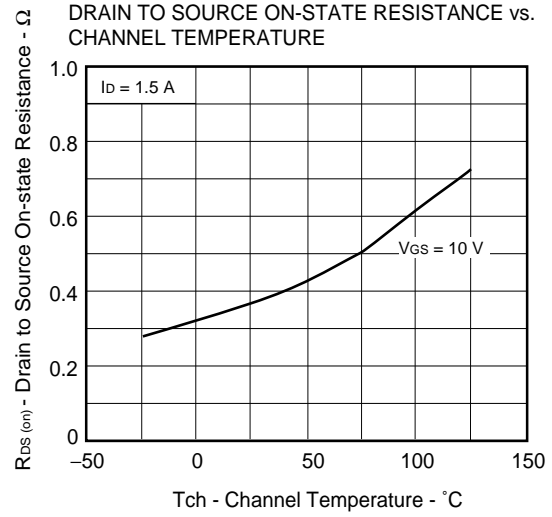
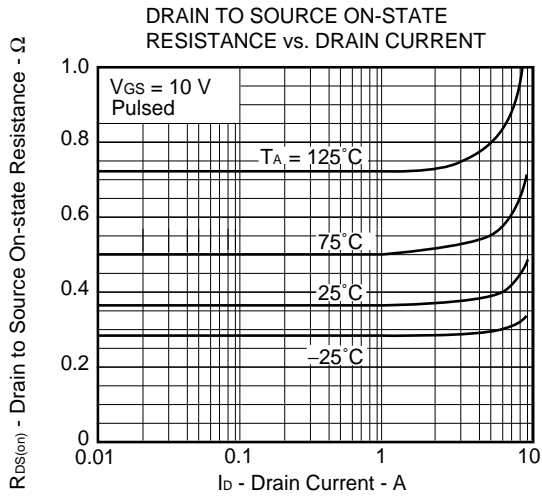


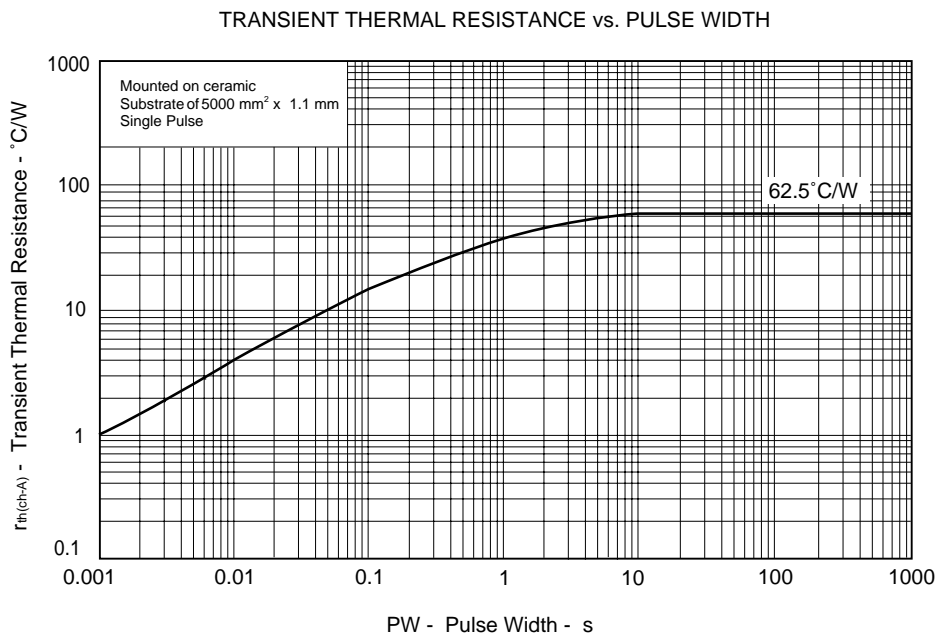
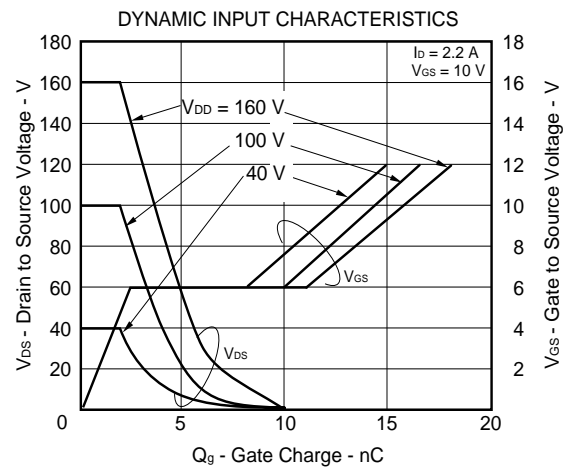
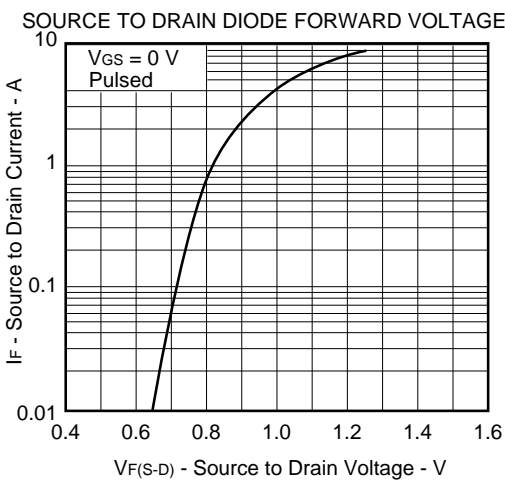
TEST CIRCUIT 2 GATE CHARGE



TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

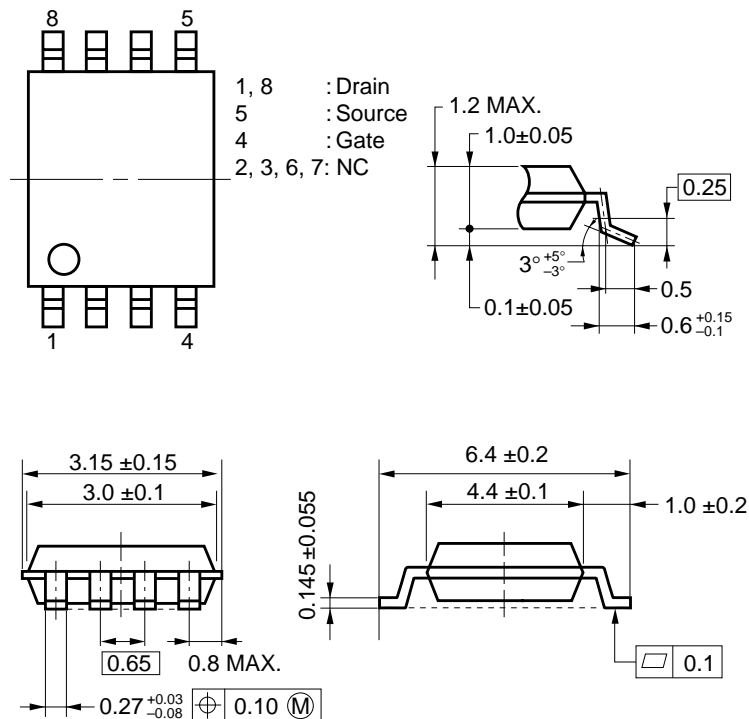






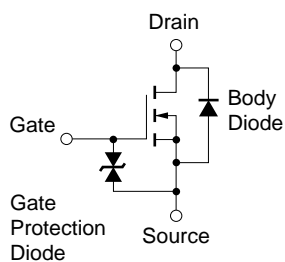
PACKAGE DRAWING (Unit: mm)

Power TSSOP8



Caution The terminal assignment is different from that of the NEC standard Power TSSOP8 package.

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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