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PRELIMINARY PRODUCT INFORMATION

NEC ELECTRON DEVICE

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1861

HORIZONTAL LOCK CLOCK GENERATOR

The μPC1861 is an LSI chip which incorporates a PLL circuit to generate clocks whose frequency is multipliable by f_H (Horizontal sync signal frequency) and is ideal for the processing of digital video signals.

Thanks to the sync separator, phase comparator, and voltage controlled oscillator (VCO) also incorporated in the LSI chip, a horizontal lock clock (synchronous with a horizontal sync signal) can be obtained by dividing the frequency of the generated clock with an external frequency divider. In addition, the μPC1861 adopts a 16-pin small outline package (SOP) and thus saves mounting space on a PC board.

FEATURES

- VCO is incorporated (may be used up to 1 820 f_H 27.6 MHz).
- Horizontal sync separator is incorporated.
- Low current consumption (approx. 55 mW typ.)

ORDERING INFORMATION

PART NUMBER	PACKAGE	QUALITY GRADE
μPC1861GR	16-pin plastic SOP (225 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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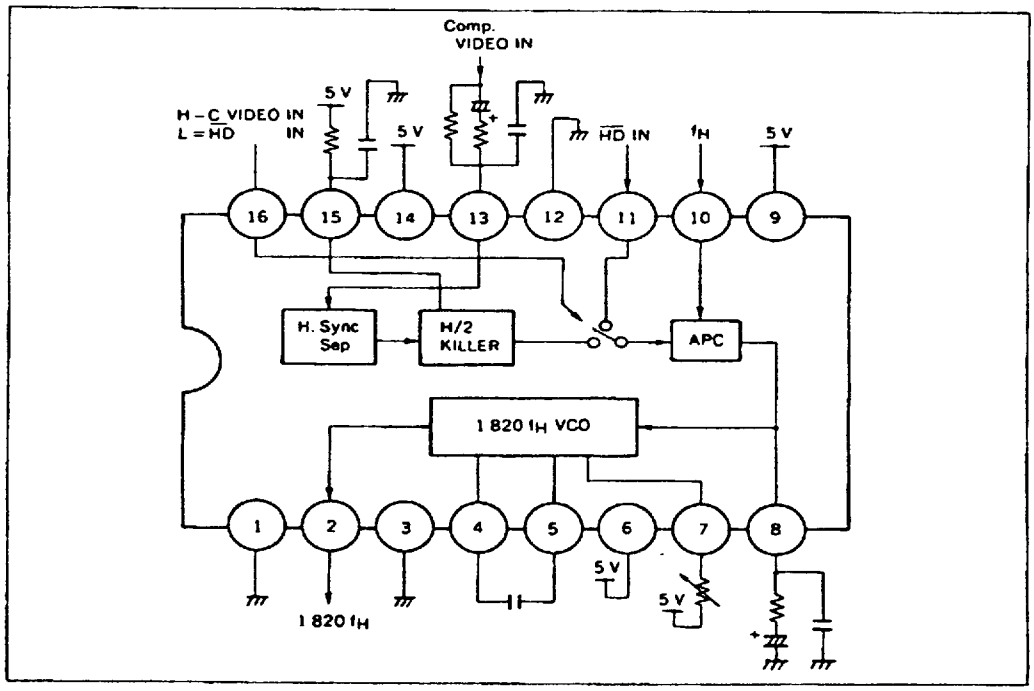
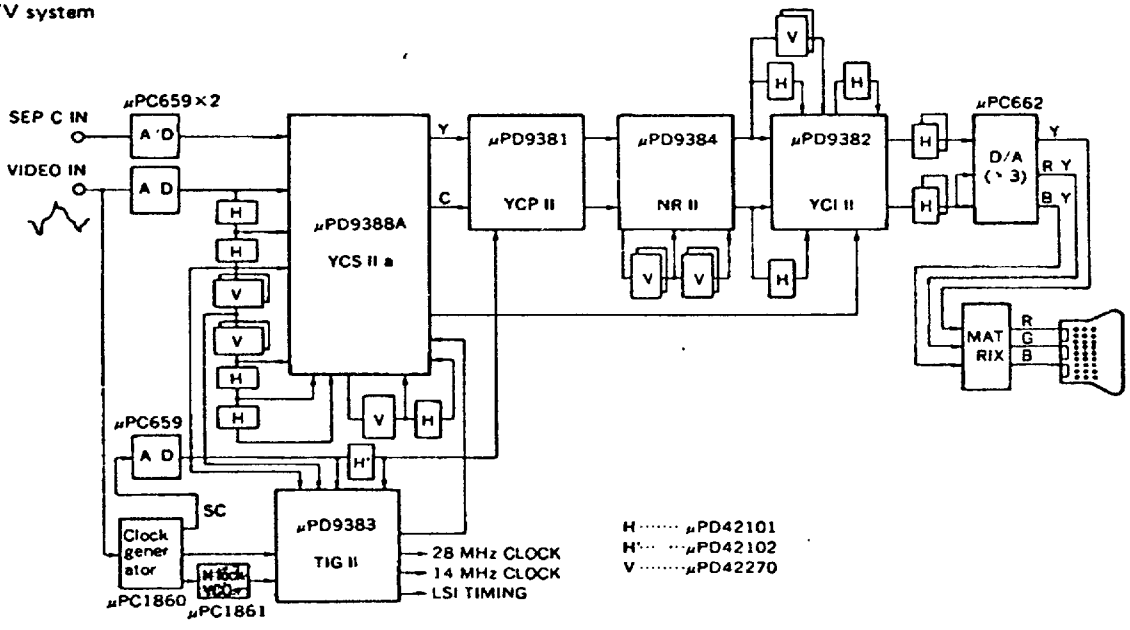
BLOCK DIAGRAM

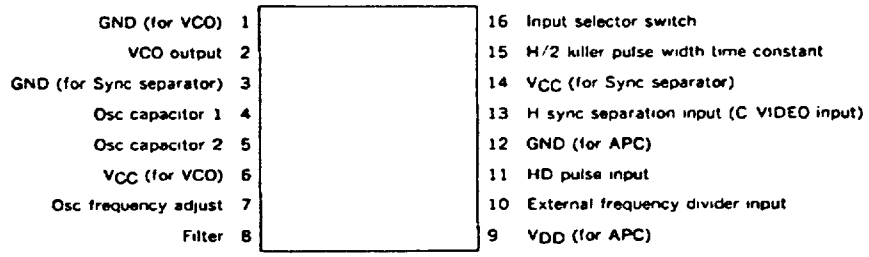


Block Diagram of System to which μPC1861 Is Applied.

(1) EDTV system



PIN ASSIGNMENTS (Top View)



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply Voltage	V_{CC}	Applicable to Power Supply pins 6 & 14	7	V
Supply Voltage	V_{DD}	Applicable to Power Supply pin 9	7	V
Composite Video Input Signal Voltage	ei2		3	V_{p-p}
Input Voltage	ei	Applicable to Input pins 10 & 11 (CMOS input)	−0.5 to V_{DD} +0.5	V
Input Select Voltage	V16	Applicable to Input pin 16 (CMOS input)	−0.5 to V_{DD} +0.5	V
Power Dissipation of Package	P_D	T_a = 75 °C	275	mW
Operating Temperature	T_{opt}		−10 to +75	°C
Storage Temperature	T_{stg}		−40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (T_{opt} = −10 to +75 °C)

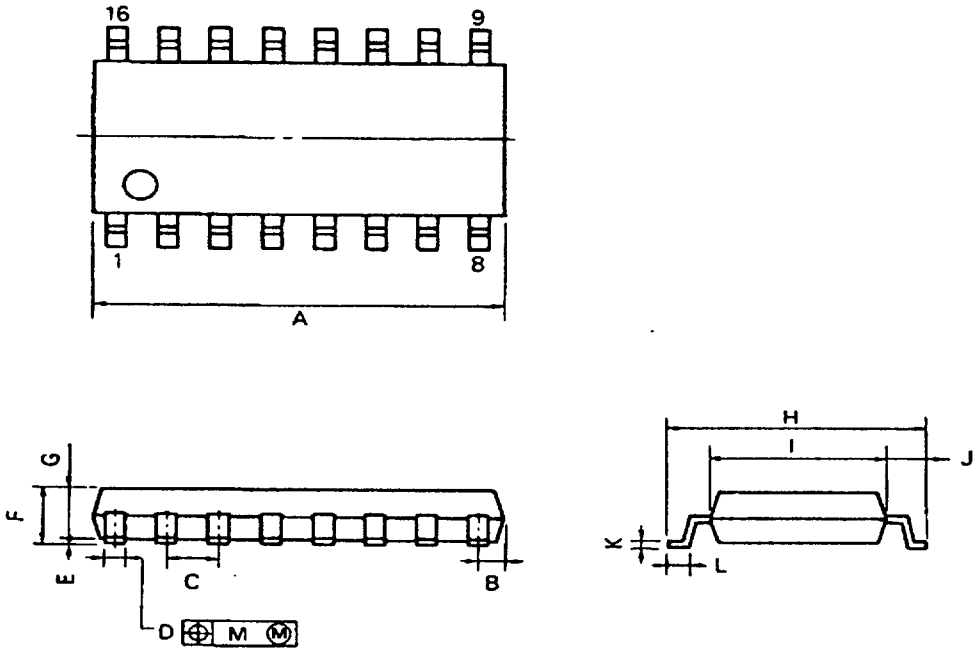
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage 1	V_{CC}	4.5	5.0	5.5	V	Applicable to Power Supply pins 6 & 14
Supply Voltage 2	V_{DD}	4.5	5.0	5.5	V	Applicable to Power Supply pin 9
Composite Video Input Signal	ei2		1.0		V_{p-p}	
Input Voltage, Low	eiL	0		0.3 V_{DD}	V	Applicable to Input pins 10 & 11 (CMOS input)
Input Voltage, High	eiH	0.7 V_{DD}		V_{DD}	V	
Input Select Voltage, Low	V16L	0		0.3 V_{DD}	V	Applicable to Input pin 11 (CMOS input)
Input Select Voltage, High	V_{16H}	0.7 V_{DD}		V_{DD}	V	Applicable to Input pin 13 (CMOS input)

AC/DC CHARACTERISTICS (T_a = 25 ± 2 °C, RH ≦ 70 %, V_{CC} = 5.0 V, V_{DD} = 5.0 V)

No.	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
1	Current Consumption 1	I_{CC1}		9.5		mA	Circuit current when no signal is input (including I_{DD}. Pins 11, 16 = "L"; Pin 13: Open; Pin 7 = 200 μA)
2	Current Consumption 2	I_{CC2}		10.7		mA	Circuit current when PLL is locked (including I_{DD}. Pins 11, 16 = "L"; Pin 13: C. Video; Pin 7 = 200 μA)
3	DC Level of H Sync Separation Level	V_{SSH}	1.9	2.2	2.5	V	Voltage of Pin No. 13 when connected to GND via 10 kΩ resistor
4	Minimum Sync Separation Level	V_{SEP}	60			mW	Critical sync level at which output to Pin 15 is no longer produced when sync level of C. VIDEO is lowered
5	H Sync Lock-in Range	f_{HP}		±1.75		kHz	Frequency range that can be pulled in by APC when HD input frequency is varied (f_H conversion)
6	VCO Control Sensitivity High level (1)	β		0.7		Hz/mV	Rate of variation of frequency with no signal being input to Pin 13, with Pins 10, 11, & 16 set to "H" or "L", and with 0 to 5 V being applied to Pin 8 (f_H conversion)
7	Free-run Frequency (Without Adjustment)	f_O		0		Hz	Frequency difference of VCO output from 1 820 f_H with no signal being input to Pin 13, with Pins 10, 11, & 16 set to "H" or "L", and with Pin 8 left open
8	Free-run Frequency Adjustable Range	f_{OC}		±1.5		MHz	Adjustable free-run frequency range with no signal being input to Pin 13, with Pins 10, 11, & 16 set to "H" or "L", and with Pin 8 left open
9	VCO Output Level	eVCO		1		V_{p-p}	Output level of VCO with no signal being input to Pin 13, with Pins 10, 11 & 16 set to "H" or "L", and with Pin 8 left open
10	Oscillation Start (Stop) Voltage of VCO	V_{ST}	2.85			V	Voltage at which VCO starts (or stops) oscillation when V_{CC} (Pin 6) is gradually increased from 0 V (or decreased from 5 V) with no signal being input to Pin 13, with Pins 10, 11, & 16 set to "H" or "L", and with Pin 8 left open
11	Fluctuation of Free-run Frequency Due to Supply Voltage Fluctuations	Δ_{fO} (V_{CC})		0		Hz/V	Fluctuation of free-run frequency at V_{CC} (Pin 6) = 4.5 to 5.5 V (under the same pin conditions as fo)
12	Fluctuation of VCO Output Level Due to Supply Voltage Fluctuations	Δ_{eVCO} (V_{CC})		0.5		V_{p-p}/V	Fluctuation of VCO output level at V_{CC} (Pin 6) = 4.5 to 5.5 V (under the same pin conditions as fo)

No.	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
13	Fluctuation of Free-run Frequency Due to Temperature Fluctuations	$\Delta f_{o(T)}$		6.5		Hz/°C	Fluctuation of free-run frequency at T_a = −10 °C to +60 °C (under the same pin conditions as fo)
14	Fluctuation of VCO Output Level Due to Temperature Fluctuations	$\Delta_{e}VCO$ (T)				V_{p-p}/°C	Fluctuation of VCO output level at T_a = −10 °C to +60 °C (under the same pin conditions as fo)
15	Residual Jitter	T_J			5	ns	Distortion width of output waveform when PLL is locked
16	Output Delay Time 1 (to C. VIDEO)	T_{d1}				ns	Amount of delay in VCO output from H. SYNC of C. VIDEO when PLL is locked at C. VIDEO input
17	Output Delay Time 2 (to HD)	T_{d2}				ns	Amount of delay in VCO output from HD when PLL is locked at HD input

16PIN PLASTIC SOP (225 mil)



S16GM-50-225B,C-1

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	1.8 MAX.	0.071 MAX.
G	1.49	0.059
H	6.5 ± 0.3	0.256 ± 0.012
I	4.4	0.173
J	1.1	0.043
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.6 ± 0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.