

BIPOLAR ANALOG INTEGRATED CIRCUIT

μ PC2715T

1.2 GHz LOW POWER CONSUMPTION WIDE BAND AMPLIFIER SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

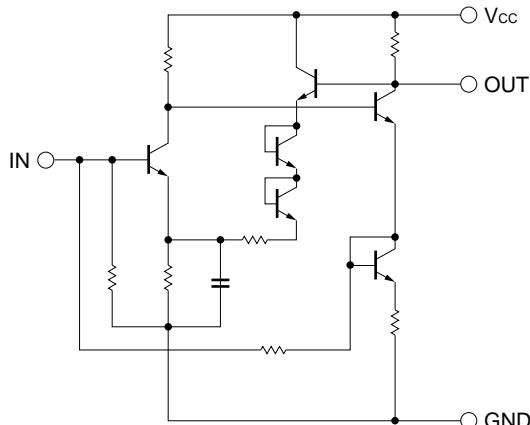
FEATURES

- Low power consumption : 15 mW ($V_{cc} = 3.4$ V, $I_{cc} = 4.5$ mA) TYP.
- High power gain : 19 dB TYP. @ $f = 0.5$ GHz
- Excellent frequency response: 1.2 GHz TYP. @ 3 dB down below the gain at 0.1 GHz
- Input and output matching : 50 Ω
- Super small package : 6 pin mini mold

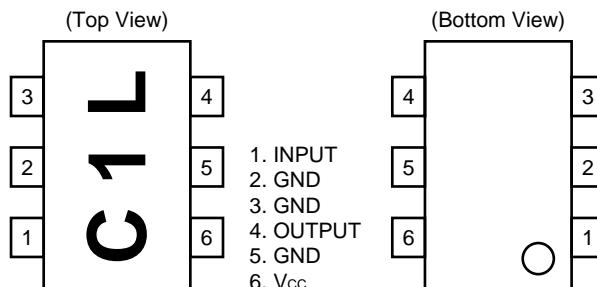
ORDERING INFORMATION

PART NUMBER	PACKAGE	SUPPLYING FORM
μ PC2715T-E3	6 pin mini mold	Embossed tape 12 mm wide. Pin 1, 2, 3 face to perforation side of the tape.

EQUIVALENT CIRCUIT



PIN CONNECTIONS



Caution: Electro-static sensitive devices

ABSOLUTE MAXIMUM RATINGS (T_A = +25 °C)

Supply Voltage	V _{cc}	4.1	V
Total Circuit Current	I _{cc}	7.5	mA
Power Dissipation	P _D	280*	mW
Operating Temperature	T _{opt}	-40 to +85	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Input Power	P _{in}	0	dBm

* Mounted on 50 × 50 × 1.6 mm epoxy glass PWD (T_A = +85 °C)

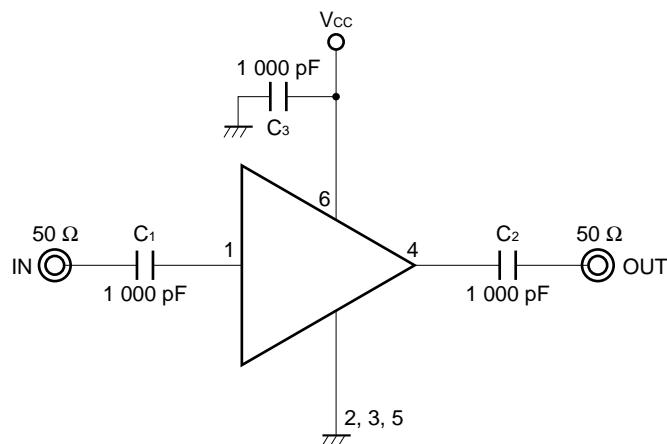
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{cc}	3.06	3.4	3.74	V

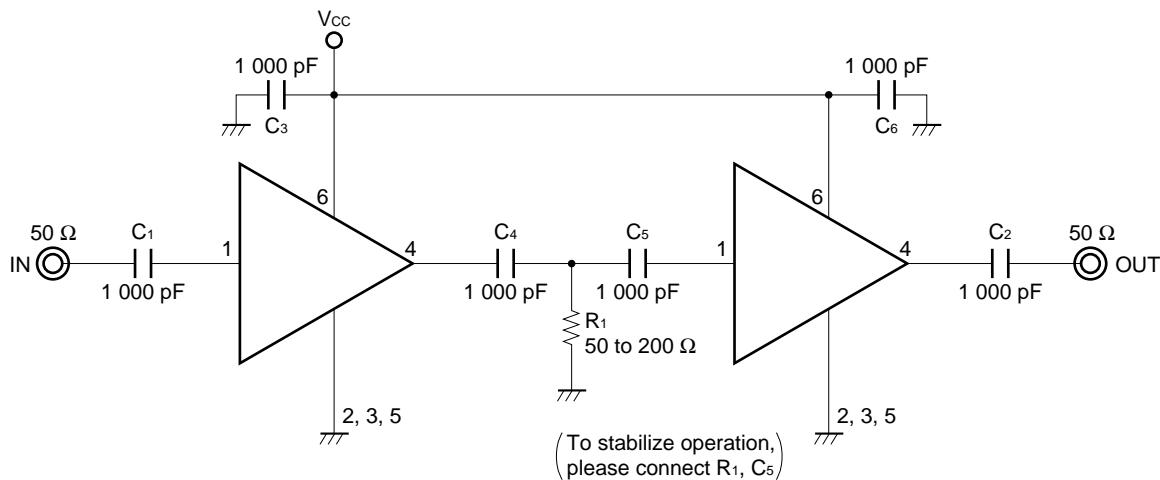
ELECTRICAL CHARACTERISTICS (T_A = +25 °C, V_{cc} = 3.4 V, Z_S = Z_L = 50 Ω)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Circuit Current	I _{cc}	3.3	4.5	5.7	mA	No Signal
Power Gain	G _P	16	19	23	dB	f = 0.5 GHz
Maximum Output Level	P _{O(sat)}	-9	-6		dBm	f = 0.5 GHz, P _{in} = -10 dBm
Noise Figure	NF		4.5	6.0	dB	f = 0.5 GHz
Upper Limit Operating Frequency	f _u	0.9	1.2		GHz	3 dB down below flat gain f = 0.1 GHz
Isolation	ISL	28	33		dB	f = 0.5 GHz
Input Return Loss	RL _{in}	12	17		dB	f = 0.5 GHz
Output Return Loss	RL _{out}	5	8		dB	f = 0.5 GHz
Gain Flatness	ΔG _P		±1.0		dB	f = 0.1 to 0.6 GHz

TEST CIRCUIT



EXAMPLE OF APPLICATION CIRCUIT



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

Capacitors for Vcc, input and output pins

1 000 pF capacitors are recommendable as bypass capacitor for Vcc pin and coupling capacitors for input/output pins.

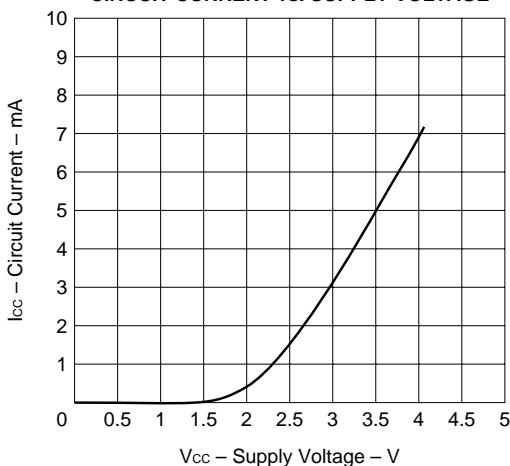
Bypass capacitor for Vcc pin is intended to minimize Vcc pin's ground impedance. Therefore, stable bias can be supplied against Vcc fluctuation.

Coupling capacitors for input/output pins are intended to minimize RF serial impedance and cut DC.

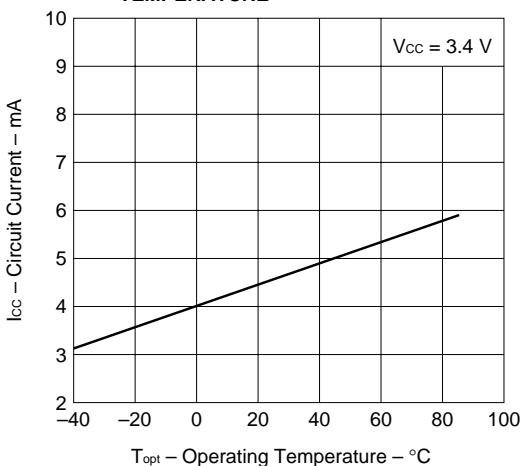
To get flat gain from 100 MHz up, 1 000 pF capacitors are assembled on the test circuit. [Actually, 1 000 pF capacitors give flat gain at least 10 MHz. In the case of under 10 MHz operation, increase the value of coupling capacitor such as 2 200 pF. Because the coupling capacitors are determined by the equation of $C = 1/(2 \pi f Z_s)$.]

TYPICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$)

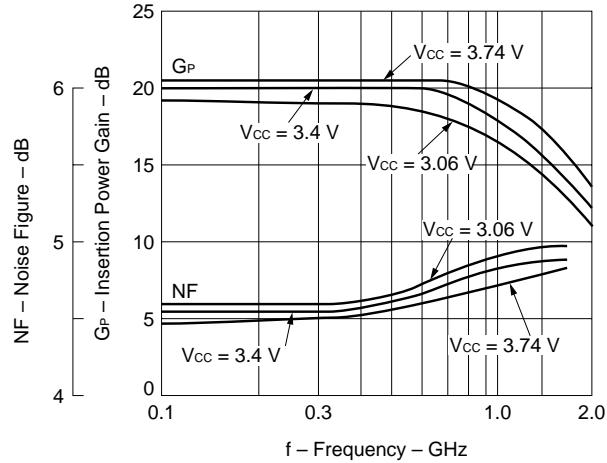
CIRCUIT CURRENT vs. SUPPLY VOLTAGE



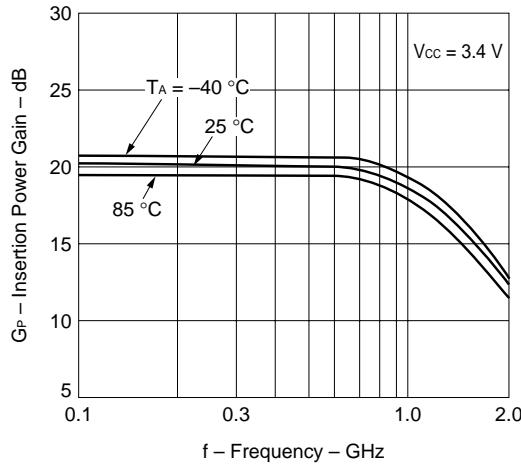
CIRCUIT CURRENT vs. OPERATING TEMPERATURE



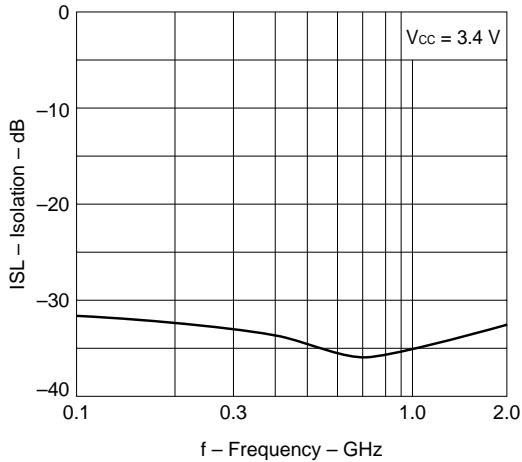
NOISE FIGURE AND INSERTION POWER GAIN vs. FREQUENCY



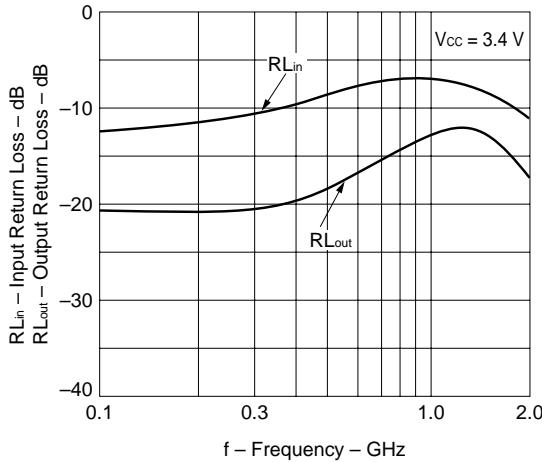
INSERTION POWER GAIN vs. FREQUENCY



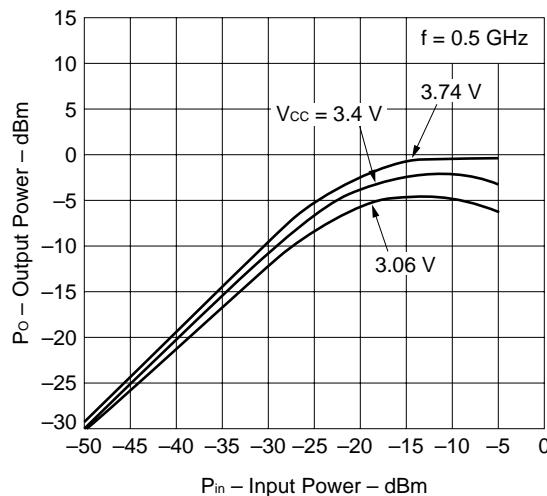
ISOLATION vs. FREQUENCY



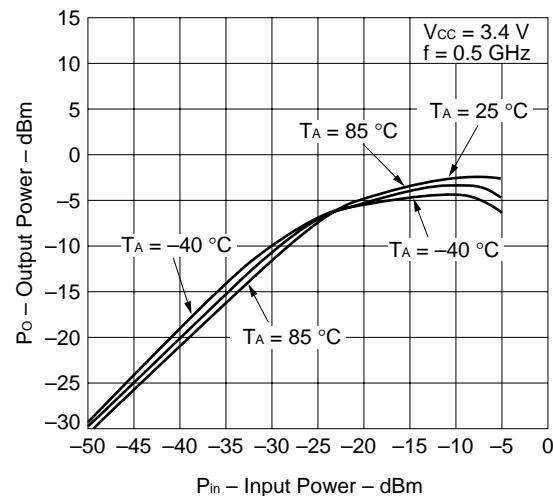
INPUT RETURN LOSS, OUTPUT RETURN LOSS vs. FREQUENCY



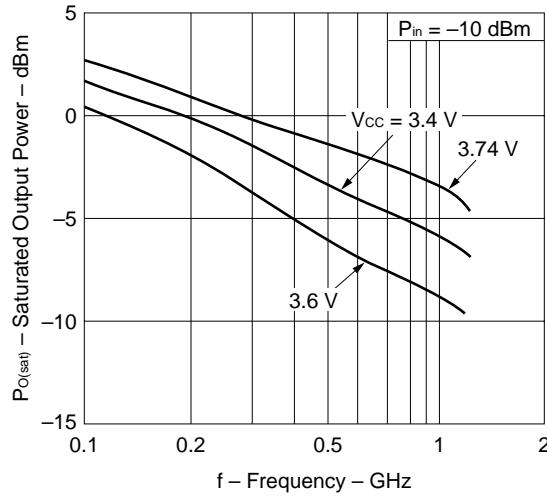
OUTPUT POWER vs. INPUT POWER



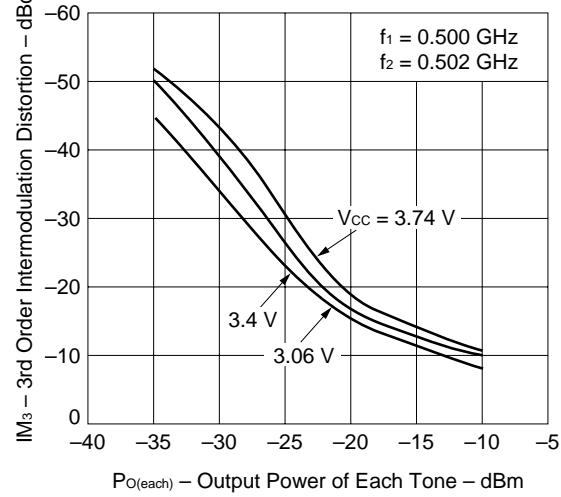
OUTPUT POWER vs. INPUT POWER

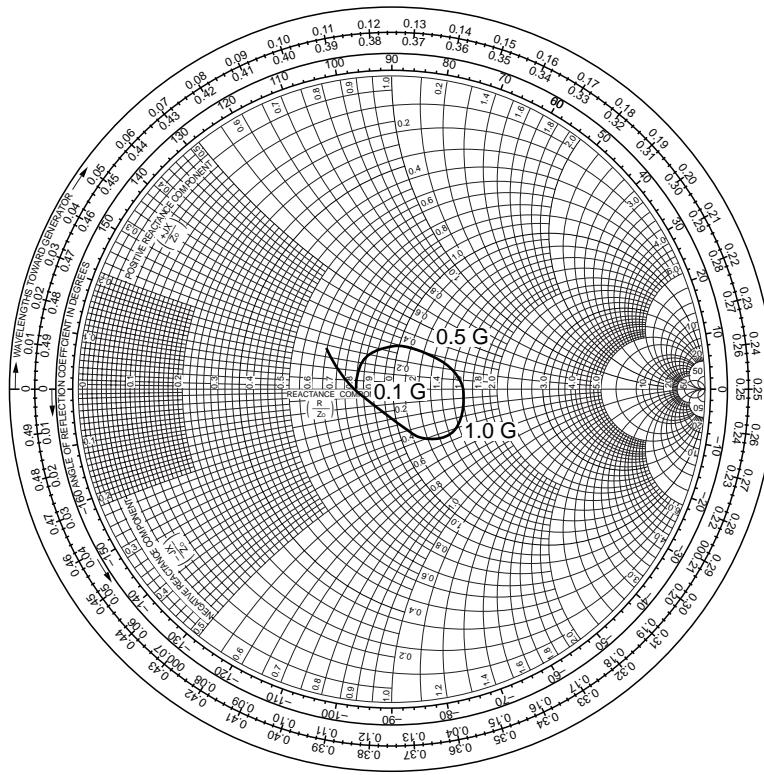
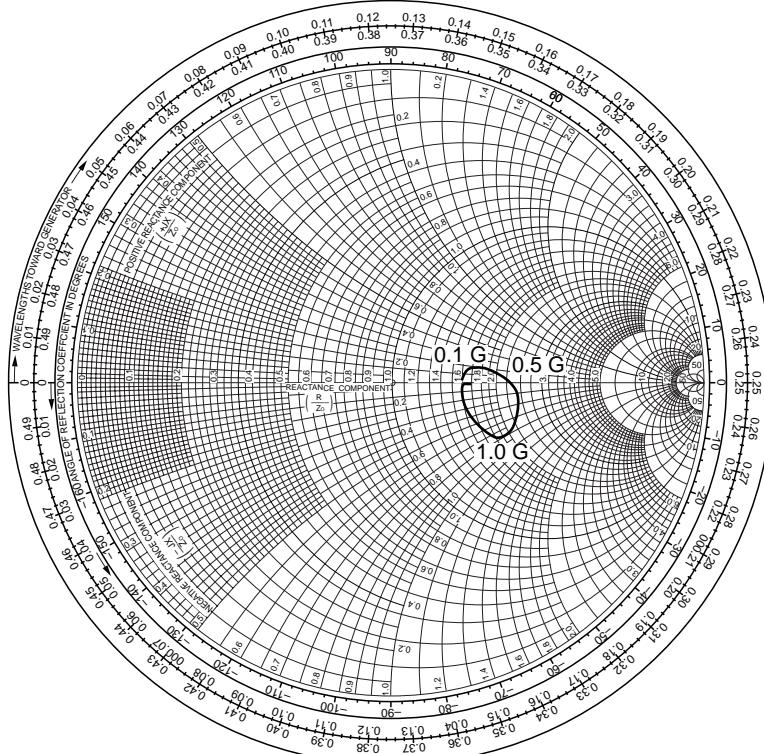


SATURATED OUTPUT POWER vs. FREQUENCY

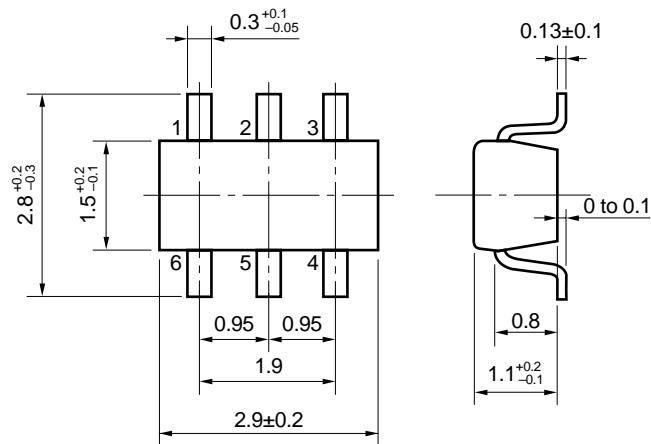


THIRD ORDER INTERMODULATION DISTORTION vs. OUTPUT POWER OF EACH TONE



S PARAMETER**S₁₁-FREQUENCY****S₂₂-FREQUENCY**

6 PINS MINI MOLD PACKAGE DIMENSIONS (Unit: mm)



NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to prevent an increase in ground impedance (which can cause abnormal oscillation).
- (3) Keep the track length of the ground pins as short as possible.
- (4) Connect a bypass capacitor (having, for example, a capacitance of 1 000 pF) to the Vcc pin.

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered in the following recommended conditions. Other soldering methods and conditions than the recommended conditions are to be consulted with our sales representatives.

μPC2715T

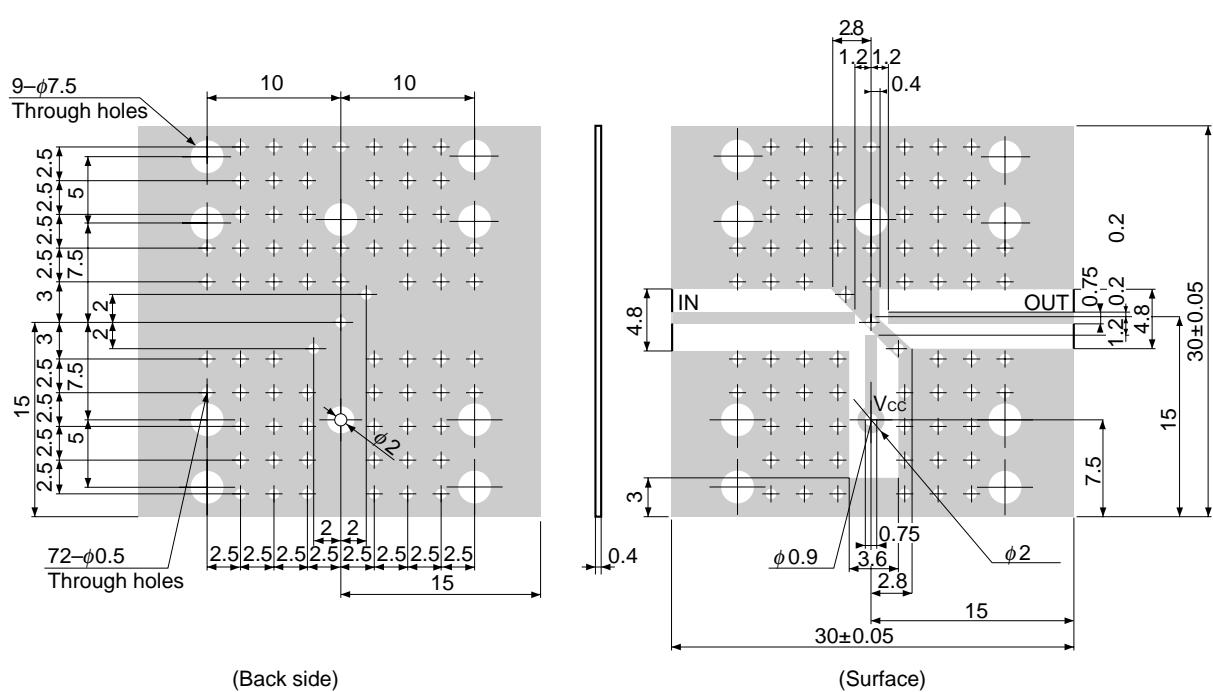
Soldering method	Soldering conditions	Recommended condition symbols
Infrared ray reflow	Package peak temperature: 235 °C, Hour: within 30 s. (more than 210 °C), Time: 3 times, Limited days: no.*	IR35-00-3
VPS	Package peak temperature: 215 °C, Hour: within 40 s. (more than 200 °C), Time: 3 times, Limited days: no.*	VP15-00-3
Wave soldering	Soldering tub temperature: less than 260 °C, Hour: within 10 s. Time: 1 time, Limited days: no.*	WS60-00-1
Pin part heating	Pin area temperature: less than 300 °C, Hour: within 3 s. Limited days: no.*	

*: It is the storage days after opening a dry pack, the storage conditions are 25 °C, less than 65 % RH.

Note 1. The combined use of soldering method is to be avoided (However, except the pin area heating method).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

Illustration of evaluation board for the test circuit



Note

- (1) 30 x 30 x 0.4 mm double sided copper clad polyimide board.
- (2) Back side: GNDpattern
- (3) Solder plated on pattern
- (4) $\oplus \ominus \bigoplus$: Through holes

[MEMO]

[MEMO]

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Anti-radioactive design is not implemented in this product.