10 Gigabit/s Transceiver with XAUI Interface

The **TenGiPHY™-L is a single chip transceiver IC for 10 Gbit/s Ethernet and Fibre Channel connectivity. It offers a serial, full duplex 10 Gbit/s, XFI compliant interface to optical components or to a serial fiber-optic module (XFP). The integrated CDR and CMU operate at a data rate of 10.3125 or 10.51875 Gbit/s. The TenGiPHY-L provides the XGXS, PCS and PMA sublayers of the 10 Gbit/s Ethernet and Fibre Channel standards.**

At the system side, a quad serial XAUI interface connects the TenGiPHY-L to the upper layers.

The networking system can control the chip via a narrow-width MDIO interface by writing and reading its control and status registers.

Applications

- Fiber optic modules according to the XENPAK multi-source agreement
- 10 Gbit/s Ethernet line cards
- 10 Gbit/s Fibre Channel line and NIC cards
- Terabit Routers

Features

- Complete 10 Gbit/s Ethernet and Fibre Channel PHY device supporting LAN applications
- Complies with IEEE 802.3ae
- Complies with ANSI 1413-D
- Compliant to XENPAK multi-source agreement
- Embedded µController allows for control and tuning of the PMDs via analog interfaces

- Clock & data recovery and clock multiplying unit without external loop filter components
- Supports various clocking modes based on external reference clocks, loop- and external timing
- Integrated bit error rate tester (BERT) usable for multiple at-speed diagnostic scenarios
- Includes the XGXS, PCS, and PMA sublayers of the OSI protocol stack
- Synchronization and de-skewing of XAUI lanes
- Performs 8B/10B (de-)coding required for the XGXS sublayer
- Various loop back modes for system debugging

- Provides access to E²PROM via I²C interface according to XENPAK requirements; automatic E²PROM download on power-up
- Power-efficient design: <1.3W @ 1.3V

Interfaces

- Full duplex, XFI compliant serial CML line interface for data rates between 10.3 and 10.5 Gbit/s
- Quad serial Gbit/s XAUI interface with data rates between 3.1 and 3.2 Gbit/s
- MDIO interface
- I²C interface
- XENPAK diagnostic interface providing eight 12-bit ADCs and four 10-bit DACs
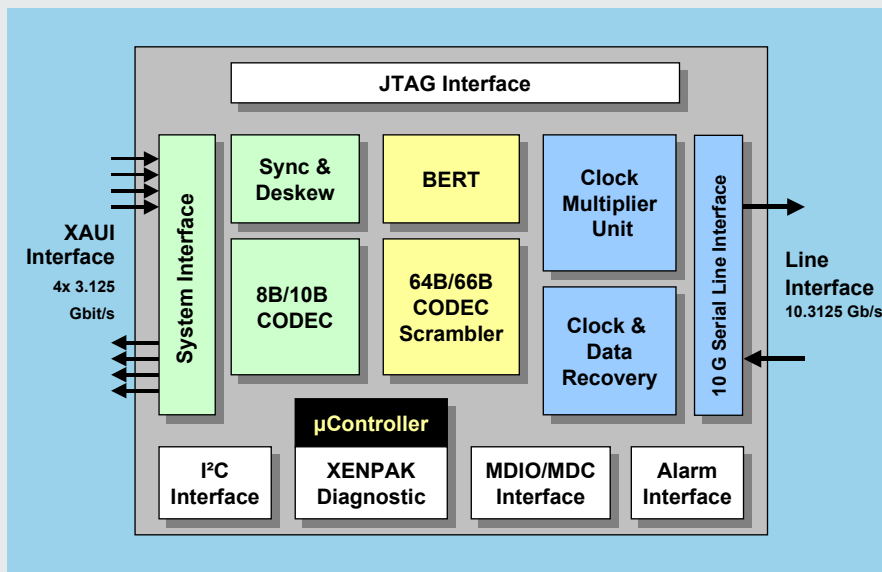- IEEE 1149.1 JTAG boundary scan interface

UPF 01012

TenGiPHY™-L

Infineon technologies

Block Diagram

JTAG Interface

Sync & Deskew

BERT

Clock Multiplier Unit

System Interface

8B/10B CODEC

64B/66B CODEC Scrambler

Clock & Data Recovery

10 G Serial Line Interface

XAUI Interface
4x 3.125 Gbit/s

Line Interface
10.3125 Gb/s

µController

I²C Interface

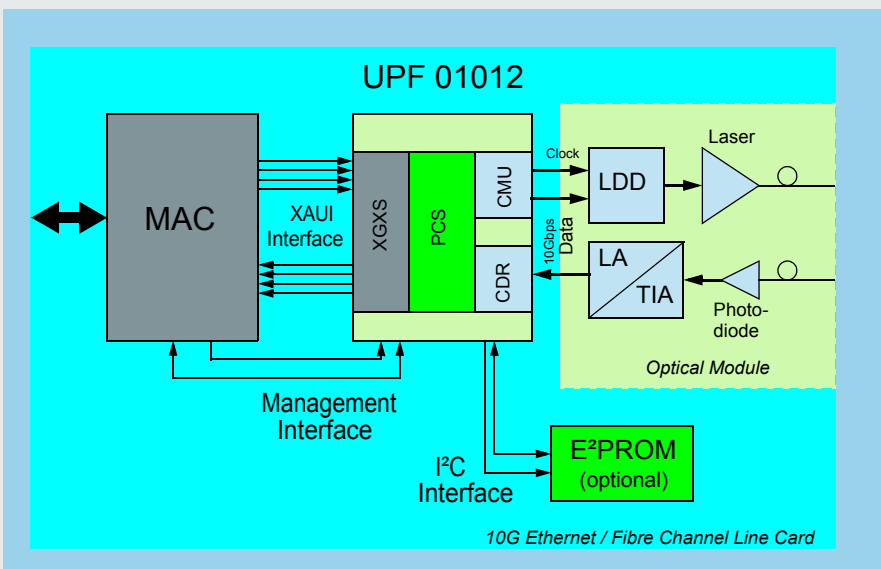XENPAK Diagnostic

MDIO/MDC Interface

Alarm Interface

Documentation and Support Package

- Data Sheet
- **Hardware Evaluation System** includes mother- and transponder board
- **WINEASY** Software for MS Windows with graphical user interface
- **Application Assistant:** Configuration Software for MS Windows for device initialization

Type	Sales Code	Package
TenGiPHY-L	UPF 01012	P-FCHBGA-177-1

Application Example

UPF 01012

MAC

XAUI Interface

XGXS

PCS

CMU

CDR

Clock

10Gbps Data

LDD

Laser

LA TIA

Photo-diode

Optical Module

Management Interface

I²C Interface

E²PROM (optional)

10G Ethernet / Fibre Channel Line Card

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

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We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide.

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