NEC

9 GHz DIVIDE-BY-4 DYNAMIC PRESCALER

UPG503B

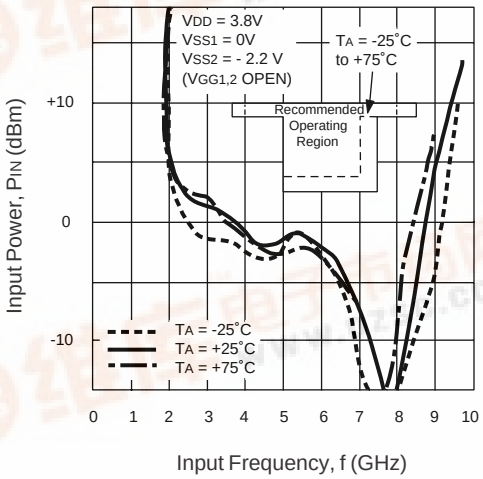
FEATURES

- **WIDE OPERATING FREQUENCY RANGE:**
  f_{IN} = 3.5 to 9.0 GHz (T_A = 25°C)
- **DIVISION RATIO OF 4**
- **GUARANTEED OPERATING TEMPERATURE RANGE:**
  -25°C to +75°C

DESCRIPTION

The UPG503B is a GaAs divide-by-4 prescaler that is capable of operating up to 9 GHz. It is designed to be used in the frequency synthesizers of microwave communication systems and measurement equipment. The UPG503B is a dynamic divider. It employs buffered FET logic (BFL). The UPG503B is available in a hermetic 8-lead ceramic flat package.

INPUT POWER vs. INPUT FREQUENCY



ELECTRICAL CHARACTERISTICS[1] (T_A = 25°C, V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V)

PART NUMBER PACKAGE OUTLINE			UPG503B BF08		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{DD}	Supply Current	mA	40	80	130
I_{SS1}	Sink Current[2] $I_{SS1} = I_{DD} - I_{SS2}$	mA		27	
I_{SS2}	Sink Current[2]	mA	21	53	93
$f_{IN(U)}$	Upper Limit of Input Frequency, P_{IN} = +9 to +10 dBm	GHz	8.6	9.0	
$f_{IN(L)}$	Lower Limit of Input Frequency, P_{IN} = +9 to +10 dBm	GHz		3.5	3.7
P_{IN}	Input Power, f_{IN} = 3.7 to 8.6 GHz f_{IN} = 5.0 to 7.4 GHz	dBm dBm	9.0 3.0		10.0 10.0
P_{OUT}	Output Power, f_{IN} = 8.6 GHz, P_{IN} = +10 dBm f_{IN} = 3.7 GHz, P_{IN} = +10 dBm	dBm dBm	0 0	3 3	
R_{TH}	Thermal Resistance, Channel to Case	°C/W			10

Note:
1.Device may exhibit low frequency spur typically below 150 Hz and -45 dBm.
2. Current is positive into the I_{DD} pin and returns through the I_{SS1} and I_{SS2} pins.

ELECTRICAL CHARACTERISTICS (T_A = 25°C to +75°C, V_{DD} = 3.8 V, V_{SS1} = 0 V, V_{SS2} = -2.2 V)

PART NUMBER PACKAGE OUTLINE			UPG503B BF08		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{DD}	Supply Current	mA		80	
I_{SS1}	Sink Current[1] $I_{SS1} = I_{DD} - I_{SS2}$	mA		27	
I_{SS2}	Sink Current[1]	mA		53	
$f_{IN(U)}$	Upper Limit of Input Frequency, P_{IN} = +9 to +10 dBm	GHz	8.0		
$f_{IN(L)}$	Lower Limit of Input Frequency, P_{IN} = +9 to +10 dBm	GHz			4.0
P_{IN}	Input Power, f_{IN} = 4.0 to 8.0 GHz f_{IN} = 5.0 to 7.0 GHz	dBm dBm	9.0 4.0		10.0 10.0
P_{OUT}	Output Power f_{IN} = 8.0 GHz, P_{IN} = +10 dBm f_{IN} = 4.0 GHz, P_{IN} = +10 dBm	dBm dBm	-1.0 -1.0	2.0 2.0	

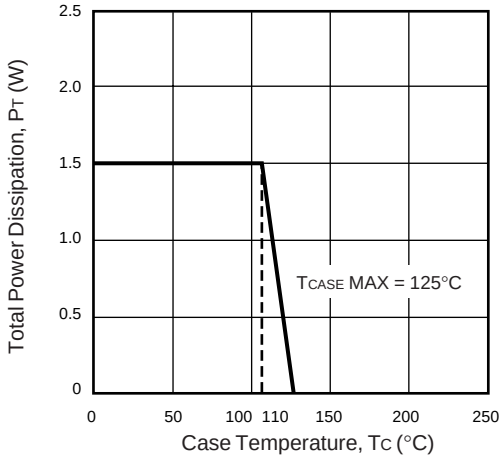
Note:
1. Current is positive into the I_{DD} pin and returns through the I_{SS1} and I_{SS2} pins.

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD}-V_{SS1}	Supply Voltage	V	5.0
V_{SS2}-V_{SS1}	Supply Voltage	V	-5.0
P_{IN}	Input Power	dBm	13
P_T	Total Power Dissipation[2]	W	1.5
T_{STG}	Storage Temperature	°C	-65 to +175
T_C	Case Temperature	°C	-65 to +125

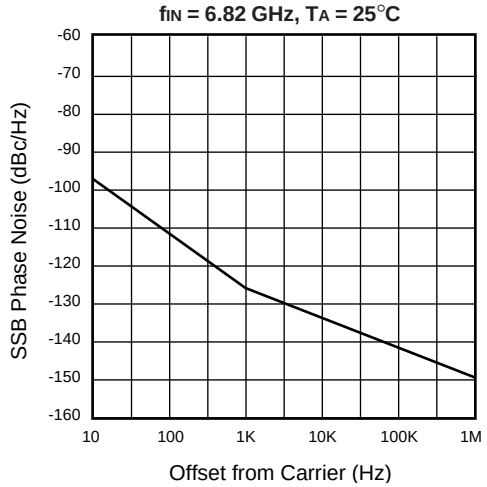
Notes:
1. Operation in excess of any one of these conditions may result in permanent damage.
2. $T_C \leq 125°C$

POWER DERATING CURVE

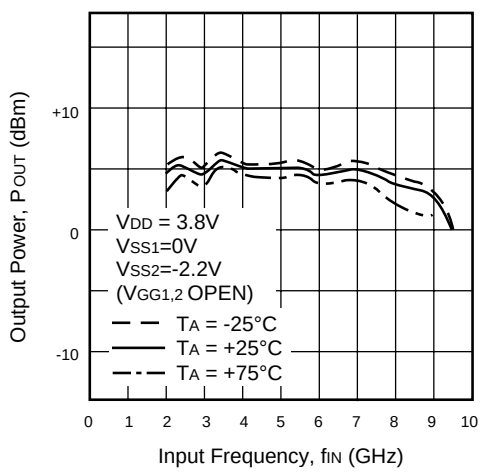


TYPICAL PERFORMANCE CURVES (T_A = 25°)

SSB PHASE NOISE VS. OFFSET FROM CARRIER
f_{IN} = 6.82 GHz, T_A = 25°C

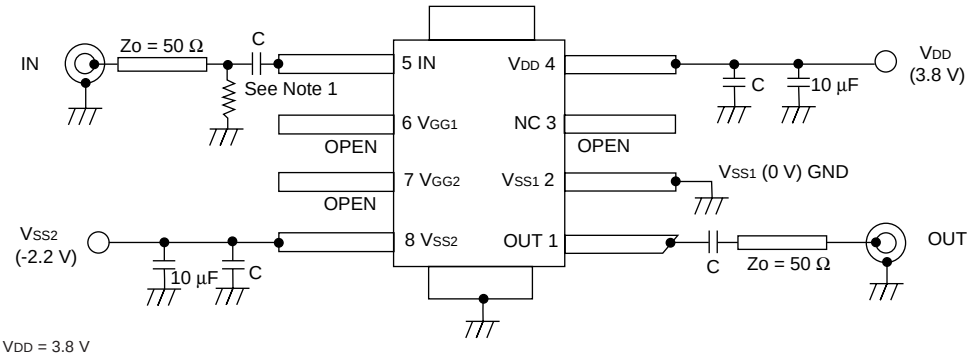


OUTPUT POWER vs. INPUT FREQUENCY



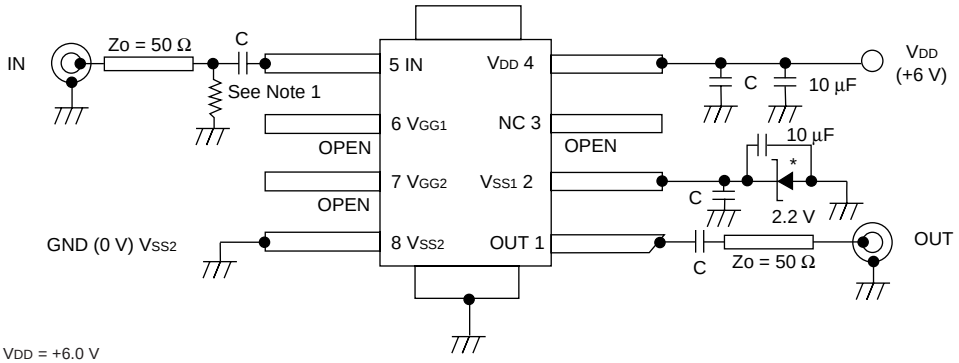
POWER SUPPLY CONFIGURATIONS (V_{GG1} and V_{GG2} are normally open)

CONFIGURATION 1
2 Bias Supply



V_{DD} = 3.8 V
V_{SS1} = 0 V (GND)
V_{SS2} = –2.2 V
C: 1000 - 5000 pF Chip Capacitor

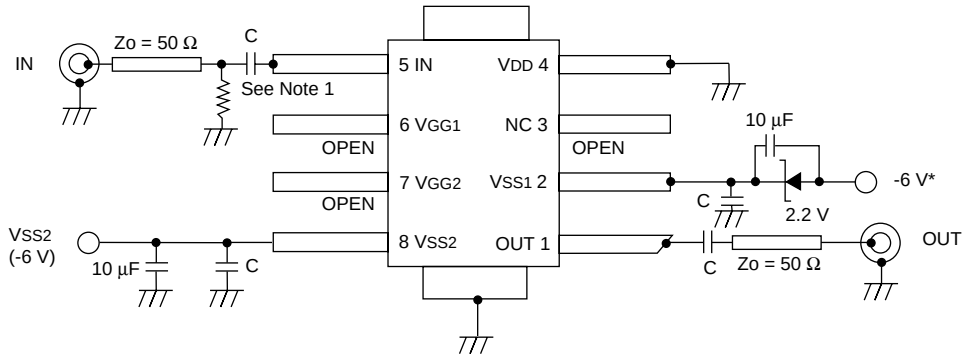
CONFIGURATION 2
Single Positive Bias Supply



V_{DD} = +6.0 V
V_{SS2} = 0 V (GND)
C: 1000 - 5000 pF Chip Capacitor

* V_{SS1} should be connected to GND through a 2.2 V Zener Diode (RD2.2FB or IN3394).

CONFIGURATION 3
Single Negative Bias Supply



V_{DD} = 0 V (GND)
V_{SS2} = –6 V
C: 1000 - 5000 pF Chip Capacitor

* For V_{SS1}, the bias voltage of -6.0 should be applied through a 2.2 V Zener Diode (RD2.2FB or IN3394).

Notes:

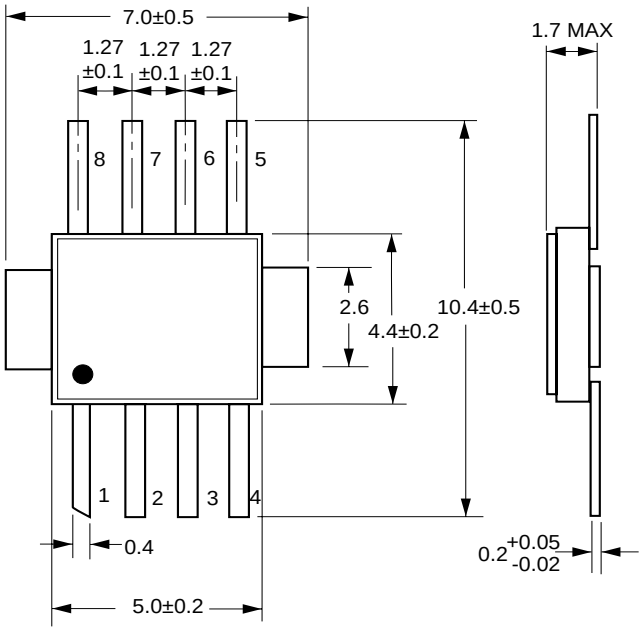
1. Because of the high internal gain and gain compression of the UPG503B, the device is prone to self-oscillation in the absence of an RF input signal. This self-oscillation can be suppressed by either of the following means:
   - Add a shunt resistor to the RF input line. Typically a resistor value between 50 and 1000 ohms will suppress the self-oscillation (see the test circuit schematic).
   - Apply a negative voltage through a 1000 ohm resistor to the normally open V_{GG1} connection. Typically voltages between 0 and -9 volts will suppress the self-oscillation.

Both of these approaches will reduce the input sensitivity of the device (by as much as 3 dB for a 50 ohm shunt resistor), but otherwise have no effect on the reliability or electrical characteristics of the device.

OUTLINE DIMENSIONS (Units in mm)

UPG503B

PACKAGE OUTLINE BF08



LEAD CONNECTIONS:

1. OUTPUT
2. V_{SS1}
3. NC*
4. V_{DD}
5. INPUT
6. V_{GG1}
7. V_{GG2}
8. V_{SS2}

* No Connection