5 BIT PROGRAMMABLE SYNCHRONOUS BUCK PLUS NON SYNCHRONOUS , LDO CONTROLLER AND 200MmA LDO ON BOARD

PRELIMINARY DATASHEET

FEATURES

- **Provides Single Chip Solution for Vcore, GTL+ ,Clock Supply & 3.3V Switcher on board**
- **Second Switcher Provides Simple Control for the On board 3.3V supply**
- **200 mA On board LDO regulator**
- **Designed to meet Intel VRM 8.2 and 8.3 specification for Pentium II™**
- **On board DAC programs the output voltage from 1.3V to 3.5V**
- **Linear regulator controller on board for 1.5V GTL+ supply**
- **Loss less Short Circuit Protection**
- **Synchronous operation allows maximum efficiency**
- **Patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load**
- **Minimum part count**
- **Soft Start**
- **High current totem pole driver for direct driving of the external Power MOSFET**
- **Power Good function Monitors all Outputs**
- **OVP Circuitry Protects the Switcher Outputs and generates a Fault output**
- **Thermal Shutdown**

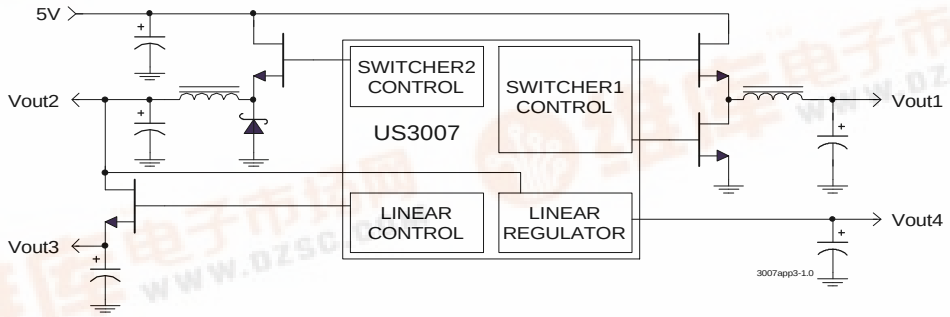
APPLICATIONS

- Total Power Soloution for Pentium II processor application

DESCRIPTION

The US3007 controller IC is specifically designed to meet Intel specification for Pentium II™ microprocessor applications as well as the next generation of P6 family processors. **The US3007 provides a single chip controller IC for the Vcore , LDO controller for GTL+ and an internal 200mA regulator for clock supply which are required for the Pentium II applications. It also contains a switching controller to convert 5V to 3.3V regulator for an on board applications that either uses AT type power supply or it is desired not to rely on the ATX power supply's 3.3V output.** These devices feature a patented topology that in combination with a few external components as shown in the typical application circuit ,will provide in excess of 14A of output current for an on- board DC/DC converter while automatically providing the right output voltage via the 5 bit internal DAC .The US3007 also features, **loss less current sensing for both switchers by using the Rds-on of the high side Power MOSFET as the sensing resistor, internal current limiting for the clock supply**, a Power Good window comparator that switches its open collector output low when any one of the outputs is outside of a pre programmed window. Other features of the device are ; Undervoltage lockout for both 5V and 12V supplies, an external programmable soft start function , programming the oscillator frequency via an external resistor, OVP circuitry for both switcher outputs and an internal thermal shutdown.

TYPICAL APPLICATION



Notes: Pentium II and Pentium Pro are trade marks of Intel Corp.

PACKAGE ORDER INFORMATION

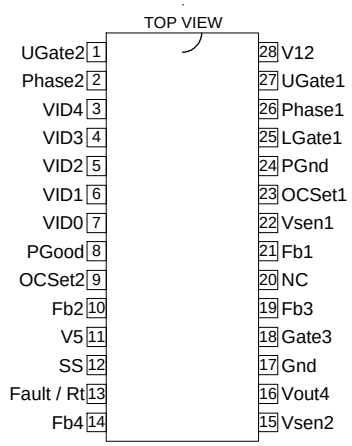
Ta (°C)	Device	Package
0 TO 70	US3007CW	28 pin Plastic SOIC WB

ABSOLUTE MAXIMUM RATINGS

V5 supply Voltage 7V
V12 Supply Voltage 20V
Storage Temperature Range ..... -65 TO 150°C
Operating Junction Temperature Range ..... 0 TO 125°C

PACKAGE INFORMATION

28 PIN WIDE BODY PLASTIC SOIC (W)



θ_{JA} =80°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified ,these specifications apply over ,V_{12} = 12V, V_5 = 5V and Ta=0 to 70°C. Typical values refer to Ta =25°C. Low duty cycle pulse testing are used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply UVLO Section						
UVLO Threshold-12V		Supply ramping up		10		V
UVLO Hysterises-12V				0.4		V
UVLO Threshold-5V		Supply ramping up		4.3		V
UVLO Hysterises-5V				0.3		V
Supply Current						
Operating Supply Current		V12 V5		6 30		mA
Switching Controllers; Vcore (Vout 1) and I/O (Vout 2)						
VID Section (Vcore only)						
DAC output voltage (note 1)			0.99Vs	Vs	1.01Vs	V
DAC Output Line Regulation				0.1		%
DAC Output Temp Variation				0.5		%
VID Input LO					0.8	V
VID Input HI			2			V
VID input internal pull-up resistor to V5			27		kΩ	
Vfb2 Voltage				2		V

Error Comparator Section						
Input bias current					2	uA
Input Offset Voltage			-2		+2	mV
Delay to Output		Vdiff=10mV			100	nS
Current Limit Section						
C.S Threshold Set Current				200		uA
C.S Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css=0.1 uF		10		%
Output Drivers Section						
Rise Time		CL=3000pF		70		nS
Fall Time		CL=3000pF		70		nS
Dead band Time Between High side and Synch Drive (Vcore Switcher Only)		CL=3000pF		200		nS
Oscillator Section (internal)						
Osc Frequency		Rt=Open		200		Khz
2.5V Regulator (Vout 4)						
Reference Voltage	Vo4	Ta=25, Vout4 = FB4		1.260		V
Reference Voltage				1.260		V
Dropout Voltage		Io = 200 mA		0.6		V
Load Regulation		1mA< Io <200 mA		0.5		%
Line Regulation		3.1V<VIO<4V, Vo=2.5V		0.2		%
Input bias current					2	uA
Output Current			200			mA
Current limit			300			mA
Thermal Shutdown				145		°C
1.5V Regulator (Vout 3)						
Reference Voltage	Vo3	Ta=25, GATE3 = FB3		1.260		V
Reference Voltage				1.260		V
Input bias current					2	uA
Output Drive Current			50			mA
Power Good Section						
Core U.V lower trip point		Vsen1 ramping down		0.90Vs		V
Core U.V upper trip point		Vsen1 ramping up		0.92Vs		V
Core U.V Hysterises				.02Vs		V
Core O.V upper trip point		Vsen1 ramping up		1.10Vs		V
Core O.V lower trip point		Vsen1 ramping down		1.08Vs		V
Core O.V Hysterises				.02Vs		V
I/O U.V lower trip point		Vsen2 ramping down		2.4		V
I/O U.V upper trip point		Vsen2 ramping up		2.6		V
FB4 lower trip point		FB4 ramping down		0.95		V
FB4 upper trip point		FB4 ramping up		1.05		V
FB3 lower trip point		FB3 ramping down		0.95		V
FB3 upper trip point		FB3 ramping up		1.05		V
Power Good Output LO		RL=3mA		0.4		V
Power Good Output HI		RL=5K pull up to 5V		4.8		V
Fault (Overvoltage) Section						
Core O.V. upper trip point		Vsen1 ramping up		1.17Vs		V
Core O.V. lower trip point		Vsen1 ramping down		1.15Vs		V
Soft Start Section						
Pull up resistor to 5V		OCset=0V , Phase=5V		23		KΩ

I/O O.V. upper trip point		Vsen2 ramping up		4.3		V
I/O O.V. lower trip point		Vsen2 ramping down		4.2		V
FAULT Output HI		Io=3mA		10		V

Note 1: Vs refers to the set point voltage given in Table 1.

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	2.0
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Table 1 - Set point voltage vs. VID codes

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	Pin Description
7	VID0	LSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open,his pin is pulled up internally by a 27kΩ resistor to 5V supply.
6	VID1	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open,his pin is pulled up internally by a 27kΩ resistor to 5V supply.
5	VID2	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open,his pin is pulled up internally by a 27kΩ resistor to 5V supply.
4	VID3	MSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open,his pin is pulled up internally by a 27kΩ resistor to 5V supply.
3	VID4	This pin selects a range of output voltages for the DAC.When in the LOW state the range is 1.3V to 2.05V and when it switches to HI state the range is 2.0V to 3.5V. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open,his pin is pulled up internally by a 27kΩ resistor to 5V supply.
8	PGOOD	This pin is an open collector output that switches LO when any of the outputs are outside of the specified under voltage trip point. It also switches low when Vsen1 pin is more than 10% above the DAC voltage setting.
21	FB1	This pin provides the feedback for the synchronous switching regulator. Typically this pin can be connected directly to the output of the switching regulator. However, a resistor divider is recommended to be connected from this pin to vout1 and GND to adjust the output voltage for any drop in the output voltage that is caused by the trace resistance. The value of the resistor connected from Vou1 to FB1 must be less than 100Ω.

PIN#	PIN SYMBOL	Pin Description
22	VSEN1	This pin is internally connected to the undervoltage and overvoltage comparators sensing the Vcore status. It must be connected directly to the Vcore supply.
10	FB2	This pin provides the feedback for the non-synchronous switching regulator. A resistor divider is connected from this pin to vout2 and GND that sets the output voltage. The value of the resistor connected from Vout2 to FB2 must be less than 100Ω.
15	VSEN2	This pin is connected to the output of the I/O switching regulator. It is an input that provides sensing for the Under/Over voltage circuitry for the I/O supply as well as the power for the internal LDO regulator.
23	OCSET1	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the C.S threshold depending on the Rds of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
26	PHASE1	This pin is connected to the Source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
9	OCSET2	This pin is connected to the Drain of the power MOSFET of the I/O supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the C.S threshold depending on the Rds of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
2	PHASE2	This pin is connected to the Source of the power MOSFET for the I/O supply and it provides the negative sensing for the internal current sensing circuitry.
12	SS	This pin provides the soft start for the 2 switching regulators. An internal resistor charges an external capacitor that is connected from 5V supply to this pin which ramps up the outputs of the switching regulators, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
13	FAULT/Rt	This pin has dual function. It acts as an output of the OVP circuitry or it can be used to program the frequency using an external resistor . When used as a fault detector, if any of the switcher outputs exceed the OVP trip point, the FAULT pin switches to 12V and the soft start cap is discharged. If the FAULT pin is to be connected to any external circuitry, it needs to be buffered as shown in the application circuit.
18	GATE3	This pin controls the gate of an external transistor for the 1.5V GTL+ linear regulator.
19	FB3	This pin provides the feedback for the linear regulator that its output drive is GATE3.
16	VOUT4	This pin is the output of the internal LDO regulator.
14	FB4	This pin provides the feedback for the internal LDO regulator that its output is Vout4.
17	GND	This pin serves as the ground pin and must be connected directly to the ground plane.
24	PGND	This pin serves as the Power ground pin and must be connected directly to the GND plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1 uF) must be connected from V12 pin to this pin for noise free operation.
25	LGATE1	Output driver for the synchronous power MOSFET for the Core supply.
27	UGATE1	Output driver for the high side power MOSFET for the Core supply.
1	UGATE2	Output driver for the high side power MOSFET for the I/O supply.
28	V12	This pin is connected to the 12 V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (typically 1 uF) must be placed close to this pin and PGND pin and be connected directly from this pin to the GND plane for the noise free operation.
11	V5	5V supply voltage. A high frequency capacitor (0.1 to 1 uF) must be placed close to this pin and connected from this pin to the GND plane for noise free operation.
20	N.C	No connect

BLOCK DIAGRAM

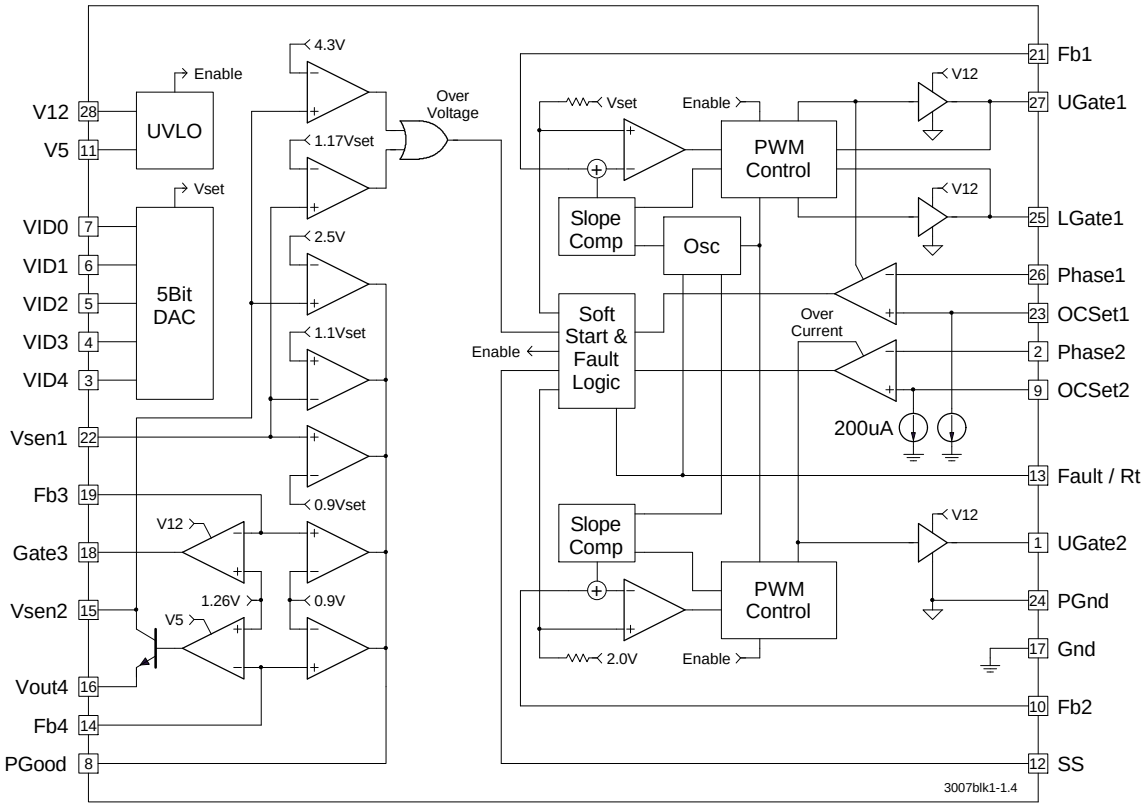


Figure 1 - Simplified block diagram of the US3007

TYPICAL APPLICATION

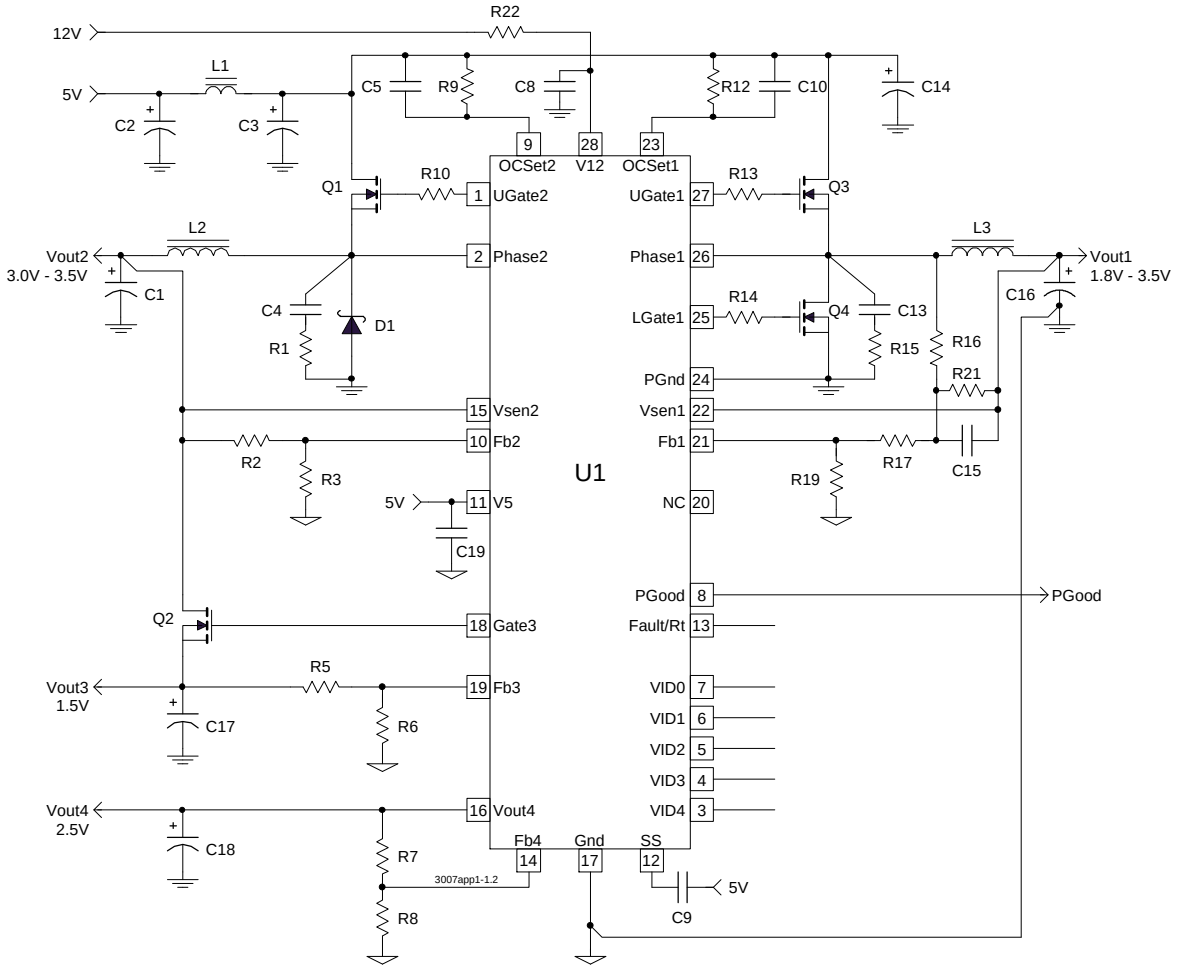


Figure 2 - Typical application of US3007 for an on board DC-DC converter providing power for the Vcore , GTL+, Clock supply as well as an on board 3.3V I/O supply for the Deschutes and the next generation processor applications.

US3007 Application Parts List

Ref Desig	Description	Qty	Part #	Manufacture
Q1	MOSFET	1	IRL3103S, TO263 package	IR
Q2	MOSFET	1	RLR024, TO252 package	IR
Q3	MOSFET	1	IRL3103S, TO263 package	IR
Q4	MOSFET with Schottky	1	IRL3103D1S, TO263 package	IR
D1	Diode	1	MBRB1035, TO263 package	IR
L1	Inductor	1 1	L=1uH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L2	Inductor	1	L=4.7uH, 5052 core with 11 turns of 1.0mm wire	Micro Metal
L3	Inductor	1	L=2.7uH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Electrolytic	2	6MV1500GX, 1500uF,6.3V	Sanyo
C2	Capacitor, Electrolytic	1	10MV470GX, 470uF,10V	Sanyo
C3	Capacitor, Electrolytic	1	10MV1200GX, 1200uF,10V	Sanyo
C4,13	Capacitor, Ceramic	2	1000pF, 0603	
C5,10	Capacitor, Ceramic	2	220pF, 0603	
C8	Capacitor, Ceramic	1	1uF, 0805	
C9,15,19	Capacitor, Ceramic	3	1uF, 0603	
C14	Capacitor, Electrolytic	2	10MV1200GX, 1200uF,10V	Sanyo
C16	Capacitor, Electrolytic	6	6MV1500GX, 1500uF,6.3V	Sanyo
C17	Capacitor, Electrolytic	1	6MV1000GX, 1000uF,6.3V	Sanyo
C18	Capacitor, Electrolytic	1	6MV150GX, 150uF,6.3V	Sanyo
R1,5,13 ,14	Resistor	4	4.7Ω, 5%, 1206	
R2	Resistor	1	75Ω, 1%, 0603	
R3,6,7,8	Resistor	4	100Ω, 1%, 0603	
R5	Resistor	1	19.1Ω, 1%, 0603	
R9	Resistor	1	1.5kΩ, 5%, 0603	
R10	Resistor	1	10Ω, 5%, 1206	
R12	Resistor	1	3.3kΩ, 5%, 0603	
R16,17,21	Resistor	3	2.2kΩ, 1%, 0603	
R19	Resistor	1	220kΩ, 1%, 0603	
R22	Resistor	1	10Ω, 5%, 0603	

TYPICAL APPLICATION

(Dual Layout with HIP6019)

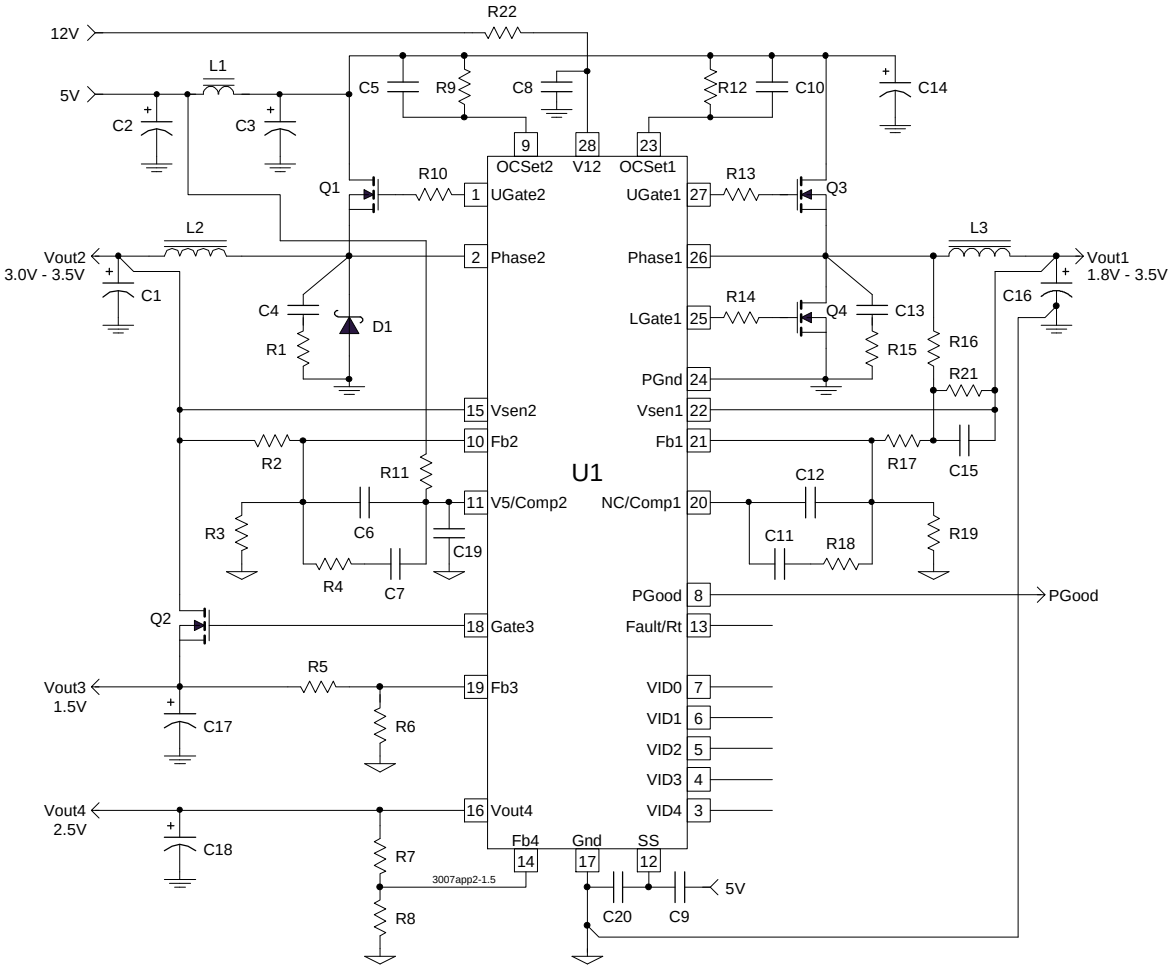


Figure 3 - Typical application of US3007 in a dual layout with HIP6019 for an on board DC-DC converter providing power for the Vcore , GTL+, Clock supply as well as an on board 3.3V I/O supply for the Deschutes and the next generation processor applications.

Components that need to be modified to make the dual layout work for US3007 and HIP6019.

Part #	R4	R11	R18	C6	C7	C9	C11	C12	C19	C20
HIP6019	V	O	V	V	V	O	V	V	O	V
US3007	O	S	O	O	O	V	O	O	V	O

S - Short O - Open V - See Unisem or Harris parts list for the value.

Table 2 - Dual layout component table

US3007 Application Parts List
Dual Layout with HIP6019

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103S, TO263 package	IR
Q2	MOSFET	1	IRLR024, TO252 package	IR
Q3	MOSFET	1	IRL3103S, TO263 package	IR
Q4	MOSFET with Schottky	1	IRL3103D1S, TO263 package	IR
D1	Diode	1	MBRB1035, TO263 package	IR
L1	Inductor	1	L=1uH, 5052 core with 4 turns of 1.0 mm wire	Micro Metal
L2	Inductor	1	L=4.7uH, 5052 core with 11 turns of 1.0mm wire	Micro Metal
L3	Inductor	1	L=2.7uH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Electrolytic	2	6MV1500GX, 1500uF,6.3V	Sanyo
C2	Capacitor, Electrolytic	1	10MV470GX, 470uF,10V	Sanyo
C3	Capacitor, Electrolytic	1	10MV1200GX, 1200uF,10V	Sanyo
C4,13	Capacitor, Ceramic	2	1000pF, 0603	
C5,10	Capacitor, Ceramic	2	220pF, 0603	
C6,7,11,12,20	Capacitor, Ceramic	5	See Table 2, dual layout component 0603 * 5	
C8	Capacitor, Ceramic	1	1uF, 0805	
C9,15,19	Capacitor, Ceramic	3	1uF, 0603	
C14	Capacitor, Electrolytic	2	10MV1200GX, 1200uF,10V	Sanyo
C16	Capacitor, Electrolytic	6	6MV1500GX, 1500uF,6.3V	Sanyo
C17	Capacitor, Electrolytic	1	6MV1000GX, 1000uF,6.3V	Sanyo
C18	Capacitor, Electrolytic	1	6MV150GX, 150uF,6.3V	Sanyo
R1,13,14,15	Resistor	4	4.7Ω, 5%, 1206	
R2	Resistor	1	75Ω, 1%, 0603	
R3,6,7,8	Resistor	4	100Ω, 1%, 0603	
R4,18	Resistor	2	See Table 2, dual layout component 0603 * 2	
R5	Resistor	1	19.1Ω, 1%, 0603	
R9	Resistor	1	1.5kΩ, 5%, 0603	
R10	Resistor	1	10Ω, 5%, 1206	
R11	Resistor	1	0Ω, 0603	
R12	Resistor	1	3.3kΩ, 5%, 0603	
R16,17,21	Resistor	3	2.2kΩ, 1%, 0603	
R19	Resistor	1	220kΩ, 1%, 0603	
R22	Resistor	1	10Ω, 5%, 0603	

Application Information

An example of how to calculate the components for the application circuit is given below.
Assuming, two set of output conditions that this regulator must meet for Vcore :
a) Vo=2.8V , Io=14.2A, ΔVo=185mV, ΔIo=14.2A
b) Vo=2V , Io=14.2A, ΔVo=140mV, ΔIo=14.2A
Also, the on board 3.3V supply must be able to provide 10A load current and maintain less than ±5% total output voltage variation.
The regulator design will be done such that it meets the worst case requirement of each condition.

Output Capacitor Selection
Vcore
The first step is to select the output capacitor. This is done primarily by selecting the maximum ESR value that meets the transient voltage budget of the total ΔVo specification. Assuming that the regulators DC initial accuracy plus the output ripple is 2% of the output voltage, then the maximum ESR of the output capacitor is calculated as :

$$ESR \le \frac{100}{14.2} = 7\ m\Omega$$

The Sanyo MVGX series is a good choice to achieve both the price and performance goals. The 6MV1500GX , 1500uF, 6.3V has an ESR of less than 36 mΩ typ . Selecting 6 of these capacitors in parallel has an ESR of ≈6 mΩ which achieves our low ESR goal.

Other type of Electrolytic capacitors from other manufacturers to consider are the Panasonic "FA" series or the Nichicon "PL" series.
3.3V supply
For the 3.3V supply, since there is not fast transient requirement, 2 of the 1500uf capacitors is sufficient.

Reducing the Output Capacitors Using Voltage Level Shifting Technique

The trace resistance or an external resistor from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly **reduce the number of output capacitors, by level shifting the DC regulation point when transitioninig from light load to full load and vice versa**. To accomplish this, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the GND pin of the 3007 is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70 mV or 35mV higher than the DAC voltage setting. This intentional voltage level shifting during the load transient eases the requirement for the output capacitor ESR at the cost of load regulation. One can show that the new ESR requirement eases up by **half the total trace resistance.** For example, if the ESR requirement of the output capacitors without voltage level shifting must be 7mΩ then after level shifting the new ESR will only need to be 8.5mΩ if the trace resistance is 5mΩ (7+5/2=9.5). However, one must be careful that the combined "voltage level shifting" and the transient response is still within the maximum tolerance of the Intel specification. To insure this, the maximum trace resistance must be less than:
Rs≤ 2(Vspec - 0.02*Vo - ΔVo)/ΔI
Where :
Rs=Total maximum trace resistance allowed
Vspec=Intel total voltage spec
Vo=Output voltage
ΔVo=Output ripple voltage
ΔI=load current step
For example, assuming:
Vspec=±140 mV=±0.1V for 2V output
Vo=2V
ΔVo=assume 10mV=0.01V
ΔI=14.2A
Then the Rs is calculated to be:
Rs≤ 2(0.140 - 0.02*2 - 0.01)/14.2=12.6mΩ
However, if a resistor of this value is used, the maximum power dissipated in the trace (or if an external resistor is being used) must also be considered. For example if Rs=12.6 mΩ , the power dissipated is (Io^2)*Rs=(14.2^2)*12.6=2.54W. This is a lot of power to be dissipated in a system. So, if the Rs=5mΩ, then the power dissipated is about 1W which is much more acceptable. If level shifting is not implemented, then the maximum output capacitor ESR was shown previously to be 7mΩ which translated to ≈ 6 of the 1500uF, 6MV1500GX type Sanyo capacitors. With Rs=5mΩ, the maximum ESR becomes 9.5mΩ which is equivalent to ≈ 4 caps. Another important consideration is that **if a trace is being used to implement the resistor, the power dissipated by the trace increases the case temperature of the output capacitors which could seriously effect the life time of the output capacitors.**

Output Inductor Selection

The output inductance must be selected such that under low line and the maximum output voltage condition, the inductor current slope times the output capacitor ESR is ramping up faster than the capacitor voltage is drooping during a load current step. However if the inductor is too small , the output ripple current and ripple voltage become too large. One solution to bring the ripple current down is to increase the switching frequency , however that will be at the cost of reduced efficiency and higher system cost. The following set of formulas are derived to achieve the optimum performance without many design iterations.

The maximum output inductance is calculated using the following equation :

$L = ESR * C * (Vinmin - Vomax) / (2* \Delta I)$

Where :

Vinmin = Minimum input voltage

For Vo = 2.8 V , ΔI = 14.2 A

$L = 0.006 * 9000 * (4.75 - 2.8) / (2 * 14.2) = 3.7$ uH

Assuming that the programmed switching frequency is set at 200 KHZ , an inductor is designed using the Micrometals' powder iron core material. The summary of the design is outlined below :

The selected core material is Powder Iron , the selected core is T50-52D from Micro Metal wounded with 8 Turns of # 16 AWG wire, resulting in 3 uH inductance with ≈ 3 mΩ of DC resistance.

Assuming L = 3 uH and the switching frequency ; Fsw = 200 KHZ , the inductor ripple current and the output ripple voltage is calculated using the following set of equations :

T = 1/Fsw

T ≡ Switching Period

$D \approx (Vo + Vsync) / (Vin - Vsw + Vsync)$

D ≡ Duty Cycle

Ton = D * T

Vsw ≡ High side Mosfet ON Voltage = Io * Rds

Rds ≡ Mosfet On Resistance

Toff = T - Ton

Vsync ≡ Synchronous MOSFET ON Voltage=Io * Rds

$\Delta Ir = (Vo + Vsync) * Toff / L$

ΔIr ≡ Inductor Ripple Current

$\Delta Vo = \Delta Ir * ESR$

ΔVo ≡Output Ripple Voltage

In our example for Vo = 2.8V and 14.2 A load , Assuming IRL3103 MOSFET for both switches with maximum on resistance of 19 mΩ, we have :

T = 1 / 200000 = 5 uSec

Vsw =Vsync= 14.2*0.019=0.27 V

$D \approx (2.8 + 0.27) / (5 - 0.27 + 0.27) = 0.61$

Ton = 0.61 * 5 = 3.1 uSec

Toff = 5 - 3.1 = 1.9 uSec

$\Delta Ir = (2.8 + 0.27) * 1.9 / 3 = 1.94$ A

$\Delta Vo = 1.94 * .006 = .011$ V = 11 mV

Power Component Selection

Vcore

Assuming IRL3103 MOSFETs as power components, we will calculate the maximum power dissipation as follows:

For high side switch the maximum power dissipation happens at maximum Vo and maximum duty cycle.

$Dmax \approx (2.8 + 0.27) / (4.75 - 0.27 + 0.27) = 0.65$

Pdh = Dmax * Io^2*Rds(max)

Pdh= 0.65*14.2^2*0.029=3.8 W

Rds(max)=Maximum Rds-on of the MOSFET at 125°C

For synch MOSFET, maximum power dissipation happens at minimum Vo and minimum duty cycle.

$Dmin \approx (2 + 0.27) / (5.25 - 0.27 + 0.27) = 0.43$

Pds = (1-Dmin)*Io^2*Rds(max)

Pds=(1 - 0.43) * 14.2^2 * 0.029 = 3.33 W

3.3V Supply

Again,for high side switch the maximum power dissipation happens at maximum Vo and maximum duty cycle. The duty cycle equation for non synchronous replaces the forward voltage of the diode with the Synch MOSFET on voltage. In equation below, Vf=0.5V

$Dmax \approx (3.3 + 0.5) / (4.75 - 0.27 + 0.5) = 0.76$

Pdh = Dmax * Io^2*Rds(max)

Pdh= 0.76*10^2*0.029=2.21 W

Rds(max)=Maximum Rds-on of the MOSFET at 125°C

For diode, the maximum power dissipation happens at minimum Vo and minimum duty cycle.

$Dmin \approx (3.3 + 0.5) / (5.25 - 0.27 + 0.5) = 0.69$

Pdd = (1-Dmin)*Io*Vf=(1 - 0.69) * 10 * 0.5 = 1.55 W

Switcher Current Limit Protection

The US3007 uses the MOSFET Rds-on as the sensing resistor to sense the MOSFET current and compares to a programmed voltage which is set externally via a resistor (Rcs) placed between the drain of the MOSFET and the "CS+" terminal of the IC as shown in the application circuit.

For example, if the desired current limit point is set to be 22A for the synchronous and 16A for the non synchronous , and from our previous selection, the maximum MOSFET Rds-on =19mW, then the current sense resistor Rcs is calculated as :
Vcore
Vcs=IcL*Rds=22*0.019=0.418V
Rcs=Vcs/Ib=(0.418V)/(200uA)=2.1kΩ
Where: Ib=200uA is the internal current setting of the US3007
3.3V supply
Vcs=IcL*Rds=16*0.019=0.3V
Rcs=Vcs/Ib=(0.3V)/(200uA)=1.50kΩ

1.5V, GTL+ Supply LDO Power MOSFET Selection

The first step in selectiong the power MOSFET for the 1.5V linear regulator is to select its maximum Rds-on of the pass transistor based on the input to output Dropout voltage and the maximum load current.
Rds(max)=(Vin - Vo)/IL
For Vo=1.5V, and Vin=3.3V , IL=2A
Rds-max=(3.3 - 1.5)/2= 0.9Ω
Note that since the MOSFETs Rds-on increases with temperature, this number must be divided by ≈ 1.5, inorder to find the Rds-on max at room temperature. The Motorola MTP3055VL has a maximum of 0.18Ω Rds-on at room temperature, which meets our requirement.
To select the heatsink for the LDO Mosfet the first step is to calculate the maximum power dissipation of the device and then follow the same procedure as for the switcher.
Pd = (Vin - Vo) * IL
Where :
Pd = Power Dissipation of the Linear Regulator
IL = Linear Regulator Load Current
For the 1.5V and 2A load:
Pd = (3.3 - 1.5)*2=3.6 W
Assuming Tj-max=125°C
Ts = Tj - Pd * (θjc + θcs)
Ts = 125 - 3.6 * (1.8 + 0.05) = 118 °C
With the maximum heat sink temperature calculated in the previous step, the Heat Sink to Air thermal resistance (θsa) is calculated as follows :
Assuming Ta=35 °C
ΔT = Ts - Ta = 118 - 35 = 83 °C Temperature Rise Above Ambient
θsa = ΔT/Pd
θsa = 83 / 3.6 = 23 °C/W

The same heat sink as the one selected for the switcher MOSFETs is also suitable for the 1.5V regulator.

2.5V, Clock Supply

The US3007 provides a complete 2.5V regulator with a minimum of 200mA current capability. The internal regulator has short circuit protection with internal thermal shutdown.

1.5V and 2.5V Supply Resistor Divider Selection

Since the internal voltage reference for the linear regulators is set at 1.26V for US3007, there is a need to use external resistor dividers to step up the voltage. The resistor dividers are selected using the following equations:
Vo=(1+Rt/Rb)*Vref
Where:
Rt=Top resistor divider
Rb=Bottom resistor divider
Vref=1.26V typical
For 1.5V supply :
Assuming Rb=1kΩ
Rt=Rb*[(Vo/Vref) - 1]
Rt=1*[(1.5/1.26) - 1]=191Ω
For 2.5V supply :
Assuming Rb=1.02kΩ
Rt=Rb*[(Vo/Vref) - 1]
Rt=1.02*[(2.5/1.26) - 1]=1kΩ

Switcher Output Voltage Adjust
Vcore
As it was discussed earlier,the trace resistance from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC regulation point when transitioninig from light load to full load and vice versa. To account for the DC drop, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the GND pin of the 3007 is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70 mV or 35mV higher than the DAC voltage setting. To do this, the top resistor of the resistor divider(R17 in the application circuit) is set at 100Ω, and the R19 is calculated. For example, if DAC voltage setting is for 2.8V and the desired output under light load is 2.835V, then R19 is calculated using the following formula :

R19= 100*{Vdac /(Vo - 1.004*Vdac)} [Ω]
R19= 100*{2.8 /(2.835 - 1.004*2.800)} = 11.76 kΩ
Select 11.8 kΩ , 1%
Note: The value of the top resistor must not exceed 100Ω. The bottom resistor can then be adjusted to raise the output voltage.

3.3V supply

The loop gain for the non synchronous switching regulator is intentionally set low to take advantage of the level shifting technique to reduce the number of output capacitors. Typically there is a 1% drop in the output voltage from light load (discontinous conduction mode) to full load (continous conduction mode) in the 3.3V supply. To account for this, the output voltage is set at 3.5V typically. The same procedure as for the synchronous is applied to the non synch with the exception that the internal voltage reference of this regulator is internally set at 2V. The following is the set of equations to use for the output voltage setting for the non-synchronous assuming the Vo=3.5V and the top resistor,(R2 in the application circuit) is; R2=75Ω. The bottom resistor, R3 is calculated as follows:
R3= R2*{2 /(Vo - 2)} [Ω]
R3= 75*{2 /(3.5 - 2)} = 100Ω , 1%
Note: The value of the top resistor , R2 must not exceed 100Ω.

Soft Start Capacitor Selection

The soft start capacitor must be selected such that during the start up when the output capacitors are charging up, the peak inductor current does not reach the current limit treshold. A minimum of 1uF capacitor insures this for most applications. An internal 10uA current source charges the soft start capacitor which slowly ramps up the inverting input of the PWM comparator Vfb3. This insures the output voltage to ramp at the same rate as the soft start cap thereby limiting the input current. For example, with 1uF and the 10uA internal current source the ramp up rate is ($\Delta V/\Delta t$)=I/C = 1V/100mS. Assuming that the output capacitance is 9000uF, the maximum start up current will be:
I=9000uF*(1V/100mS)=0.09A

Input Filter

It is highly recommended to place an inductor between the system 5V supply and the input capacitors of the switching regulator to isolate the 5V supply from the switching noise that occurs during the turn on and off of the switching components. Typically an inductor in the range of 1 to 3 uH will be sufficient in this type of application.

External Shutdown

The best way to shutdown the US3007 is to pull down on the soft start pin using an external small signal transistor such as 2N3904 or 2N7002 small signal MOSFET. This allows slow ramp up of the output, the same as the power up.

Layout Considerations

Switching regulators require careful attention to the layout of the components, specifically power components since they switch large currents. These switching components can create large amount of voltage spikes and high frequency harmonics if some of the critical components are far away from each other and are connected with inductive traces. The following is a guideline of how to place the critical components and the connections between them in order to minimize the above issues.
Start the layout by first placing the power components:

1) Place the input capacitors C3 and C14 and the high side mosfets ,Q1 and Q3 as close to their respective input caps as possible
2) Place the synchronous mosfet,Q4 and the Q3 as close to each other as possible with the intention that the source of Q3 and drain of the Q4 has the shortest length. Repeat this for the Q1 and D1 for the non synchronous.
3) Place the snubber R15 & C13 between Q4 & Q3. Repeat this for R1 and C4 with respect to the Q1 and D1 for the non synchronous.
4) Place the output inductor ,L3 and the output capacitors ,C16 between the mosfet and the load with output capacitors distributed along the slot 1 and close to it. Repeat this for L2 with respect to the C1 for the non synchronous.
5) Place the bypass capacitors, C8 and C19 right next to 12V and 5V pins. C8 next to the 12V, pin 28 and C19 next to the 5V, pin 11.
6) Place the US3007 such that the pwm output drives, pins 27 and 25 are relatively short distance from gates of Q3 and Q4. The non-synch MOSFET must also be situated such that the distance from its gate to the pin 1 of the US3007 is also relatively short.
7) Place all resistor dividers close to their respective feedback pins.
8) Place the 2.5V output capacitor, C18 close to the pin16 of the IC and the 1.5V output capacitor, C17 close to the Q2 MOSFET.

Note: It is better to place the 1.5V linear regulator components close to the 3007 and then run a trace from the output of the regulator to the load. However, if this is not possible then the trace from the linear drive output pin, pin 18 **must be run away from any high frequency data signals.**
It is critical, to place high frequency ceramic capacitors close to the clock chip and termination resistors to provide local bypassing.
9) Place R12 and C10 close to pin 23 and R9 and C5 close to pin 9.
10) Place C9 close to pin 12

Component connections:
Note : It is extremely important that no data bus should be passing through the switching regulator section specifically close to the fast transition nodes such as PWM drives or the inductor voltage.
Using the 4 layer board, dedicate on layer to GND, another layer as the power layer for the 5V, 3.3V, Vcore, 1.5V and if it is possible for the 2.5V.
Connect all grounds to the ground plane using direct vias to the ground plane.
Use large low inductance/low impedance plane to connect the following connections either using component side or the solder side.
a) C14 to Q3 Drain and C3 to Q1 drain
b) Q3 Source to Q4 Drain and Q1 Source to D1 cathode
c) Q4 drain to L3 and D1 cathode to L2
d) L3 to the output capacitors, C16 and L2 to the output capacitors, C1
e) C16 to the load, slot 1
f) Input filter L1 to the C16 and C3
g) C1 to Q2 drain
h) C17 to the Q2 source
I) A minimum of 0.2 inch width trace from the C18 capacitor to pin 16

Connect the rest of the components using the shortest connection possible