

### 4 BIT PROGRAMMABLE SYNCHRONOUS BUCK PLUS FOUR LDO CONTROLLER PRELIMINARY DATASHEET

#### **FFATURES**

- Provides Single Chip Solution for Vcore, GTL+,AGP Bus, 1.8V, 2.5V
- Automatic Voltage Selection for AGP slot's Vddq supply
- 4 Linear regulator controller on board to achieve lowest system cost solution
- Standby Vref provides reference for the ACPI regulators
- Designed to meet Intel Latest VRM specification for next generation microrocessors
- On board DAC programs the output voltage from 1.3V to 2.05V
- On board resistor dividers provides lowest component count
- Loss less Short Circuit Protection for all outputs
- Synchronous operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Soft Start
- High current totem pole driver for direct driving of the external Power MOSFET
- Power Good function Monitors all Outputs
- OVP Circuitry Protects the Switcher Output and generates a Fault output

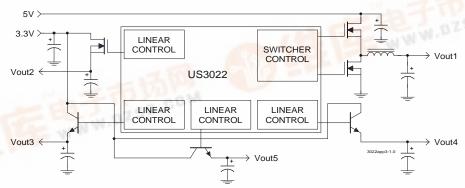
#### APPLICATIONS

 Total Power Soloution for Next Generation Intel Processor application

#### DESCRIPTION

The US3022 is the first controller IC with five controller in one package specifically designed to meet Intel specification for next generation microprocessor applications requiring multiple on board regulators. The US3022 provides a single chip controller IC for the Vcore, 4 LDO controllers, one with the automatic select pin that connects to the TYPE DETECT pin of the AGP slot for the AGP Vddg supply, one for GTL+, the other for the 1.8V chip set regulator as well as 2.5V for the clock as required for the next generation PC applications. The US3022 typically uses Bipolar transistors for Vout3(1.5V) and Vout4(1.8V) and Vout5 however if Vaux pin is connected to 12V, then MOSFETs can also be used as external pass elements. No external resistor divider is necessary for any of the regulators. The switching regulator feature a patented topology that in combination with a few external components as shown in the typical application circuit, will provide well in excess of 20A of output current for an on-board DC/DC converter while automatically providing the right output voltage via the 5 bit internal DAC .The US3022 also features, loss less current sensing for both switcher by using the Rds-on of the high side Power MOSFET as the sensing resistor, an output under voltage shutdown that detects short circuit condition for the linear outputs and latches the system off, and a Power Good window comparator that switches its open collector output low when any one of the outputs is outside of a pre programmed window.

#### TYPICAL APPLICATION



# PACKAGE ORDER INFORMATION

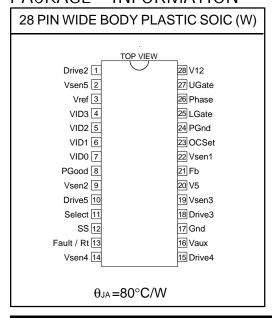
Ta (°C)	Device	Package
0 TO 70	US3022CW	28 pin Plastic SOIC WB

### ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range .....-65 TO 150°C

Operating Junction Temperature Range ....... 0 TO 125°C

### PACKAGE INFORMATION



### **ELECTRICAL SPECIFICATIONS**

Unless otherwise specified ,these specifications apply over ,V12 = 12V, V5 = 5V and Ta=0 to  $70^{\circ}$ C. Typical values refer to Ta =25°C. Low duty cycle pulse testing are used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply UVLO Section						
UVLO Threshold-12V		Supply ramping up		10		V
UVLO Hysterises-12V				0.6		V
UVLO Threshold-5V		Supply ramping up		4.4		V
UVLO Hysterises-5V				0.3		V
Supply Current						
Operating Supply Current						
		V12		6		mA
		V5		30		

Switching Controllers; Vcore (Vsen 1) and AGP (Vsen 2)

VID Section (vcore only)					
DAC output voltage (note 1)		0.99Vs	Vs	1.01Vs	V
DAC Output Line Regulation			0.1		%
DAC Output Temp Variation			0.5		%
VID Input LO				0.8	V
VID Input HI		2			V
VID input internal pull-up					
resistor to V5			27		kΩ
Vsen2 Voltage	Select<0.8V		1.5		V
<u>,                                      </u>	Select>2V		3.3		V

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			<u> </u>			
Error Comparator Section						
Input bias current					2	uA
Input Offset Voltage			-2		+2	mV
Delay to Output		Vdiff=10mV			100	nS
Current Limit Section						
C.S Threshold Set Current				200		uA
C.S Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css=0.1 uF		10		%
Output Drivers Section						
Rise Time		CL=3000pF		70		nS
Fall Time		CL=3000pF		70		nS
Dead band Time Between						
High side and Synch Drive						
(Vcore Switcher Only)		CL=3000pF		200		nS
Oscillator Section (internal)						<del>                                     </del>
Osc Frequency		Rt=Open		217		Khz
1.8V Regulator (Vsen 4)						
Vsense Voltage	Vo4	Ta=25, Drive4 = Vsen4		1.800		V
Vsense Voltage		10. 20, 2		1.800		V
Input bias current				11000	2	uA
Output Drive Current		Vaux-Vdrive>0.6V	50			mA
Calpat Billo Carroll		vaax vanvos o.ov				1117
1.5V Regulator (Vsen 3)						
Vsense Voltage	Vo3	Ta=25, Drive3 = Vsen3		1.500		V
Vsense Voltage		•		1.500		V
Input bias current					2	uA
Output Drive Current		Vaux-Vdrive>0.6V	50			mA
2.5V Regulator (Vsen 5)						
Vsense Voltage	Vo5	Ta=25, Drive5 = Vsen5		2.500		V
Vsense Voltage				2.500		V
Input bias current					2	uA
Output Drive Current		Vaux-Vdrive>0.6V	50			mA
Power Good Section						
Vsen1 UV lower trip point		Vsen1 ramping down		0.90Vs		V
Vsen1 UV upper trip point		Vsen1 ramping up		0.92Vs		V
Vsen1 UV Hysterises				.02Vs		V
Vsen1 HV upper trip point		Vsen1 ramping up		1.10Vs		V
Vsen1 HV lower trip point		Vsen1 ramping down		1.08Vs		V
Vsen1 HV Hysterises				.02Vs		V
Vsen2 trip point		Select<0.8V		1.100		V
т ост т.р р ст. т.		Select>2V		2.560		V
Vsen4 trip point			1	1.320		V
Vsen3 trip point				1.140		V
Vsen5 trip point			1	1.875		<del>  v</del>
Power Good Output LO		RL=3mA		0.4		T V
Power Good Output HI		RL=5K pull up to 5V		4.8		T V
Fault (Overvoltage) Section		.tz=ort pail up to ov		1.0		† •
Core O.V. upper trip point		Vsen1 ramping up		1.17Vs		V
Core O.V. lower trip point		Vsen1 ramping down		1.17 VS		V
FAULT Output HI		lo=3mA		10		V
Soft Start Section		IO-OHIA		10		V
Soft Start Current		OCset=0V , Phase=5V	1	20		uA
Joh Start Current		OGSEL-UV, FIIASE=3V		20		<u> un</u>

Note 1: Vs refers to the set point voltage given in Table 1.

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Vref Section						
Vref Initial Accuracy		No Load,Ta=25	1.980	2.000	2.020	V
Vref Initial Accuracy		No Load, Over Temp	1.960	2.000	2.040	V
Vref Change with Load		No Load to 30K load	-2			%
Vref Output Impedance			150	300	600	Ohm

VID3	VID2	VID1	VID0	Vs
1	1	1	1	1.30
1	1	1	0	1.35
1	1	0	1	1.40
1	1	0	0	1.45
1	0	1	1	1.50
1	0	1	0	1.55
1	0	0	1	1.60
1	0	0	0	1.65
0	1	1	1	1.70
0	1	1	0	1.75
0	1	0	1	1.80
0	1	0	0	1.85
0	0	1	1	1.90
0	0	1	0	1.95
0	0	0	1	2.00
0	0	0	0	2.05

Table 1 - Set point voltage vs. VID codes

5	5 = 6 6 5 1 5 = 1	
PIN	DESCRIPTION	ONS
PIN#	PIN SYMBOL	Pin Description
7	VID0	LSB input to the DAC that programs the output voltage. This pin is TTL compatible that
		realizes a logic "1" as either HI or Open. When left open, his pin is pulled up internally by
		a $27k\Omega$ resistor to 5V supply.
6	VID1	Input to the DAC that programs the output voltage. This pin is TTL compatible that real-
		izes a logic "1" as either HI or Open. When left open, his pin is pulled up internally by a
		27k $Ω$ resistor to 5V supply.
5	VID2	Input to the DAC that programs the output voltage. This pin is TTL compatible that real-
		izes a logic "1" as either HI or Open. When left open, his pin is pulled up internally by a
		27k $Ω$ resistor to 5V supply.
4	VID3	MSB input to the DAC that programs the output voltage. This pin is TTL compatible that
		realizes a logic "1" as either HI or Open. When left open, his pin is pulled up internally by
		a 27kΩ resistor to 5V supply.
3	Vref	This pin provides a 2V reference that remains on when the 5V pin is connected to the 5V
		standby of the ATX supply. In this application, the Vref pin is used to provide reference for
		the ACPI regulators.
8	PGOOD	This pip is an approach set or output that quitched LO when any of the autputs are outpide
0	PGOOD	This pin is an open collector output that switches LO when any of the outputs are outside
		of the specified under voltage trip point. It also switches low when Vsen1 pin is more than 10% above the DAC voltage setting.
21	FB	This pin provides the feedback for the synchronous switching regulator. Typically this pin
۷١	10	can be connected directly to the output of the switching regulator. However, a resistor
		divider is recommended to be connected from this pin to vout1 and GND to adjust the
		output voltage for any drop in the output voltage that is caused by the trace resistance.
		The value of the resistor connected from Vout1 to FB1 must be less than $1000\Omega$ .
1	Drive2	This pin controls the gate of an external MOSFET for the AGP linear regulator.
10	Drive5	This pin controls the gate of an external transistor for the 2.5V Clock linear regulator.

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PIN#	PIN SYMBOL	Pin Description
22	Vsen1	This pin is internally connected to the undervoltage and overvoltage comparators sensing
		the Vcore status. It must be connected directly to the Vcore supply.
9	Vsen2	This pin provides the feedback for the AGP linear regulator. The Select pin when con-
		nected to the "Type Detect" pin of the AGP slot automatically selects the right voltage for
		the AGP Vddq.
15	Drive4	This pin controls the gate of an external MOSFET for the 1.8V chip set linear regulator.
23	OCSET	This pin is connected to the Drain of the power MOSFET of the Core supply and it
		provides the positive sensing for the internal current sensing circuitry. An external resis-
		tor programs the C.S threshold depending on the Rds of the power MOSFET. An external
		capacitor is placed in parallel with the programming resistor to provide high frequency
		noise filtering.
26	PHASE	This pin is connected to the Source of the power MOSFET for the Core supply and it
		provides the negative sensing for the internal current sensing circuitry.
12	SS	This pin provides the soft start for all the regulators. An internal current source charges
		an external capacitor that is connected from this pin to GND which ramps up the outputs
		of the regulators, preventing the outputs from overshooting as well as limiting the input
		current. The second function of the Soft Start cap is to provide long off time (HICCUP) for
		the synchronous MOSFET during current limiting.
13	FAULT/Rt	This pin has dual function. It acts as an output of the OVP circuitry or it can be used to
		program the frequency using an external resistor. When used as a fault detector, if any
		of the switcher outputs exceed the OVP trip point, the FAULT pin switches to 12V and
		the soft start cap is discharged. If the FAULT pin is to be connected to any external
		circuitry, it needs to be buffered.
18	Drive3	This pin controls the gate of an external transistor for the 1.5V GTL+ linear regulator.
19	Vsen3	This pin provides the feedback for the linear regulator that its output drive is Drive3.
16	Vaux	This pin is normally connected to 3.3V or 5V input. When connected to the 12V supply,
		it provides gate drive voltage for the # 3, #4 and #5 (Drive 3,4,5) linear regulator's pass
44	\/a = = 4	transistors in case MOSFET transistors are being used instead of Bipolars.
14 17	Vsen4 GND	This pin provides the feedback for the linear regulator that its output drive is Drive4.  This pin serves as the ground pin and must be connected directly to the ground plane.
24	PGND	This pin serves as the Power ground pin and must be connected directly to the ground pin and must be connected directly to the GND
24	FGND	plane close to the source of the synchronous MOSFET. A high frequency capacitor
		(typically 1 uF) must be connected from V12 pin to this pin for noise free operation.
25	LGATE	Output driver for the synchronous power MOSFET for the Core supply.
27	UGATE	Output driver for the high side power MOSFET for the Core supply.
28	V12	This pin is connected to the 12 V supply and serves as the power Vcc pin for the output
20	V 12	drivers. A high frequency capacitor (typically 1 uF) must be placed close to this pin and
		PGND pin and be connected directly from this pin to the GND plane for the noise free
		operation.
20	V5	5V supply voltage. A high frequency capacitor (0.1 to 1 uF) must be placed close to this
-	-	pin and connected from this pin to the GND plane for noise free operation.
11	Select	This pin provides automatic voltage selection for the AGP switching regulator. When it is
		pulled LO, the voltage is 1.5V and when left open or pulled to HI, the voltage is 3.3V.
2	Vsen5	This pin provides the feedback for the linear regulator that its output drive is Drive5.

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# **BLOCK DIAGRAM**

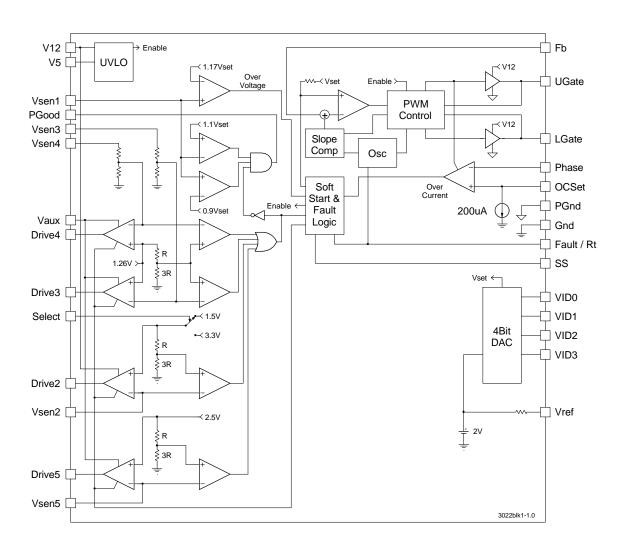


Figure 1 - Simplified block diagram of the US3022.

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# TYPICAL APPLICATION

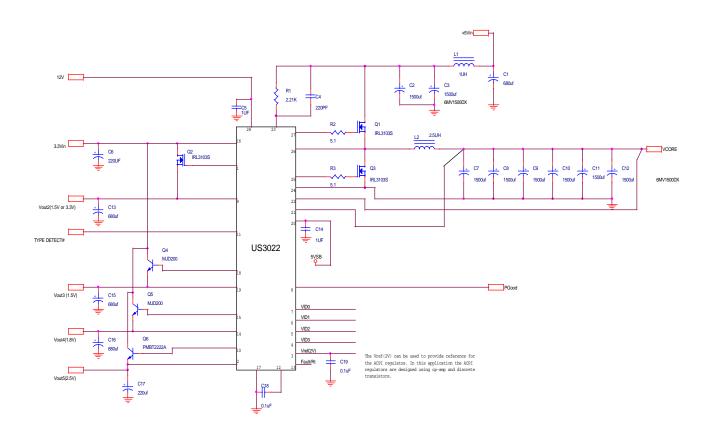


Figure 2 - Typical application of US3022 for an on board DC-DC converter providing power for the Vcore, GTL+, 1.8V chip set supply, 2.5V clock supply as well as auto select AGP supply for the next generation PC applications.