

UTRON

UT611024

Rev 1.3

128K X 8 BIT HIGH SPEED CMOS SRAM

**FEATURES**

- Fast access time : 10/12/15 ns (max.)
- Low operating power consumption : 100 mA (typical)
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Package : 32-pin 300 mil skinny PDIP  
32-pin 300 mil SOJ  
32-pin 8 x 20mm TSOP-1  
32-pin 8 x 13.4mm STSOP

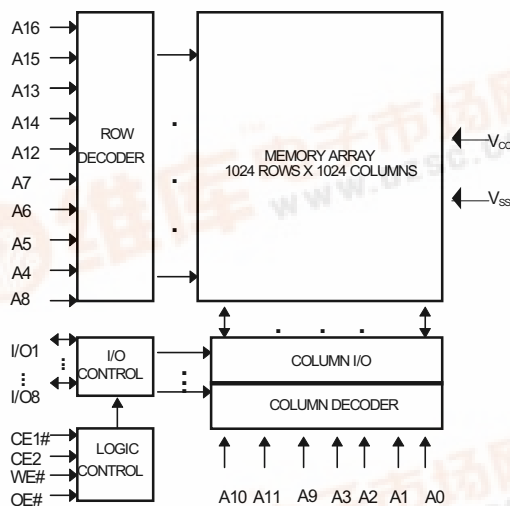
**GENERAL DESCRIPTION**

The UT611024 is a 1,048,576-bit high-speed CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

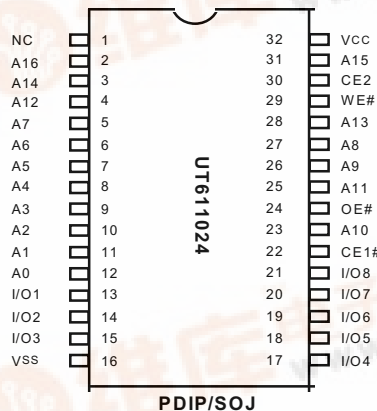
The UT611024 is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT611024 operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

**FUNCTIONAL BLOCK DIAGRAM**

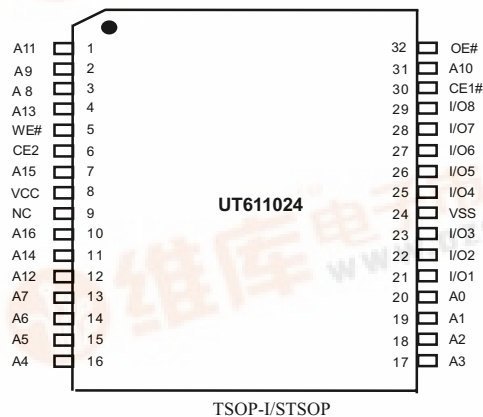


**PIN CONFIGURATION**



**PIN DESCRIPTION**

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
CE1#,CE2	Chip Enable 1, 2 Inputs
WE#	Write Enable Input
OE#	Output Enable Input
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground
NC	No Connection





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ABSOLUTE MAXIMUM RATINGS\*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	VTERM	-0.5 to +7.0	V
Operating Temperature	TA	0 to +70	°C
Storage Temperature	TSTG	-65 to +150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	IOUT	50	mA
Soldering Temperature (under 10 sec)	Tsolder	260	°C

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

This

is a stress rating only and functional operation of the device or any other conditions above those indicated in the

operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for

extended period may affect device reliability.

TRUTH TABLE

MODE	CE1#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	ISB, ISB1
Standby	X	L	X	X	High - Z	ISB, ISB1
Output Disable	L	H	H	H	High - Z	ICC
Read	L	H	L	H	DOUT	ICC
Write	L	H	X	L	DIN	ICC

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (VCC = 5V±10%, TA = 0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	
Input High Voltage	V <sub>IH</sub>		2.2	VCC+0.5	V	
Input Low Voltage	V <sub>IL</sub>		- 0.5	0.8	V	
Input Leakage Current	I <sub>LI</sub>	VSS ≤ V <sub>IN</sub> ≤ VCC	- 1	1	μA	
Output Leakage Current	I <sub>LO</sub>	VSS ≤ V <sub>I/O</sub> ≤ VCC CE1# = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or OE# = V <sub>IH</sub> or WE# = V <sub>IL</sub>	- 1	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = - 4mA	2.4	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8mA	-	0.4	V	
Operating Power Supply Current	ICC	CE1# = V <sub>IL</sub> , CE2 = V <sub>IH</sub> I <sub>I/O</sub> = 0mA, Cycle=Min.	- 10	-	180	mA
			- 12	-	160	mA
			- 15	-	140	mA
Standby Power Supply Current	ISB	CE1# = V <sub>IH</sub> or CE2 = V <sub>IL</sub>	-	30	mA	
	ISB1	CE1# ≥ VCC-0.2V or CE2 ≤ 0.2V	-	5	mA	

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**128K X 8 BIT HIGH SPEED CMOS SRAM****CAPACITANCE (TA=25°C, f=1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	CIN	-	8	pF
Input/Output Capacitance	CI/O	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> =30pF, I <sub>OH</sub> /I <sub>OL</sub> =-4mA/8mA

**AC ELECTRICAL CHARACTERISTICS (VCC = 5V±10% , TA = 0°C to 70°C)****(1) READ CYCLE**

PARAMETER	SYMBOL	UT611024-10		UT611024-12		UT611024-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	10	-	12	-	15	-	ns
Address Access Time	t <sub>AA</sub>	-	10	-	12	-	15	ns
Chip Enable Access Time	t <sub>ACE1</sub> , t <sub>ACE1</sub>	-	10	-	12	-	15	ns
Output Enable Access Time	t <sub>OE</sub>	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	t <sub>CLZ1*</sub> , t <sub>CLZ2*</sub>	2	-	3	-	4	-	ns
Output Enable to Output in Low Z	t <sub>OLZ*</sub>	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t <sub>CHZ1*</sub> , t <sub>CHZ2*</sub>	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t <sub>OHZ*</sub>	-	5	-	6	-	7	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	3	-	ns

**(2) WRITE CYCLE**

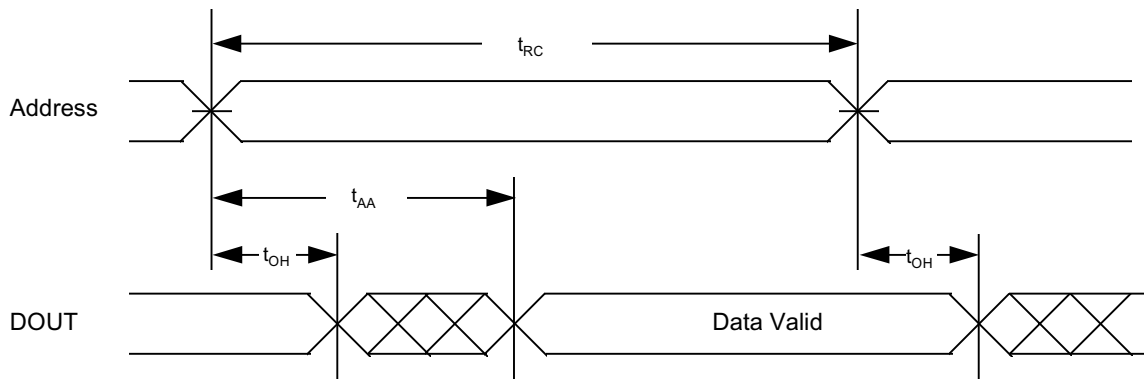
PARAMETER	SYMBOL	UT611024-10		UT611024-12		UT611024-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	10	-	12	-	15	-	ns
Address Valid to End of Write	t <sub>AW</sub>	8	-	10	-	12	-	ns
Chip Enable to End of Write	t <sub>CW1</sub> , t <sub>CW2</sub>	8	-	10	-	12	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	8	-	9	-	10	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	0	-	ns
Output Active from End of Write	t <sub>OW*</sub>	2	-	3	-	4	-	ns
Write to Output in High Z	t <sub>WHZ*</sub>	-	6	-	7	-	8	ns

\*These parameters are guaranteed by device characterization, but not production tested.

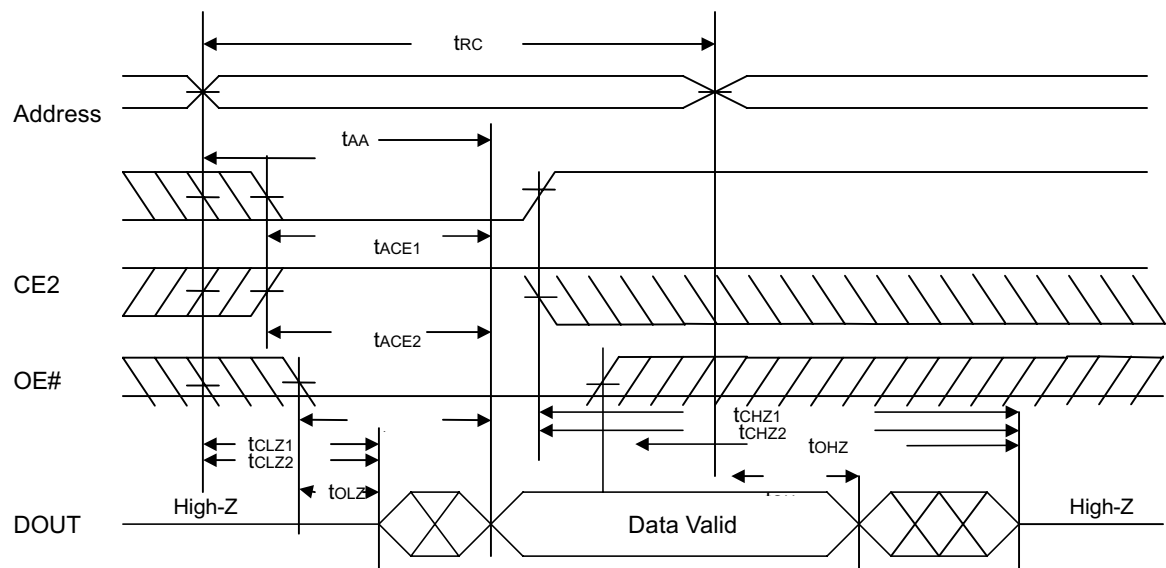


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 (CE#, CE2 and OE# Controlled) (1,3,5,6)

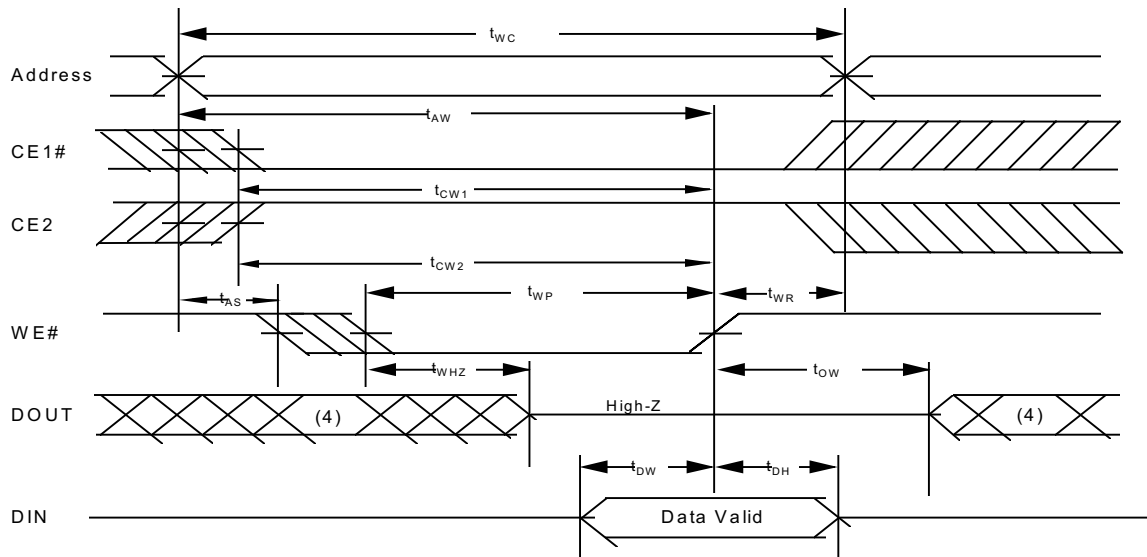


Notes :

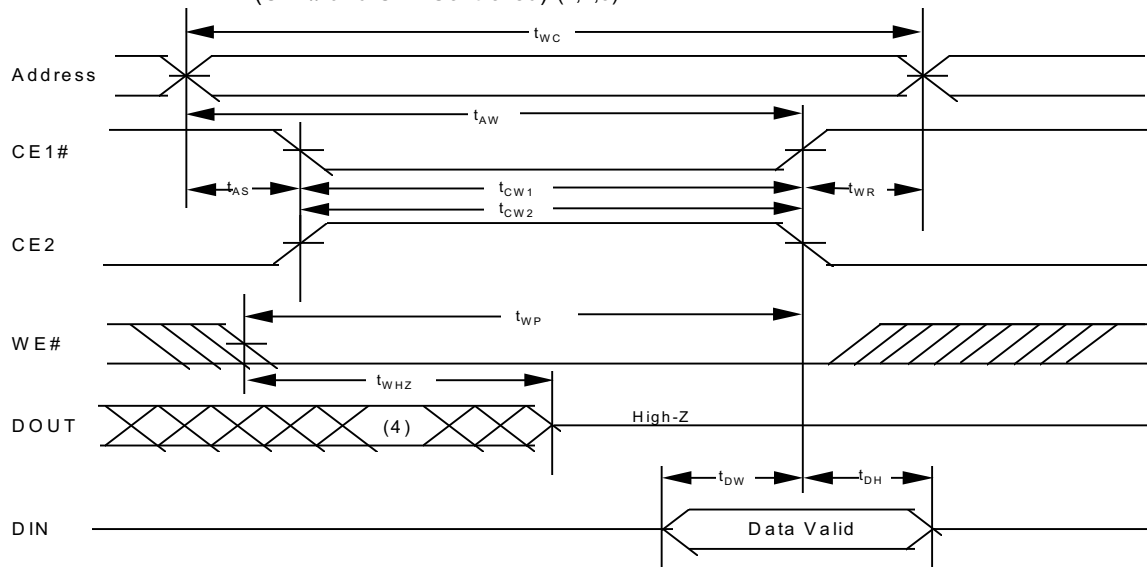
1. WE# is HIGH for read cycle.
2. Device is continuously selected CE1#=V<sub>IL</sub> and CE2=V<sub>IH</sub>.
3. Address must be valid prior to or coincident with CE1# and CE2 transition; otherwise  $t_{AA}$  is the limiting parameter.
4. OE# is low.
5.  $t_{CLZ1}$ ,  $t_{CLZ2}$ ,  $t_{OLZ}$ ,  $t_{CHZ1}$ ,  $t_{CHZ2}$  and  $t_{OHZ}$  are specified with  $C_L=5pF$ . Transition is measured  $\pm 500mV$  from steady state.
6. At any given temperature and voltage condition,  $t_{CHZ1}$  is less than  $t_{CLZ1}$ ,  $t_{CHZ2}$  is less than  $t_{CLZ2}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .



WRITE CYCLE 1 (WE# Controlled) (1,2,3,5)



WRITE CYCLE 2 (CE1# and CE2 Controlled) (1,2,5)



Notes :

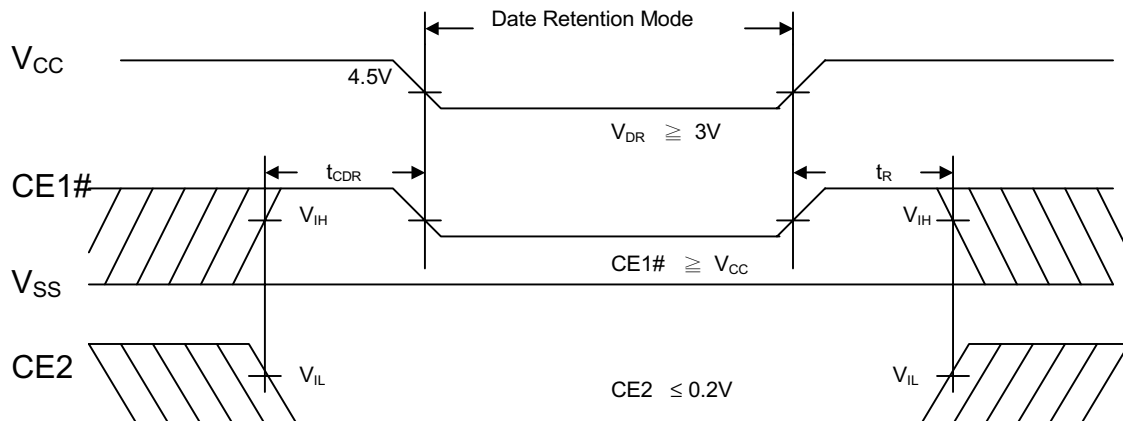
1. WE# or CE# must be HIGH during all address transitions.
2. A write occurs during the overlap of a low CE# and a low WE#.
3. During a WE# controlled with write cycle with OE# LOW,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# LOW transition occurs simultaneously with or after WE# LOW transition, the outputs remain in a high impedance state.
6.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.



**DATA RETENTION CHARACTERISTICS (TA = 0°C to 70°C)**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	$V_{DR}$	$CE1\# \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$	3	-	5.5	V
Data Retention Current	$I_{DR}$	$V_{CC}=3V$ $CE1\# \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$	-	-	3	mA
Chip Disable to Data Retention Time	$t_{CDR}$	See Data Retenti Waveforms (below)	0	-	-	ns
Recovery Time	$t_R$		3	-	-	ns

**DATA RETENTION WAVEFORM**





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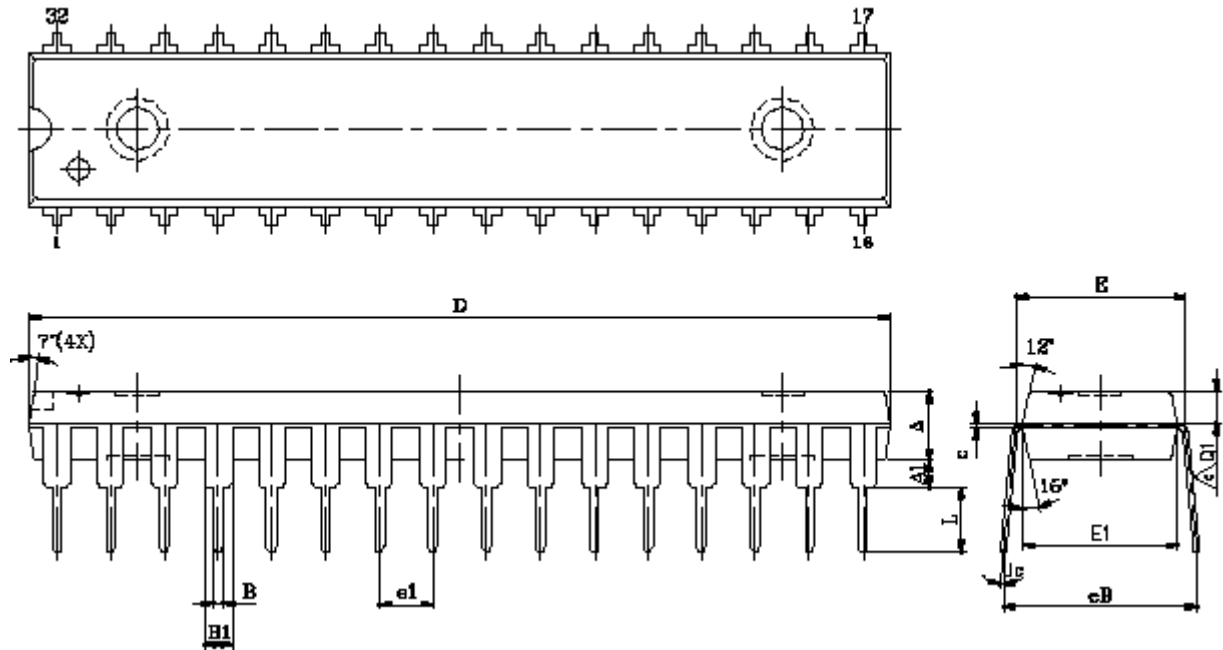
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PACKAGE OUTLINE DIMENSION

32 PIN P-DIP (300MIL) PACKAGE OUTLINE DIMENSION



UNIT SYMBOL	INCH(BASE)	MM(REF)
A	0.130 ±0.005	3.302 ±0.127
A1	0.015(MIN)	0.381 (MIN)
B	0.018 ±0.004	0.457 ±0.102
B1	0.050 ±0.008	1.270 ±0.203
c	0.010 ±0.004	0.254 ±0.102
D	1.600 ±0.005	40.640 ±0.127
E	0.315 ±0.010	8.001 ±0.254
E1	0.288 ±0.004	7.315 ±0.102
e1	0.100 TYP	2.540 TYP
eB	0.350 ±0.020	8.890 ±0.508
L	0.125 (MIN)	3.175 (MIN)
Q1	0.060 ±0.005	1.524 ±0.127
1c	0°~10°	0°~10°



Note :

1. All EDGE WITH MATTE FINISH.
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION.



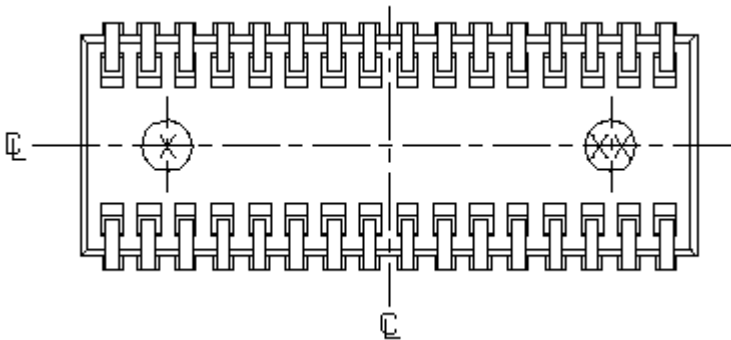
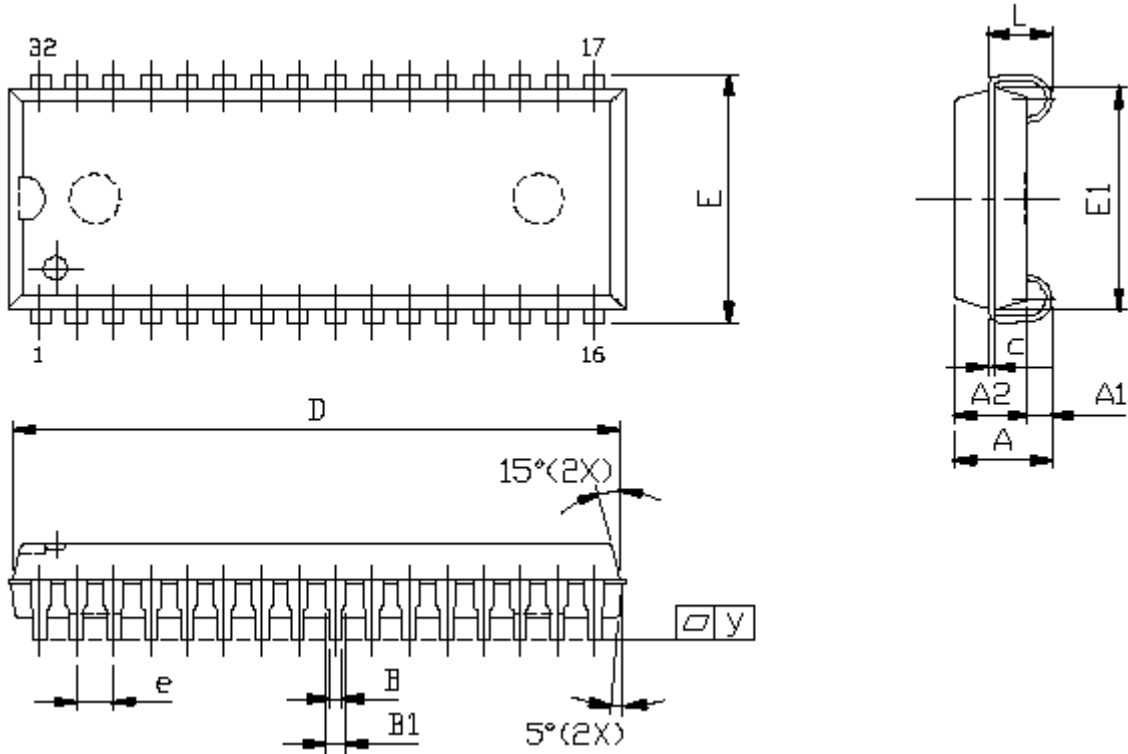
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32PIN SOJ PACKAGE OUTLINE DIMENSION



SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.148 (MAX)	3.759 (MAX)
A1		0.026 (MIN)	0.660 (MIN)
A2		0.100 ±0.005	2.540 ±0.127
B		0.018 (TYP)	0.457(TYP)
B1		0.028 (TYP)	0.711 (TYP)
C		0.010 (TYP)	0.254 (TYP)
D		0.830 (MAX)	21.082 (MAX)
E		0.335 (TYP)	8.509 (TYP)
E1		0.300 ±0.005	7.620 ±0.127
e		0.050 (TYP)	1.270 (TYP)
L		0.086 ±0.010	2.184 ±0.254
y		0.003 (MAX)	0.076 (MAX)







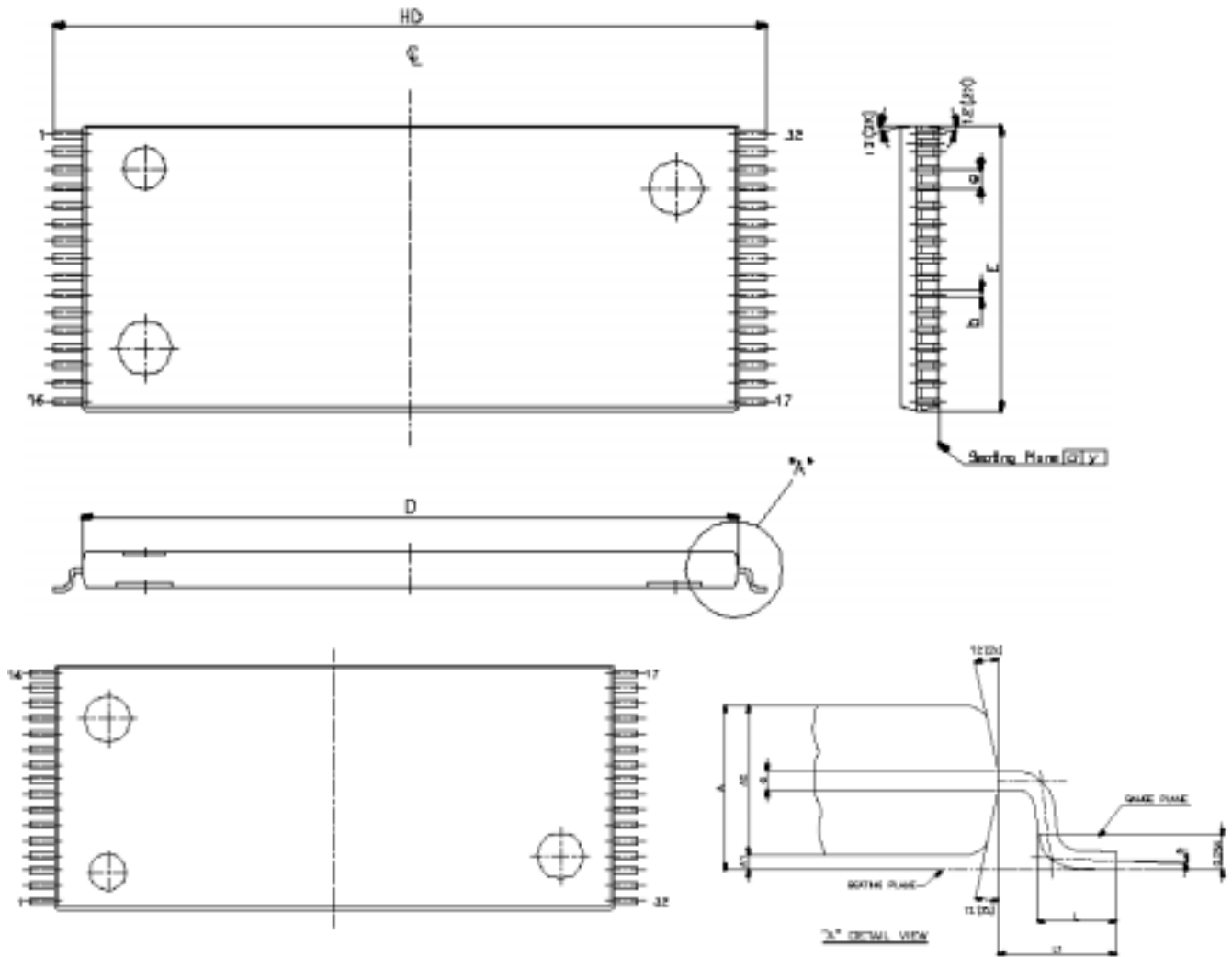
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32PIN TSOP-I PACKAGE OUTLINE DIMENSION



NOTE: 1. L/F MT'L: ALLOY

SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004 ±0.002	0.10 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.008 + 0.002 - 0.001	0.20 + 0.05 - 0.03
c		0.005 (TYP)	0.127 (TYP)
D		0.724 ±0.004	18.40 ±0.10
E		0.315 ±0.004	8.00 ±0.10
e		0.020 (TYP)	0.50 (TYP)
HD		0.787 ±0.008	20.00 ±0.20
L		0.0197 ±0.004	0.50 ±0.10
L1		0.0315 ±0.004	0.08 ±0.10
y		0.003 (MAX)	0.076 (MAX)
θ		0°~5°	0°~5°



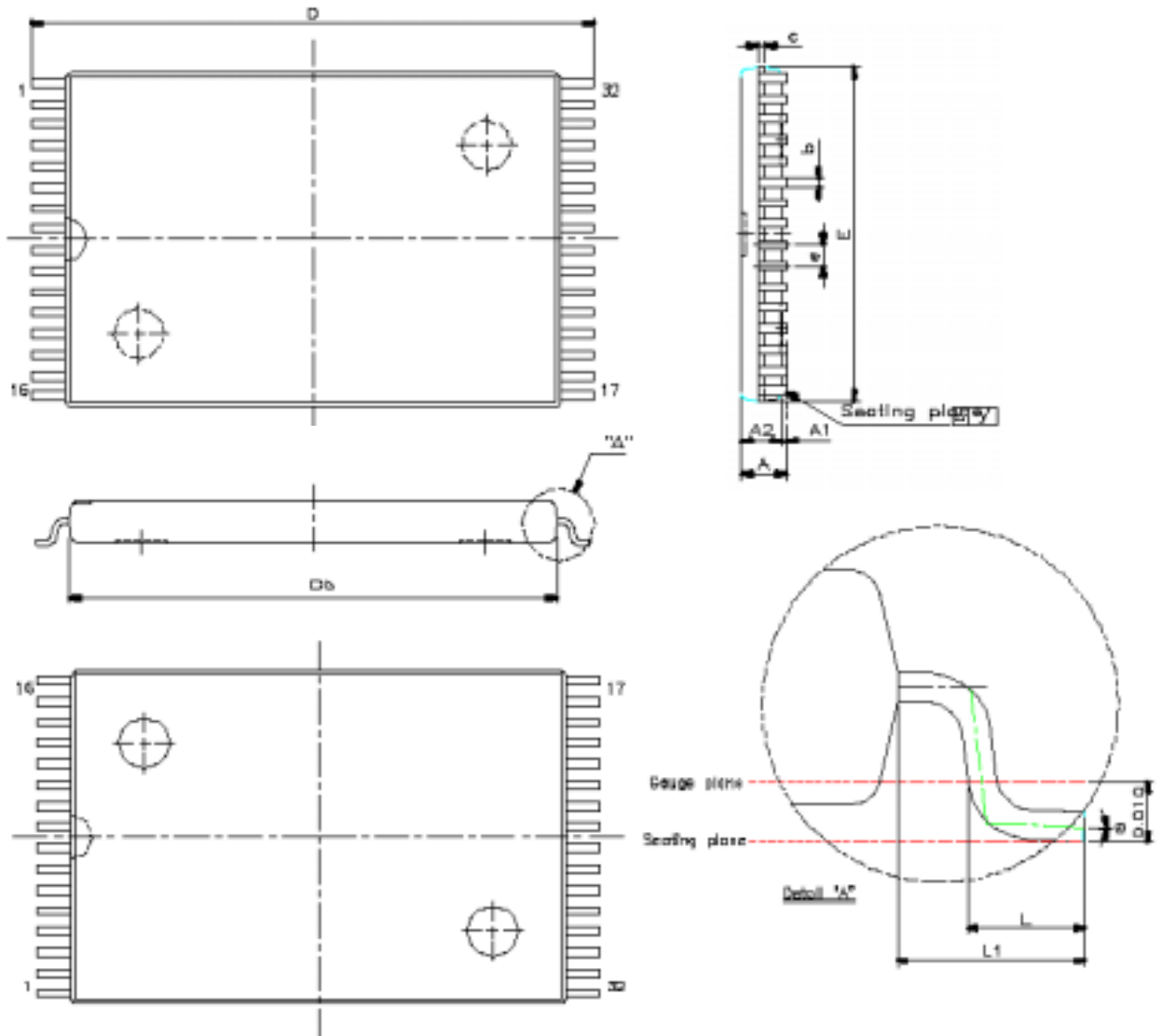
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32PIN 8mm x 13.4mm STSOP PACKAGE OUTLINE DIMENSION



SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		1.20(Max.)	0.047(Max.)
A1		0.10 ± 0.05	0.004 ± 0.002
A2		1.00 ± 0.05	0.039 ± 0.002
b		0.20(typ.)	0.006(typ.)
c		0.15(typ.)	0.006(typ.)
D		13.40 ± 0.20	0.526 ± 0.006
Db		11.80 ± 0.10	0.465 ± 0.004
E		8.000 ± 0.10	0.315 ± 0.004
e		0.50(typ.)	0.020(typ.)
L		0.50 ± 0.10	0.020 ± 0.004
L1		0.80 ± 0.10	0.0315 ± 0.004
y		0.08(Max.)	0.003(Max.)
e		0°~5°	0°~5°

Note :

E dimension is not including End flash.

The total of both sides' end flash is not above 0.3mm.



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**ORDERING INFORMATION**

<b>PART NO.</b>	<b>ACCESS TIME (ns)</b>	<b>PACKAGE</b>
UT611024KC-15	12	32PIN SKINNY PDIP
UT611024KC-15	15	32PIN SKINNY PDIP
UT611024JC-10	10	32PIN SOJ
UT611024JC-12	12	32PIN SOJ
UT611024JC-15	15	32PIN SOJ
UT611024LC-10	10	32PIN TSOP-1
UT611024LC-12	12	32PIN TSOP-1
UT611024LC-15	15	32PIN TSOP-1
UT611024LS-10	10	32PIN STSOP
UT611024LS-12	12	32PIN STSOP
UT611024LS-15	15	32PIN STSOP