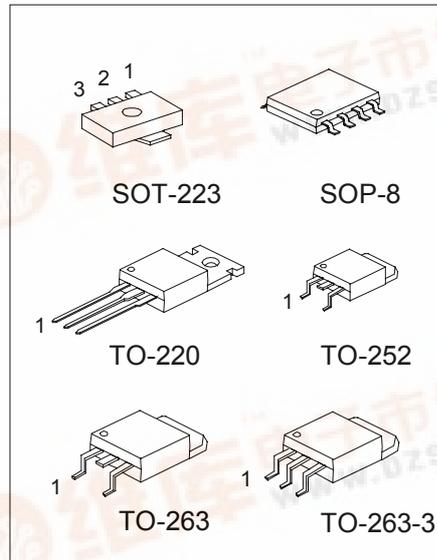


UTCLD1117/A LINEAR INTEGRATED CIRCUIT

LOW DROP FIXED AND ADJUSTABLE POSITIVE VOLTAGE REGULATORS

DESCRIPTION

The UTC LD1117/A is a LOW DROP Voltage Regulator able to provide up to 0.8/1.0A of Output Current, available even in adjustable version ($V_{ref}=1.25V$). Concerning fixed versions, are offered the following Output Voltages: 1.8V, 2.5V, 2.85V, 3.0V, 3.3V and 5.0V. The 2.85V type is ideal for SCSI-2 lines active termination. The device is supplied in: SOT-223, TO-252, TO-263, TO-263-3, SOP-8 and TO-220. The SOT-223, TO-263, TO-263-3 and TO-252 surface mount packages optimize the thermal characteristics even offering a relevant space saving effect. High efficiency is assured by NPN pass transistor. In fact in the case, unlike than PNP one, the Quiescent Current flows mostly into the load. Only a very common $10\mu F$ minimum capacitor is needed for stability. On chip trimming allows the regulator to reach a very tight output voltage tolerance, within $\pm 1\%$ at $25^{\circ}C$. The ADJUSTABLE LD1117/A is pin to pin compatible with the other standard Adjustable voltage regulators maintaining the better performances in terms of Drop and Tolerance.



SOP-8 1: GND; 2,3,6,7: Vout;
4: Vin; 5,8: NC

FEATURES

- *Low dropout voltage (1V Typ.)
- *2.85V device performances are suitable for SCSI-2 active termination
- *Output current up to 0.8/1.0A
- *Fixed output voltage of: 1.8V, 2.5V, 2.85V, 3.0V, 3.3V, 5.0V
- *Adjustable version availability ($V_{ref}=1.25V$)
- *Internal current and thermal limit
- *Available in $\pm 1\%$ (at $25^{\circ}C$) and 2% in all temperature range
- *Supply voltage rejection: 75dB (TYP)
- *Temperature range: $0^{\circ}C$ to $125^{\circ}C$



UTCLD1117/A LINEAR INTEGRATED CIRCUIT

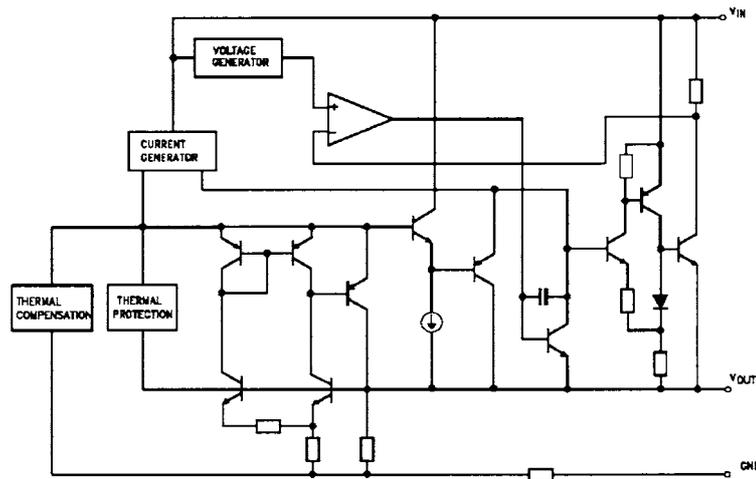
MARKING INFORMATION

PACKAGE	VOLTAGE CODE	PIN CODE	PIN 1	PIN 2	PIN 3	MARKING
SOT-223	18:1.8V	A	GND	OUT	IN	
	25:2.5V	B	OUT	GND	IN	
	28:2.85V	C	GND	IN	OUT	
	30:3.0V	D	IN	GND	OUT	
	33:3.3V					
50:5.0V						
TO-220 TO-252 TO-263 TO-263-3	AD:ADJ	A	GND	OUT	IN	
		B	OUT	GND	IN	
		C	GND	IN	OUT	
		D	IN	GND	OUT	

Note: The current code "A" means output current up to 1.0A, while without "A" means output current up to 0.8A.

UTCLD1117/A LINEAR INTEGRATED CIRCUIT

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
DC Input Voltage	V _{IN}	15	V
Power Dissipation	P _{tot}	12	W
Storage temperature	T _{stg}	-65 ~ +150	°C
Operating Junction Temperature	T _{op}	0 ~ +125	°C

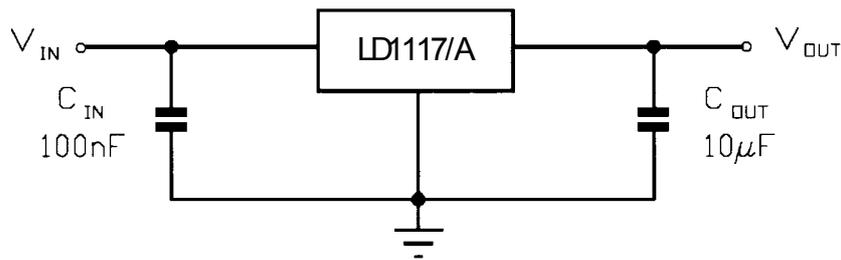
Note: Absolute Maximum Ratings are those value beyond which damage to the device may occur. Functional operation under there condition is not implied. Over the above suggested Max Power Dissipation a Short Circuit could definitively damage the device.

THERMAL DATA

PARAMETER	SYMBOL	VALUE	UNIT
Thermal Resistance Junction-case	R _{th-case}		
SOT-223		15	°C/W
SOP-8		20	°C/W
TO-252		8	°C/W
TO-220		3	°C/W
TO-263		3	°C/W
Thermal Resistance Junction-ambient	R _{thj-amb}		
TO-220		50	°C/W

UTCLD1117/A LINEAR INTEGRATED CIRCUIT

APPLICATION CIRCUIT



UTC LD1117/A-1.8 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, $T_j=0$ to 125°C , $C_o=10\mu\text{F}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_o	$V_{in}=3.8\text{V}$, $I_o=10\text{mA}$, $T_j=25^\circ\text{C}$	1.780	1.800	1.820	V
Output Voltage	V_o	$I_o=0$ to $800/1000\text{mA}$, $V_{in}=3.3$ to 8V	1.760		1.840	V
Line Regulation	ΔV_o	$V_{in}=3.3$ to 8V , $I_o=0\text{mA}$		1	6	mV
Load Regulation	ΔV_o	$V_{in}=3.3\text{V}$, $I_o=0$ to $800/1000\text{mA}$		1	10	mV
Temperature stability	ΔV_o			0.5		%
Long Term Stability	ΔV_o	1000 hrs, $T_j=125^\circ\text{C}$		0.3		%
Operating Input Voltage	V_{in}	$I_o=100\text{mA}$			10	V
Quiescent Current	I_d	$V_{in}\leq 8\text{V}$		5	10	mA
Output Current	I_o	$V_{in}=6.8\text{V}$, $T_j=25^\circ\text{C}$	800	950	1200	mA
Output Noise Voltage	eN	$B=10\text{Hz}$ to 10KHz , $T_j=25^\circ\text{C}$		100		μV
Supply Voltage Rejection	SVR	$I_o=40\text{mA}$, $f=120\text{Hz}$, $T_j=25^\circ\text{C}$, $V_{in}=5.5\text{V}$, $V_{\text{ripple}}=1\text{Vpp}$	60	75		dB
Dropout Voltage	V_d	$I_o=100\text{mA}$		1.00	1.10	V
		$I_o=500\text{mA}$		1.05	1.15	V
		$I_o=800\text{mA}$		1.10	1.20	V
		$I_o=1000\text{mA}$		1.15	1.25	V
Thermal Regulation		$T_a=25^\circ\text{C}$, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-2.5 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, $T_j=0$ to 125°C , $C_o=10\mu\text{F}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Output Voltage	V_o	$V_{in}=4.5\text{V}$, $I_o=10\text{mA}$, $T_j=25^\circ\text{C}$	$\pm 1\%$	2.475	2.500	2.525	V
			$\pm 2\%$	2.450	2.500	2.550	V
Output Voltage	V_o	$I_o=0$ to $800/1000\text{mA}$, $V_{in}=3.9$ to 10V	$\pm 2\%$	2.450		2.550	V
			$\pm 4\%$	2.400		2.600	V
Line Regulation	ΔV_o	$V_{in}=3.9$ to 10V , $I_o=0\text{mA}$		1	6	mV	
Load Regulation	ΔV_o	$V_{in}=3.9\text{V}$, $I_o=0$ to $800/1000\text{mA}$		1	10	mV	
Temperature stability	ΔV_o			0.5		%	
Long Term Stability	ΔV_o	1000 hrs, $T_j=125^\circ\text{C}$		0.3		%	
Operating Input Voltage	V_{in}	$I_o=100\text{mA}$			15	V	
Quiescent Current	I_d	$V_{in}\leq 10\text{V}$		5	10	mA	
Output Current	I_o	$V_{in}=7.5\text{V}$, $T_j=25^\circ\text{C}$	800	950	1200	mA	

UTCLD1117/A LINEAR INTEGRATED CIRCUIT

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		μV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=5.5V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V
		Io=500mA		1.05	1.15	V
		Io=800mA		1.10	1.20	V
		Io=1000mA		1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-2.85 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=4.85V, Io=10mA, Tj=25°C	2.82	2.85	2.88	V
Output Voltage	Vo	Io=0 to 800/1000mA, Vin=4.25 to 10V	2.79		2.91	V
Line Regulation	ΔVo	Vin=4.25 to 10V, Io=0mA		1	6	mV
Load Regulation	ΔVo	Vin=4.25V, Io=0 to 800/1000mA		1	10	mV
Temperature stability	ΔVo			0.5		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin	Io=100mA			15	V
Quiescent Current	Id	Vin≤10V		5	10	mA
Output Current	Io	Vin=7.85V, Tj=25°C	800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		μV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=5.85V, Vripple=1Vpp	60	75		DB
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V
		Io=500mA		1.05	1.15	V
		Io=800mA		1.10	1.20	V
		Io=1000mA		1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-3.0 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Output Voltage	Vo	Vin=5V, Io=10mA, Tj=25°C	±1%	2.97	3.00	3.03	V
			±2%	2.94	3.00	3.06	V
Output Voltage	Vo	Io=0 to 800/1000mA, Vin=4.5 to 10V	±2%	2.94		3.06	V
			±4%	2.88		3.12	V
Line Regulation	ΔVo	Vin=4.5 to 12V, Io=0mA		1	6	mV	
Load Regulation	ΔVo	Vin=4.5V, Io=0 to 800/1000mA		1	10	mV	
Temperature stability	ΔVo			0.5		%	
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%	
Operating Input Voltage	Vin	Io=100mA			15	V	
Quiescent Current	Id	Vin≤12V		5	10	mA	
Output Current	Io	Vin=8V, Tj=25°C	800	950	1200	mA	
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		μV	
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=6V, Vripple=1Vpp	60	75		dB	

UTC LD1117/A LINEAR INTEGRATED CIRCUIT

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V
		Io=500mA		1.05	1.15	V
		Io=800mA		1.10	1.20	V
		Io=1000mA		1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-3.3 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Output Voltage	Vo	Vin=5.3V, Io=10mA, Tj=25°C	±1%	3.267	3.300	3.333	V
			±2%	3.235	3.300	3.365	V
Output Voltage	Vo	Io=0 to 800/1000mA, Vin=4.75 to 10V	±2%	3.235		3.365	V
			±4%	3.160		3.440	V
Line Regulation	ΔVo	Vin=4.75 to 15V, Io=0mA		1	6	mV	
Load Regulation	ΔVo	Vin=4.75V, Io=0 to 800/1000mA		1	10	mV	
Temperature stability	ΔVo			0.5		%	
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%	
Operating Input Voltage	Vin	Io=100mA			15	V	
Quiescent Current	Id	Vin≤15V		5	10	mA	
Output Current	Io	Vin=8.3V, Tj=25°C	800	950	1200	mA	
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		μV	
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=6.3V, Vripple=1Vpp	60	75		DB	
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V	
		Io=500mA		1.05	1.15	V	
		Io=800mA		1.10	1.20	V	
		Io=1000mA		1.15	1.25	V	
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W	

UTC LD1117/A-5.0 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Output Voltage	Vo	Vin=7V, Io=10mA, Tj=25°C	±1%	4.95	5.00	5.05	V
			±2%	4.90	5.00	5.10	V
Output Voltage	Vo	Io=0 to 800/1000mA, Vin=6.5 to 15V	±2%	4.90		5.10	V
			±4%	4.80		5.20	V
Line Regulation	ΔVo	Vin=6.5 to 15V, Io=0mA		1	10	mV	
Load Regulation	ΔVo	Vin=6.5V, Io=0 to 800/1000mA		1	15	mV	
Temperature stability	ΔVo			0.5		%	
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%	
Operating Input Voltage	Vin	Io=100mA			15	V	
Quiescent Current	Id	Vin≤15V		5	10	mA	
Output Current	Io	Vin=10V, Tj=25°C	800	950	1200	mA	
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		μV	
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=8V, Vripple=1Vpp	60	75		dB	

UTCLD1117/A LINEAR INTEGRATED CIRCUIT

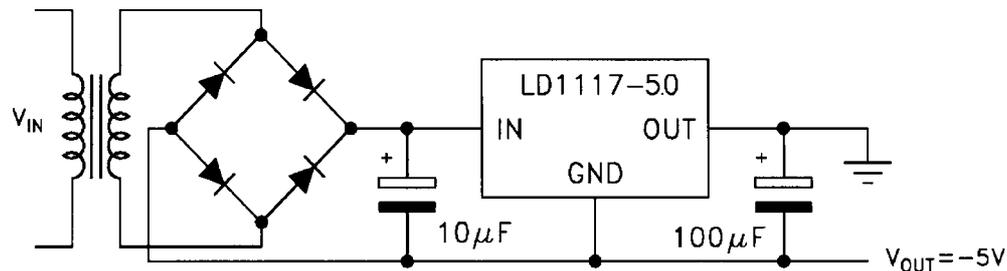
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V
		Io=500mA		1.05	1.15	V
		Io=800mA		1.10	1.20	V
		Io=1000mA		1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-ADJUSTABLE ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference Voltage	Vref	Vin-Vo=2V, Io=10mA, Tj=25°C	1.238	1.25	1.262	V
Reference Voltage	Vref	Io=10 to 800/1000mA, Vin-Vo=1.4 to 10V	1.225		1.275	V
Line Regulation	ΔVo	Vin-Vo=1.5 to 13.75V, Io=10mA		0.035	0.200	%
Load Regulation	ΔVo	Vin-Vo=3V, Io=10 to 800/1000mA		0.10	0.400	%
Temperature stability	ΔVo			0.50		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin				15	V
Adjustment Pin Current	Iadj	Vin≤15V		60	120	μA
Adjustment Pin Current Change	ΔIadj	Vin-Vo=1.4 to 10V, Io=10 to 800/1000mA		1	5	μA
Minimum Load Current	Io(min)	Vin=15V		2	5	mA
Output Current	Io	Vin-Vo=5V, Tj=25°C	800	950	1200	mA
Output Noise (%Vo)	eN	B=10Hz to 10KHz, Tj=25°C		0.003		%
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin-Vo=3V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V
		Io=500mA		1.05	1.15	V
		Io=800mA		1.10	1.20	V
		Io=1000mA		1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

TYPICAL APPLICATIONS



FLOATING INPUT

FIG.1 Negative Supply

UTCLD1117/A LINEAR INTEGRATED CIRCUIT

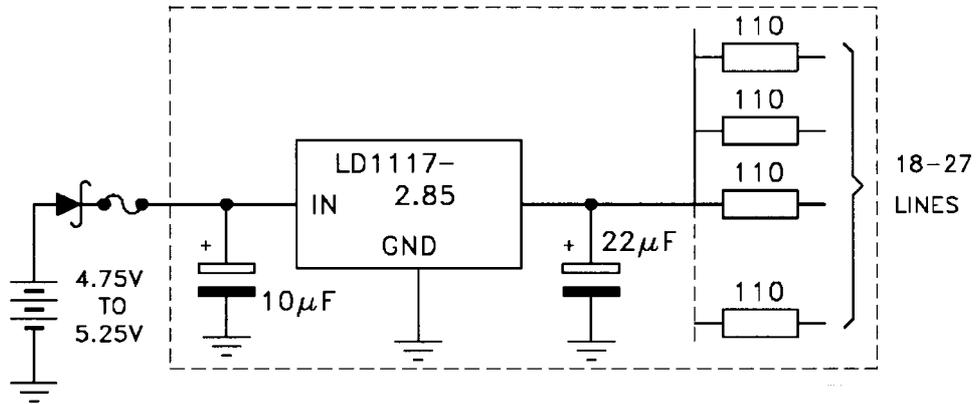


FIG.2 Active Terminator for SCSI-2 BUS

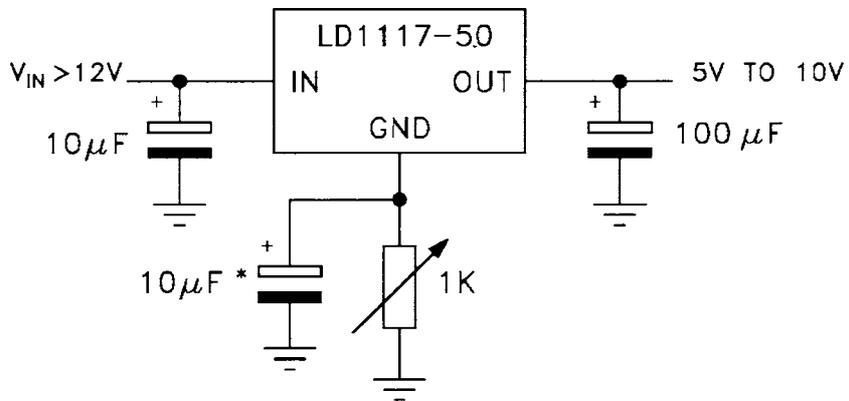


FIG.3 Circuit for Increasing Output Voltage

UTCLD1117/A LINEAR INTEGRATED CIRCUIT

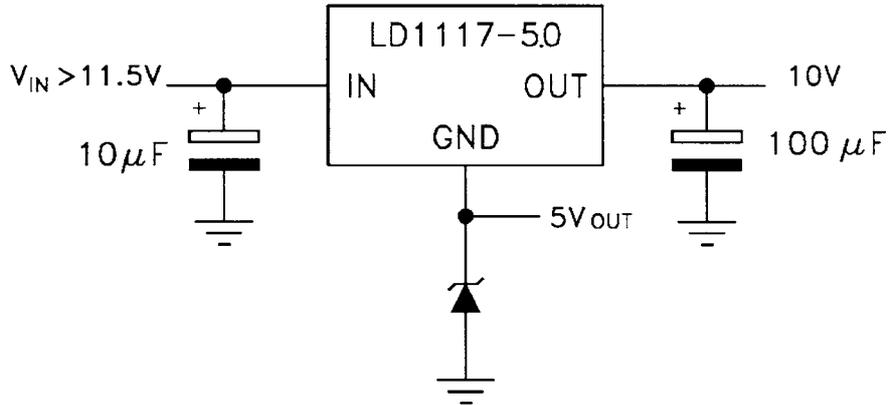


FIG.4 Voltage Regulator With Reference

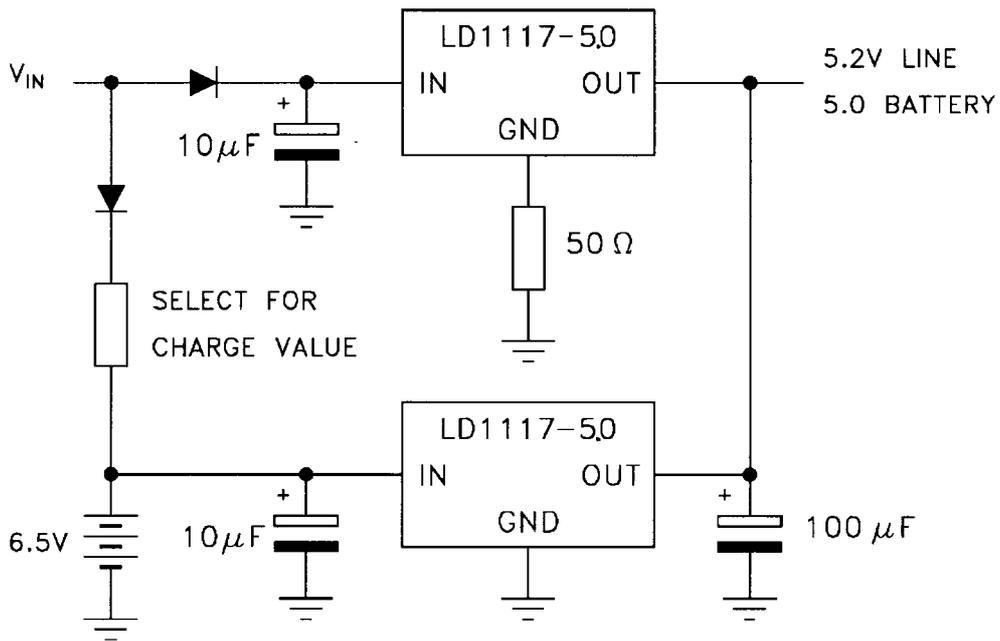


FIG.5 Battery Backed-up Regulated Supply

UTCLD1117/A LINEAR INTEGRATED CIRCUIT

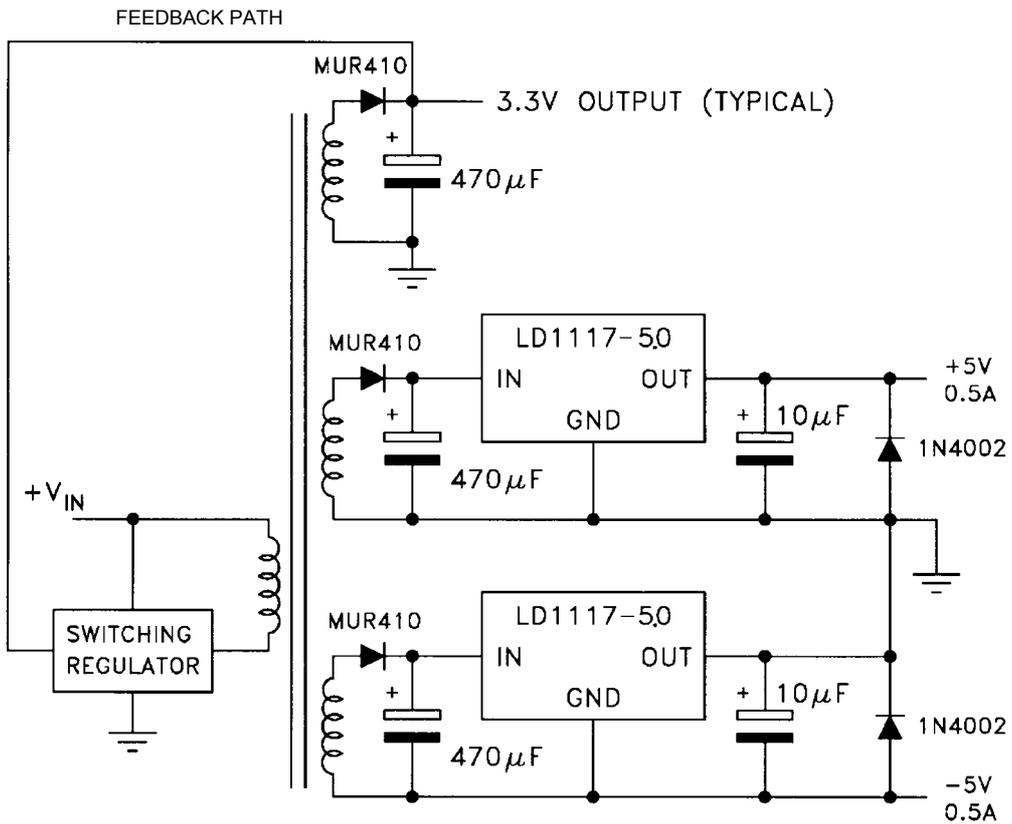


FIG.6 Post-Regulated Dual Supply

UTCLD1117/A LINEAR INTEGRATED CIRCUIT

LD1117/A ADJUSTABLE APPLICATION NOTE

The LD1117/A ADJUSTABLE has a thermal stabilized $1.25 \pm 0.012V$ reference voltage between the OUT and ADJ pins. I_{ADJ} is $60\mu A$ typ. ($120\mu A$ max.) and ΔI_{ADJ} is $1\mu A$ typ. ($5\mu A$ max.).

$R1$ is normally fixed to 120Ω . From figure 7 we obtain:

$$V_{OUT} = V_{REF} + R2(I_{ADJ} + I_{R1}) = V_{REF} + R2(I_{ADJ} + V_{REF} / R1) = V_{REF}(1 + R2/R1) + R2 \times I_{ADJ}$$

In normal application $R2$ value is in the range of few Kohm., so the $R2 \times I_{ADJ}$ product could not be considered in the V_{OUT} calculation; then the above expression becomes: $V_{OUT} = V_{REF}(1 + R2/R1)$

In order to have the better load regulation it is important to realize a good Kelvin connection of $R1$ and $R2$ resistors. In particular $R1$ connection must be realized very close to OUT and ADJ pin, while $R2$ ground connection must be placed as near as possible to the negative Load pin. Ripple rejection can be improved by introducing a $10\mu F$ electrolytic capacitor placed in parallel to the $R2$ resistor (See Fig. 8)

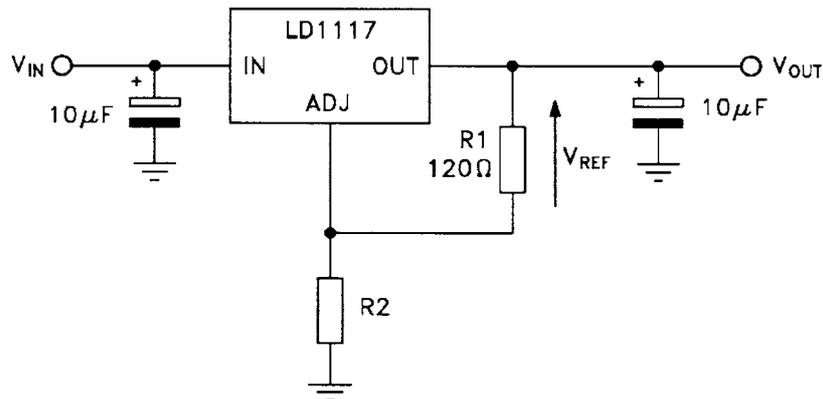


FIG.7 Adjustable Output Voltage Application Circuit

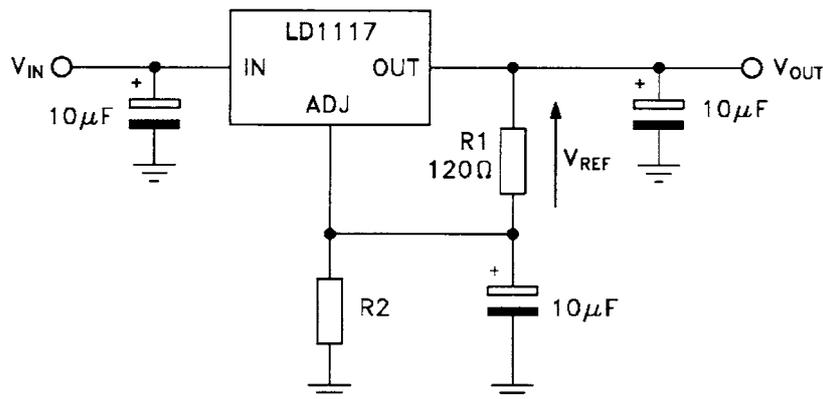


FIG.8 Adjustable Output Voltage Application with improved Ripple Rejection.

UTCLD1117/A LINEAR INTEGRATED CIRCUIT

TYPICAL CHARACTERISTICS

Fig.1 Reference Voltage vs. Temperature

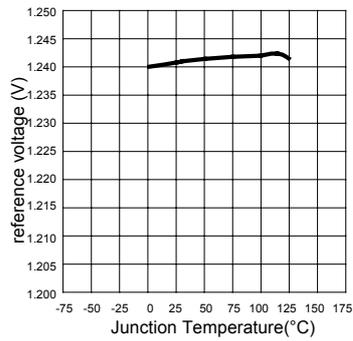


Fig.2 Output Voltage vs. Temperature

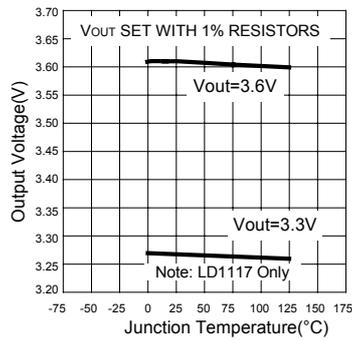


Fig.3 Maximum Power Dissipation

