FAIRCHILD SEMICONDUCTOR™

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V320
8-Bit Registered Bus Transceiver

General Description

The V320 is an 8-bit universal bus transceiver designed for high speed interfacing with the VME320 backplane. It has output characteristics optimized for driving large capacitive loads and features modified input levels (V_{IH}/V_{IL}) for increased noise immunity and reduced input skew. The V320 functionality consists of bus transceiver circuits with 3-STATE, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. $\overline{OE}$ and direction pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or in both. The select controls can multiplex stored and real time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{OE}$ is active LOW. In the isolation mode ($\overline{OE}$ HIGH) A data may be stored in the B register and/or B data may be stored in the A register.

Features

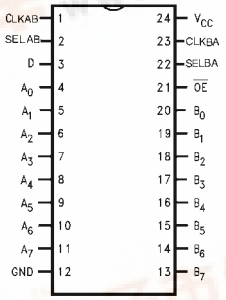
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Guaranteed output skew
- Guaranteed MOS (Multiple Output Switching) Specifications
- Output switching specified for both 50 pF and 250 pF, and 500 pF loads
- Guaranteed simultaneous switching noise level (V_{OLP}/V_{OLV}) and dynamic threshold performance (V_{IHD}/V_{ILD})
- Glitch free power up/down high impedance for live insertion
- BiCMOS technology for high drive and low power dissipation
- –40°C to 85°C commercial temperature and V_{CC} specifications
- Modified specifications across V_{CC} and temperature (V_{CC} = 5.0V ±1%, T = 25°C ± 20°C) present more realistic system conditions
- Available in TSSOP (MTC)

Ordering Code:

Order Number	Package Number	Package Description
V320MTC	MTC24	24-Lead Thin Shrink Small Outline Package, JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

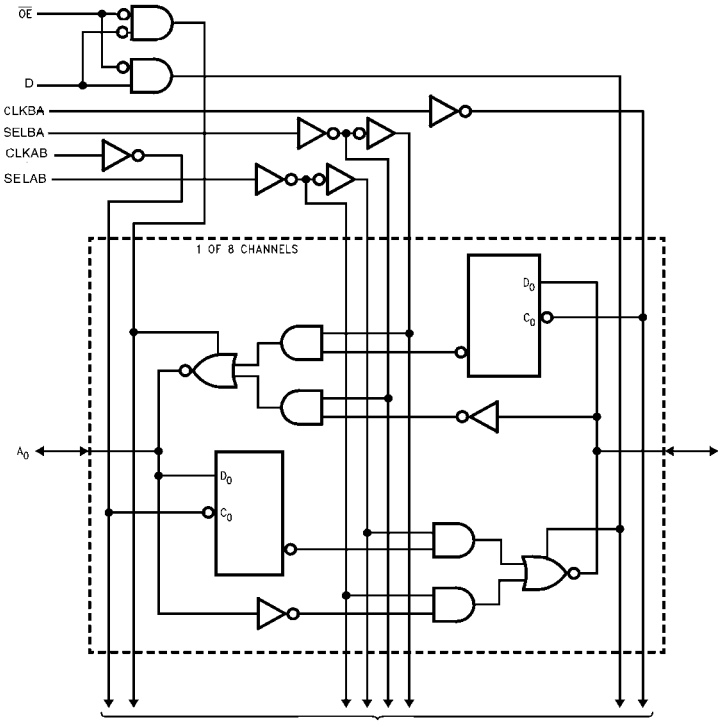
Pin Names	Description
D	Direction A-to-B (High) B-to A (Low)
$\overline{OE}$	Output Enable (Active LOW)
CLKAB/SELAB	A-to-B Clock/Select
CLKBA/SELBA	B-to-A Clock/Select
A0–7	A Inputs/Outputs (TTL)
B0–7	B Inputs/Outputs (TTL)

Functional Table

$\overline{OE}$	D	SELAB	SELBA	CLKAB	CLKBA	A_0–A_7	B_0–B_7	Function
H	X	X	X	H or L	H or L			Isolation
H	X	X	X	LH	X	Input	Input	CLK A Data into A
H	X	X	X	X	LH			CLK B Data into A Reg.
L	H	L	X	X	X			A to B – Transparent
L	H	L	X	LH	X			CLK A Data into A Reg.
L	H	H	X	H or L	X	Input	Output	A Reg. to B (Storage)
L	H	H	X	LH	X			CLK A Data into A Reg. and B output
L	L	X	L	X	X			B to A – Transparent
L	L	X	L	X	LH			CLK B Data into B Reg.
L	L	X	H	X	H or L	Output	Input	B Reg. to A (Storage)
L	L	X	H	X	LH			CLK B Data into B Reg.and A output

L = Low
H = High
LH = Low to High transition
X = Don't Care

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

DC Input Voltage (V_I)	−0.5V to +7.0V
DC Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +7.0V
Outputs Active (Note 2)	−0.5V to V_{CC} +0.5V
DC Output Sink Current into A-port/B-port I_{OL}	64 mA
DC Output Source Current from A-port/B-port I_{OH}	−32 mA
DC Input Diode Current (I_{IK})	
$V_I < 0_V$	−30 mA to +5.0 mA
ESD Rating typical	> 2000V
Storage temperature (T_{STG})	−65° C to +15°C
Max I_{OL} (Current Applied to a LOW Output)	2 X I_{OL} Spec.

Recommended Operating Conditions

Supply Voltage V_{CC}	
Operating V_{CC}	4.5V to 5.5V
Minimum Input Edge Rate	
Data Input	50 mV/ns
Enable	20 mV/ns
Clock	100 mV/ns
Operating Temperature (T_A)	−40°C to +85°C

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics ($4.5V < V_{CC} \leq 5.5V$)

Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Symbol		Parameter	V_{CC} (V)	Min	Typ	Max	Units	Conditions
V_{IH}	B-Port/A-Port	HIGH Level Input Voltage	4.5–5.5	2.0			V	Recognized HIGH Signal
			4.95–5.05	1.8 (Note 3)				
V_{IL}	B-Port/A-Port	LOW Level Input Voltage	4.5–5.5			0.8	V	Recognized LOW Signal
			4.95–5.05			1.2 (Note 3)		
V_{OH}	B-Port/A-Port	HIGH Level Output Voltage	4.5	2.5			V	−3 mA
			4.5	2.0				−32 mA
I_{OH}	B-Port/A-Port	High Level Output Current Drive	4.5	−32			mA	V_{OH} = 2.0V
V_{OL}	B-Port/A-Port	LOW Level Output Voltage	4.5	0.55			V	64 mA
I_{OL}	B-Port/A-Port	Low Level Output Current Drive (Sink)	4.5	64			mA	V_{OL} = 0.55V
I_{OS}	B-Port/A-Port	Short Circuit Current	5.5	−100		−275	mA	V_{OUT} = 0.0V
I_{OFF}	A-Port and Control Pins	Power-OFF Leakage Current	0.0			100uA	uA	V_{OUT} = 5.5V, All Others GND
I_{CCH}	B-Port/A-Port	Quiescent Power Supply Current	5.5			250	uA	All Outputs HIGH
I_{CCI}	B-Port/A-Port	B-Port/A-Port	5.5			30	mA	All Outputs LOW
I_{CCZ}	B-Port/A-Port	3-STATE Power Supply Current	5.5			50	uA	All Outputs 3-STATE

Note 3: Extended Characteristics ($4.95 > V_{CC} > 5.05$, T = 25°C ± 20°C)

Capacitance and Dynamic Switching Characteristics

Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ $T_A = 25°C$	Max	Units	Conditions
C_{IN}	Input Capacitance (Control Pin)		5		pF	$V_{CC} = 5.0V$ $V_I = V_{CC}$ or 0
$C_{I/O}$	Output Capacitance (A and B ports)		11		pF	$V_{CC} = 5.0V$ $V_I = V_{CC}$ or 0
Output Switching Noise (Ground Bounce)						
V_{OLP}	Quiet Output Dynamic Peak V_{OL}			0.8	V	$V_{CC} = 5.0V$, T= 25°C
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	−1.2			V	$C_L = 50$ pF
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	2.5			V	
Input Noise Immunity (Dynamic Threshold)						
V_{IHD}	High Level Threshold Movement	2.2			V	$V_{CC} = 5.0V$, T= 25°C
V_{ILD}	Low Level Threshold Movement			0.5	V	$C_L = 50$ pF

AC Operating Requirements

Over recommended ranges of supply voltage and operating free-air temperature

Symbol			Min	Typ	Max	Units
f_{CLOCK}	Max Clock Frequency		200 (Note 4)			MHz
t_{WIDTH}	Pulse Duration	HIGH or LOW	3.0			ns
t_{SU}	Setup Time	Bus to CLKAB/CLKBA	1.5			ns
t_{HOLD}	Hold Time	Bus to CLKAB/CLKBA	1.0			ns

Note 4: $C_L = 50$ pF

AC Electrical Characteristics
(–40°C to 85°C, V_{CC} = 4.5V to 5.5V) 1 Output Switching

Symbol	From (Input)	Mode	To (Output)	Min	Typ	Max	Units
Output Load: C_L = 50 pF, R_L= 500Ω, 1 Output Switching							
t_{PLH}, t_{PHL}	CLKAB/CLKBA	Register	Bus A or B	1.7		5.6	ns
t_{PLH}, t_{PHL}	Bus A or B	Transparent	Bus A or B	1.5		4.8	ns
t_{PLH}, t_{PHL}	SELAB/SELBA	Select Bus	Bus A or B	1.5		5.9	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	1.5		6.0	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	1.5		6.3	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	1.5		6.0	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	1.5		6.3	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			0.3		1.2	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			0.3		1.4	ns
Output Load: C_L = 250 pF, R_L = 500Ω, 1 Output Switching							
t_{PLH}, t_{PHL}	CLKAB/CLKBA	Register	Bus A or B	2.0		7.5	ns
t_{PLH}, t_{PHL}	Bus A or B	Transparent	Bus A or B	2.0		7.0	ns
t_{PLH}, t_{PHL}	SELAB/SELBA	Select Bus	Bus A or B	2.0		7.5	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	(Note 5)		(Note 5)	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	2.0		8.0	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	(Note 5)		(Note 5)	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	2.0		8.3	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			1.7		3.9	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			0.8		3.1	ns
Output Load: C_L = 500 pF, R_L = 500Ω, Output Switching							
$t_{PLH}t_{PHL}$	CLKAB/CLKBA	Register	Bus A or B	3.0		12.2	ns
$t_{PLH}t_{PHL}$	Bus A or B	Transparent	Bus A or B	3.0		11.6	ns
$t_{PLH}t_{PHL}$	SELAB/SELBA	Select Bus	Bus A or B	3.0		12.4	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	(Note 5)		(Note 5)	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	3.0		12.6	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	(Note 5)		(Note 5)	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	6.3		13.2	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			3.5		7.2	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			1.4		5.1	ns

Note 5: 3-STATE delays are dominated by the RC Network (500 Ω/ 250 pF, or 500 Ω/ 500 pF) on the output and thus have been excluded from this datasheet.

AC Electrical Characteristics
(–40°C to 85°C, V_{CC} = 4.5V to 5.5V) 8 Output Switching

Symbol	From (Input)	Mode	To (Output)	Min	Typ	Max	Units
Output Load: C_L = 50 pF, R_L = 500Ω, 8 Outputs Switching							
t_{PLH}, t_{PHL}	CLKAB/CLKBA	Register	Bus A or B	1.5		6.6	ns
t_{PLH}, t_{PHL}	Bus A or B	Transparent	Bus A or B	1.5		6.3	ns
t_{PLH}, t_{PHL}	SELAB/SELBA	Select Bus	Bus A or B	1.5		6.6	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	1.5		6.6	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	1.5		6.6	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	1.5		6.6	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	1.5		7.6	ns
t_{OSHL}	Output to Output Skew (Note 6)					1.3	ns
t_{OSHL}	Output to Output Skew (Note 6)					1.1	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			0.5		1.5	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			0.4		1.9	ns
Output Load: C_L = 250 pF, R_L = 500Ω, 8 Outputs Switching							
t_{PLH}, t_{PHL}	CLKAB/CLKBA	Register	Bus A or B	2.5		11.2	ns
t_{PLH}, t_{PHL}	Bus A or B	Transparent	Bus A or B	2.5		9.5	ns
t_{PLH}, t_{PHL}	SELAB/SELBA	Select Bus	Bus A or B	2.5		11.2	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	(Note 8)		(Note 8)	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	2.5		11.5	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	(Note 8)		(Note 8)	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	2.5		13.5	ns
t_{OSHL}	Output to Output Skew (Note 8)					2.5	ns
t_{OSLH}	Output to Output Skew (Note 8)					2.0	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			2.0		5.5	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			1.4		4.4	ns
Output Load: C_L = 500 pF, R_L = 500Ω, 8 Outputs Switching							
t_{PLH}, t_{PHL}	CLKAB/CLKBA	Register	Bus A or B	3.5		17.0	ns
t_{PLH}, t_{PHL}	Bus A or B	Transparent	Bus A or B	3.5		15.9	ns
t_{PLH}, t_{PHL}	SELAB/SELBA	Select Bus	Bus A or B	3.5		17.0	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	(Note 8)		(Note 8)	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	3.5		18.5	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	(Note 8)		(Note 8)	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	3.5		22.3	ns
t_{OSHL}	Output to Output Skew (Note 6)					3.9	ns
t_{OSLH}	Output to Output Skew (Note 6)					3.1	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			4.4		7.8	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			2.5		6.6	ns

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to outputs switching in the same direction also.

Note 7: Device to Device Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs from any two devices.

Note 8: 3-STATE delays are dominated by the RC Network (500 Ω/ 250 pF, or 500 Ω/ 500 pF) on the output and thus have been excluded from this datasheet.

Extended AC Electrical Characteristics
(5°C to 45°C, V_{CC} = 4.95V to 5.05V), 1 Output Switching

Symbol	From (Input)	Mode	To (Output)	Min	Typ	Max	Units
Output Load: C_L = 50 pF, R_L = 500Ω, 1 Output Switching							
t_{PLH}, t_{PHL}	CLKAB/CLKBA	Register	Bus A or B	1.5		5.2	ns
t_{PLH}, t_{PHL}	Bus A or B	Transparent	Bus A or B	1.5		4.3	ns
t_{PLH}, t_{PHL}	SELAB/SELBA	Select Bus	Bus A or B	2.0		4.8	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	1.5		6.0	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	2.2		5.0	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	1.5		6.0	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	2.2		5.2	ns
t_{PV}	Device to Device Skew (Note 10)					2.0	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			3.0		1.2	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			0.4		1.2	ns
Output Load: C_L = 250 pF, R_L = 500Ω, 1 Output Switching							
t_{PLH}, t_{PHL}	CLKAB/CLKBA	Register	Bus A or B	2.5		7.4	ns
t_{PLH}, t_{PHL}	Bus A or B	Transparent	Bus A or B	2.5		6.7	ns
t_{PLH}, t_{PHL}	SELAB/SELBA	Select Bus	Bus A or B	3.0		7.2	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	(Note 9)		(Note 9)	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	3.2		7.2	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	(Note 9)		(Note 9)	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	3.2		8.1	ns
t_{PV}	Device to Device Skew (Note 10)					2.5	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			2.1		3.5	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			1.0		2.5	ns
Output Load: C_L = 500 pF, R_L = 500Ω, 1 Output Switching							
t_{PLH}, t_{PHL}	CLKAB/CLKBA	Register	Bus A or B	3.5		10.6	ns
t_{PLH}, t_{PHL}	Bus A or B	Transparent	Bus A or B	3.5		10.0	ns
t_{PLH}, t_{PHL}	SELAB/SELBA	Select Bus	Bus A or B	4.0		10.6	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	(Note 9)		(Note 9)	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	4.2		10.5	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	(Note 9)		(Note 9)	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	4.2		11.3	ns
t_{PV}	Device to Device Skew					5.0	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			3.8		6.4	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			1.7		3.8	ns

Note 9: 3-STATE delays are dominated by the RC Network (500 Ω/ 250 pF, or 500 Ω/ 500 pF) on the output and thus have been excluded from this datasheet.

Note 10: Device to Device Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs from any two devices.

Extended AC Electrical Characteristics
(5°C to 45°C, V_{CC} = 4.95V to 5.05V), 8 Outputs Switching

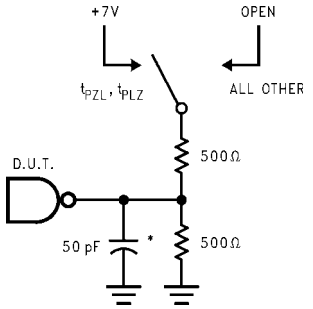
Symbol	From (Input)	Mode	To (Output)	Min	Typ	Max	Units
Output Load: C_L = 50 pF, R_L = 500Ω, 8 Outputs Switching							
t_{PLH}, t_{PHL}	CLKAB/CLKBA	Register	Bus A or B	2.5		6.2	ns
t_{PLH}, t_{PHL}	Bus A or B	Transparent	Bus A or B	2.5		5.4	ns
t_{PLH}, t_{PHL}	SELAB/SELBA	Select Bus	Bus A or B	2.5		5.7	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	1.5		6.0	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	2.5		5.7	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	1.5		6.0	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	2.5		7.2	ns
t_{OSHL}	Output to Output Skew (Note 12)					1.1	ns
t_{OSLH}	Output to Output Skew (Note 12)					0.9	ns
t_{PV}	Device to Device Skew (Note 13)					2.5	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			0.5		1.3	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			0.6		1.4	ns
Output Load: C_L = 250 pF, R_L = 500Ω, 8 Outputs Switching							
t_{PLH}, t_{PHL}	CLKAB/CLKBA	Register	Bus A or B	3.5		10.5	ns
t_{PLH}, t_{PHL}	Bus A or B	Transparent	Bus A or B	3.5		10.5	ns
t_{PLH}, t_{PHL}	SELAB/SELBA	Select Bus	Bus A or B	3.5		10.5	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	(Note 11)		(Note 11)	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	3.5		10.5	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	(Note 11)		(Note 11)	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	3.5		14.8	ns
t_{OSHL}	Output to Output Skew (Note 12)					2.3	ns
t_{OSLH}	Output to Output Skew (Note 12)					1.9	ns
t_{PV}	Device to Device Skew(Note 13)					4.0	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			2.7		4.7	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			1.8		3.7	ns
Output Load: C_L = 500 pF, R_L = 500Ω, 8 Outputs Switching							
t_{PLH}, t_{PHL}	CLKAB/CLKBA	Register	Bus A or B	5.0		15.3	ns
t_{PLH}, t_{PHL}	Bus A or B	Transparent	Bus A or B	5.0		13.6	ns
t_{PLH}, t_{PHL}	SELAB/SELBA	Select Bus	Bus A or B	5.0		15.3	ns
t_{PLZ}, t_{PHZ}	$\overline{OE}$	Output Disable	Bus A or B	(Note 11)		(Note 11)	ns
t_{PZH}, t_{PZL}	$\overline{OE}$	Output Enable	Bus A or B	5.0		15.1	ns
t_{PLZ}, t_{PHZ}	Direction (D)	Dir. Disable	Bus A or B	(Note 11)		(Note 11)	ns
t_{PZH}, t_{PZL}	Direction (D)	Dir. Enable	Bus A or B	5.0		19.4	ns
t_{OSHL}	Output to Output Skew (Note 12)					3.5	ns
t_{OSLH}	Output to Output Skew (Note 12)					2.9	ns
t_{PV}	Device to Device Skew					5.0	ns
t_{RISE}	Transition Time, Outputs (1V to 2V)			4.6		7.0	ns
t_{FALL}	Transition Time, Outputs (1V to 2V)			2.9		4.9	ns

Note 11: 3-STATE delays are dominated by the RC Network (500 Ω/ 250 pF, or 500 Ω/ 500 pF) on the output and thus have been excluded from this datasheet.

Note 12: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to outputs switching in the same direction also.

Note 13: Device to Device Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs from any two devices.

AC Loading and Waveforms



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

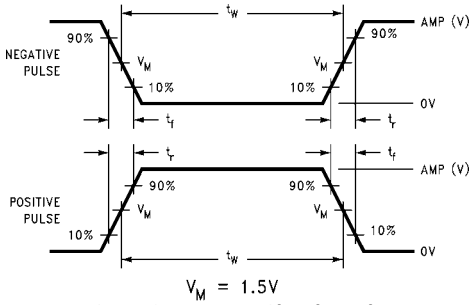


FIGURE 2. Test Input Signal Levels Input Pulse Requirements

Test Input Signal Requirements

Amplitude	Rep. Rate	t_W	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

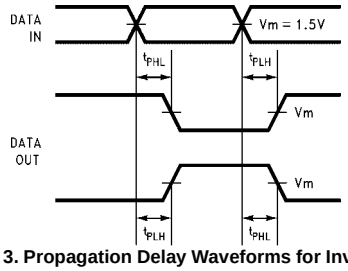


FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

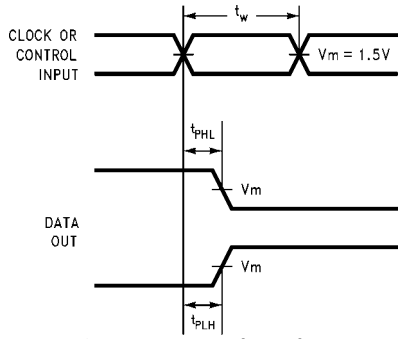


FIGURE 4. Propagation Delay, Pulse Width Waveforms

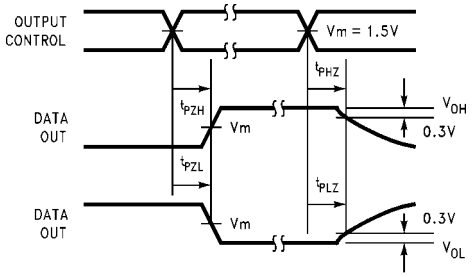


FIGURE 5. 3-STATE Output HIGH and LOW Enable and Disable Times

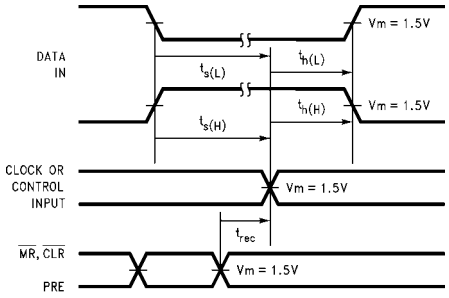
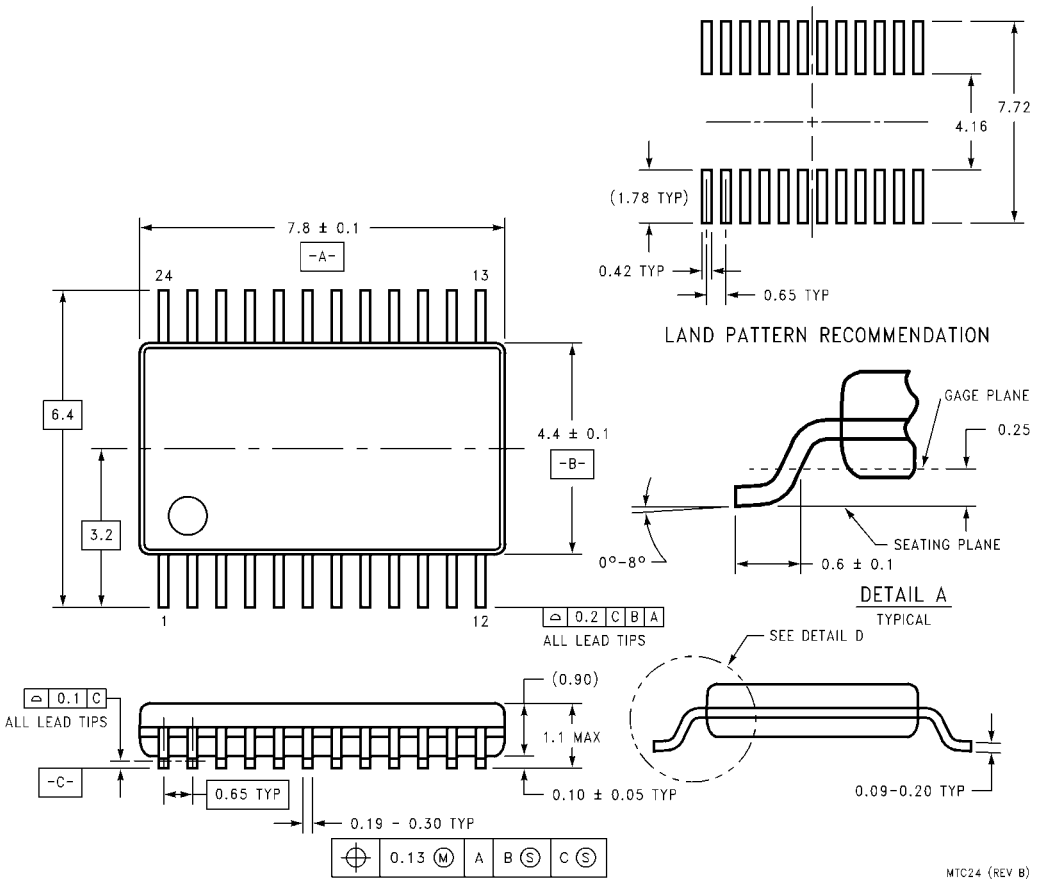


FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Thin Shrink Small Outline Package, JEDEC MO-153, 4.4mm Wide
Package Number MTC24

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