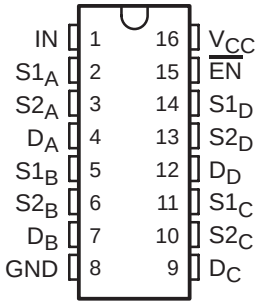
查询TS3V340供应商

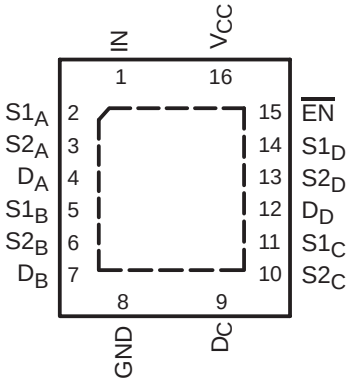


- **Low Differential Gain and Phase ($D_G$ = 0.2%, $D_P$ = 0.1° Typ)**
- **Wide Bandwidth ($B_W$ = 500 MHz Typ)**
- **Low Crosstalk ($X_{TALK}$ = −80 dB Typ)**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low and Flat ON-State Resistance ($r_{on}$ = 3 Ω Typ, $r_{on(flat)}$ = 1 Ω Typ)**
- **$V_{CC}$ Operating Range From 3 V to 3.6 V**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Data and Control Inputs Provide Undershoot Clamp Diode**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Suitable for Both RGB and Composite Video Switching**

**D, DBQ, DGV, OR PW PACKAGE**
**(TOP VIEW)**




**RGY PACKAGE**
**(TOP VIEW)**




## description/ordering information

The TI video switch TS3V340 is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable ($\overline{EN}$) input. When $\overline{EN}$ is low, the switch is enabled, and the D port is connected to the S port. When $\overline{EN}$ is high, the switch is disabled, and the high-impedance state exists between the D and S ports. The select (IN) input controls the data path of the multiplexer/demultiplexer.

Low differential gain and phase makes this switch ideal for composite and RGB video applications. The device has a wide bandwidth and low crosstalk, making it suitable for high-frequency applications as well.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | QFN − RGY | Tape and reel | TS3V340RGYR | TF340 |
| | SOIC − D | Tube | TS3V340D | TS3V340 |
| | | Tape and reel | TS3V340DR | |
| | SSOP (QSOP) − DBQ | Tape and reel | TS3V340DBQR | TF340 |
| | TSSOP − PW | Tube | TS3V340PW | TF340 |
| | | Tape and reel | TS3V340PWR | |
| | TVSOP − DGV | Tape and reel | TS3V340DGVR | TF340 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## description/ordering information (continued)

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ feature ensures that damaging current will not backflow through the device when it is powered down. This switch maintains isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{EN}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**FUNCTION TABLE**

| INPUTS | | INPUT/OUTPUT D | FUNCTION |
|---|---|---|---|
| $\overline{EN}$ | IN | | |
| L | L | S1 | D port = S1 port |
| L | H | S2 | D port = S2 port |
| H | X | Z | Disconnect |

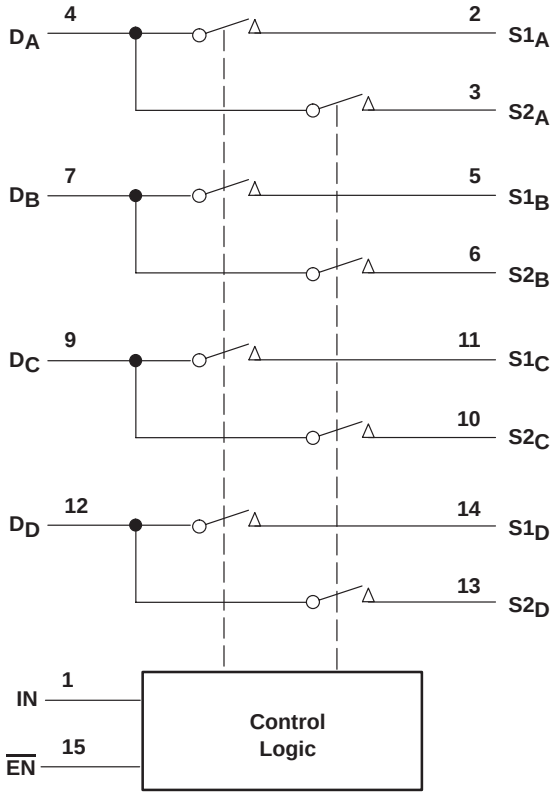
**PIN DESCRIPTION**

| PIN NAME | DESCRIPTION |
|---|---|
| S1, S2 | Analog video I/Os |
| D | Analog video I/Os |
| IN | Select input |
| $\overline{EN}$ | Switch-enable input |

**PARAMETER DEFINITIONS**

| PARAMETER | DESCRIPTION |
|---|---|
| $R_{ON}$ | Resistance between the D and S ports, with the switch in the ON state |
| $I_{OZ}$ | Output leakage current measured at the D and S ports, with the switch in the OFF state |
| $I_{OS}$ | Short-circuit current measured at the I/O pins |
| $V_{IN}$ | Voltage at IN |
| $V_{EN}$ | Voltage at $\overline{EN}$ |
| $C_{IN}$ | Capacitance at the control ($\overline{EN}$, IN) inputs |
| $C_{OFF}$ | Capacitance at the analog I/O port when the switch is OFF |
| $C_{ON}$ | Capacitance at the analog I/O port when the switch is ON |
| $V_{IH}$ | Minimum input voltage for logic high for the control ($\overline{EN}$, IN) inputs |
| $V_{IL}$ | Maximum input voltage for logic low for the control ($\overline{EN}$, IN) inputs |
| $V_{IK}$ | I/O and control ($\overline{EN}$, IN) inputs diode clamp voltage |
| $V_I$ | Voltage applied to the D or S pins when D or S is the switch input |
| $V_O$ | Voltage applied to the D or S pins when D or S is the switch output |
| $I_{IH}$ | Input high leakage current of the control ($\overline{EN}$, IN) inputs |
| $I_{IL}$ | Input low leakage current of the control ($\overline{EN}$, IN) inputs |
| $I_I$ | Current into the D or S pins when D or S is the switch input |
| $I_O$ | Current into the D or S pins when D or S is the switch output |
| $I_{off}$ | Output leakage current measured at the D or S ports, with $V_{CC}$ = 0 |
| $t_{pds}$ | Propagation delay measured between $S1_X$ and $S2_X$ under the specified conditions, measured from 50% of the digital input to 90% of the analog output |
| $B_W$ | Frequency response of the switch in the ON state, measured at −3 dB |
| $X_{TALK}$ | Unwanted signal coupled from channel to channel. Measured in −dB. $X_{TALK}$ = 20 log $V_O/V_I$. This is a nonadjacent crosstalk. |
| $O_{IRR}$ | OFF isolation is the resistance (measured in −dB) between the input and output with the switch OFF. |
| $D_G$ | Magnitude variation between analog input and output pins when the switch is ON and the DC offset of composite video signal varies at the analog input pin. In NTSC standard, the frequency of the video signal is 3.58 MHz, and DC offset is from 0 to 0.714 V. |
| $D_P$ | Phase variation between analog input and output pins when the switch is ON and the DC offset of composite video signal varies at the analog input pin. In NTSC standard, the frequency of the video signal is 3.58 MHz, and DC offset is from 0 to 0.714 V. |
| $I_{CC}$ | Static power-supply current |
| $I_{CCD}$ | Variation of $I_{CC}$ for a change in frequency in the control ($\overline{EN}$, IN) inputs |
| $\Delta I_{CC}$ | Increase in supply current for each control input that is at the specified voltage level, rather than $V_{CC}$ or GND |

## functional diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 4.6 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2) . . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . . −0.5 V to 7 V
Control input clamp current, $I_{IK}$ ($V_{IN}$ < 0) . . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0) . . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . . ±128 mA
Continuous current through $V_{CC}$ or GND terminals . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): D package . . . . . 73°C/W
(see Note 5): DBQ package . . . . . 90°C/W
(see Note 5): DGV package . . . . . 120°C/W
(see Note 5): PW package . . . . . 108°C/W
(see Note 6): RGY package . . . . . 39°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground, unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. $V_I$ and $V_O$ are used to denote specific conditions for $V_{I/O}$.
4. $I_I$ and $I_O$ are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

### recommended operating conditions (see Note 7)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 3 | 3.6 | V |
| $V_{IH}$ | High-level control input voltage ($\overline{EN}$, IN) | 2 | 5.5 | V |
| $V_{IL}$ | Low-level control input voltage ($\overline{EN}$, IN) | 0 | 0.8 | V |
| $V_O$ | Analog I/O voltage | 0 | 5.5 | V |
| $T_A$ | Operating free-air temperature | −40 | 85 | °C |

NOTE 7: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted)†

| PARAMETER | | TEST CONDITIONS | | | | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $\overline{EN}$, IN | $V_{CC}$ = 3 V, | $I_{IN}$ = −18 mA | | | | | −1.8 | V |
| $I_{IH}$ | $\overline{EN}$, IN | $V_{CC}$ = 3.6 V, | $V_{IN}$ and $V_{EN}$ = 5.5 V | | | | | ±1 | µA |
| $I_{IL}$ | $\overline{EN}$, IN | $V_{CC}$ = 3.6 V, | $V_{IN}$ and $V_{EN}$ = GND | | | | | ±1 | µA |
| $I_{OZ}$§ | | $V_{CC}$ = 3.6 V, | $V_O$ = 0 to 5.5 V, | $V_I$ = 0, | Switch OFF | | | ±1 | µA |
| $I_{OS}$¶ | | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 $V_{CC}$, | $V_I$ = 0, | Switch ON | 50 | | | mA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_O$ = 0 to 5.5 V, | $V_I$ = 0 | | | | 1 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, | $I_{I/O}$ = 0, | Switch ON or OFF | | | 0.7 | 1.5 | mA |
| $\Delta I_{CC}$ | $\overline{EN}$, IN | $V_{CC}$ = 3.6 V, | One input at 3 V, | Other inputs at $V_{CC}$ or GND | | | | 30 | µA |
| $I_{CCD}$ | | $V_{CC}$ = 3.6 V, D and S ports open, | $V_{EN}$ = GND, $V_{IN}$ input switching 50% duty cycle | | | | | 0.35 | mA/ MHz |
| $C_{IN}$ | $\overline{EN}$, IN | $V_{IN}$ or $V_{EN}$ = 5.5 V, | 3.3 V or 0, | f = 1 MHz | | | 2.5 | 3.5 | pF |
| $C_{OFF}$ | D port | $V_I$ = 5.5 V, 3.3 V, or 0, | f = 1 MHz, | Outputs open, | Switch OFF | | 5.5 | 7 | pF |
| | S port | | | | | | 3.5 | 5 | |
| $C_{ON}$ | | $V_I$ = 5.5 V, 3.3 V, or 0, | f = 1 MHz, | Outputs open, | Switch ON | | 10.5 | 14 | pF |
| $r_{on}$# | | $V_{CC}$ = 3 V | $V_I$ = 1 V, | $I_O$ = 13 mA | | | 3 | 6 | Ω |
| | | | $V_I$ = 2 V, | $I_O$ = 26 mA | | | 3 | 6 | |
| $r_{on(flat)}$‖ | | $V_{CC}$ = 3.3 V, | $V_I$ = 0 to $V_{CC}$, | $I_O$ = 26 mA | | | 1 | | Ω |

† $V_I$, $V_O$, $I_I$, and $I_O$ refer to I/O pins.
‡ All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
§ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
¶ The $I_{OS}$ test is applicable to only one ON channel at a time. The duration of this test is less than 1 s.
# Measured by the voltage drop between the D and S terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (D or S) terminals.
‖ $r_{on(flat)}$ is the difference of $r_{on}$ in a given channel at specified voltages.

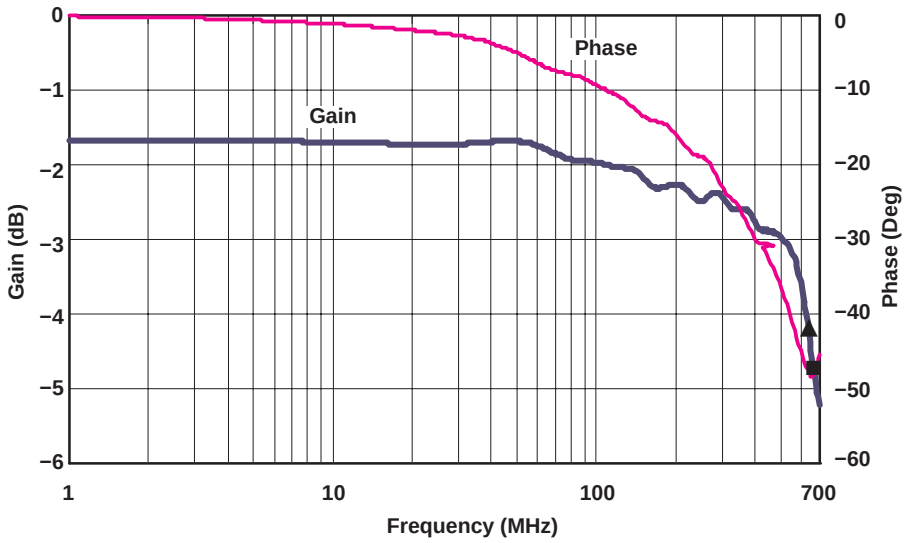
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V, $R_L$ = 75 Ω, $C_L$ = 20 pF (unless otherwise noted) (see Figures 6 and 7)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd(s)}$ | IN | D | | 2 | 5 | ns |
| $t_{ON}$ | IN or $\overline{EN}$ | S | | 4 | 7 | ns |
| $t_{OFF}$ | IN or $\overline{EN}$ | S | | 2 | 7 | ns |

## dynamic characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted)

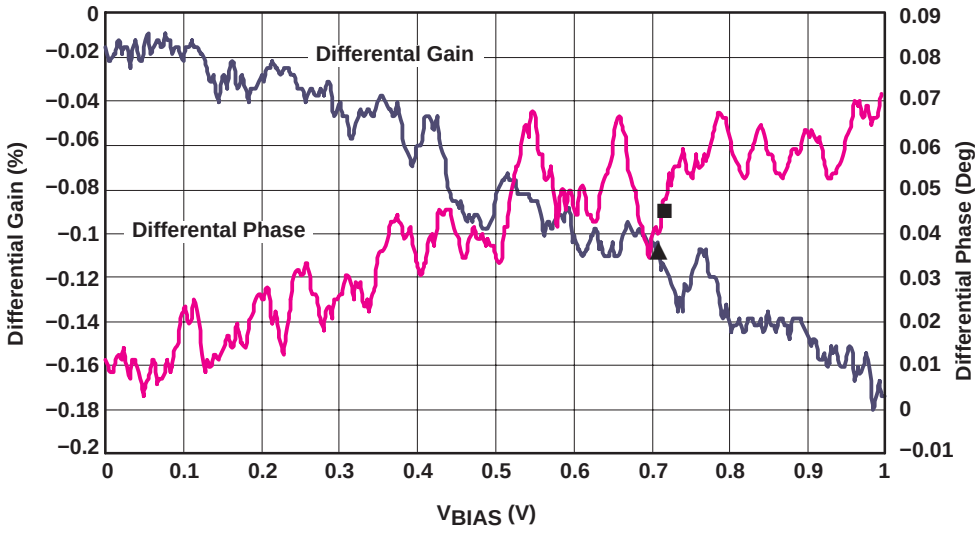
| PARAMETER | TEST CONDITIONS | | | | TYP‡ | UNIT |
|---|---|---|---|---|---|---|
| $D_G$☆ | $R_L$ = 150 Ω, | f = 3.58 MHz, | See Figure 7 | | 0.2 | % |
| $D_P$☆ | $R_L$ = 150 Ω, | f = 3.58 MHz, | See Figure 7 | | 0.1 | ° |
| $B_W$ | $R_L$ = 150 Ω, | See Figure 8 | | | 500 | MHz |
| $X_{TALK}$ | $R_L$ = 150 Ω, | f = 10 MHz, | $R_{IN}$ = 10 Ω, | See Figure 9 | −80 | dB |
| $O_{IRR}$ | $R_L$ = 150 Ω, | f = 10 MHz, | See Figure 10 | | −60 | dB |

‡ All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
☆ $D_G$ and $D_P$ are expressed in absolute magnitude.



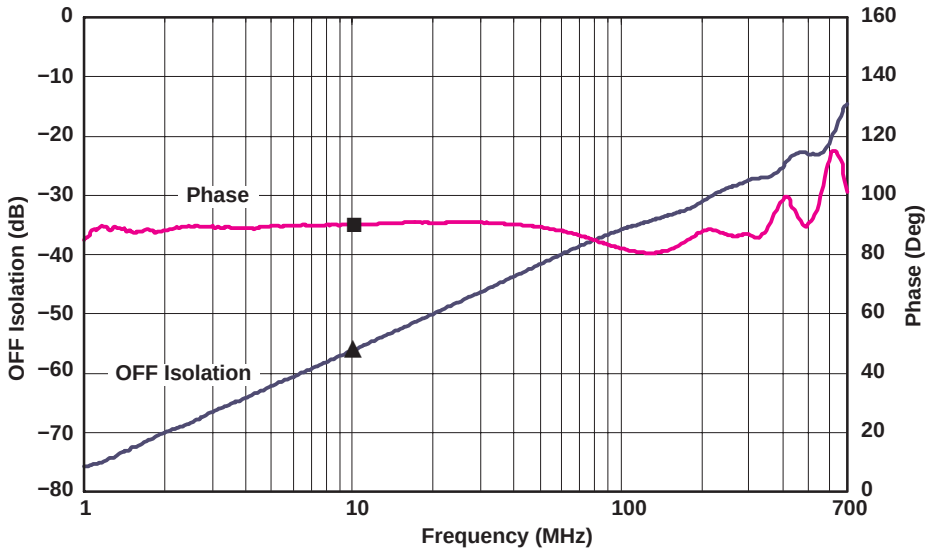

▲ Gain −3 dB at 627 MHz
■ Phase at −3-dB Frequency, −47 Deg

**Figure 1. Gain/Phase vs Frequency**



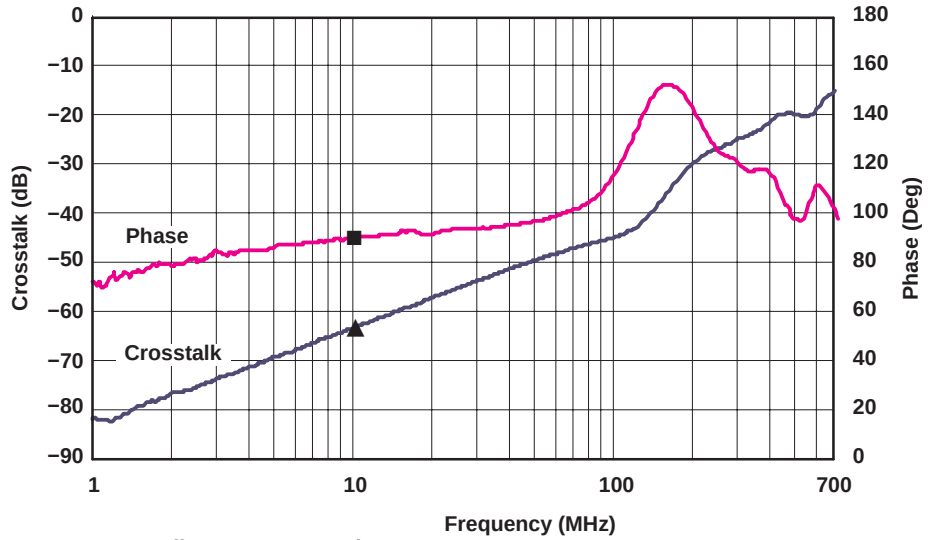

▲ Differential Gain at 0.714 V, −0.11%
■ Differential Phase at 0.714 V, 0.0466 Deg

**Figure 2. Differential Gain/Phase vs $V_{BIAS}$**




▲ OFF Isolation at 10 MHz, −56 dB
■ Phase at 10 MHz, 90 Deg

**Figure 3. OFF Isolation vs Frequency**




▲ Crosstalk at 10 MHz, −63 dB
■ Phase at 10 MHz, 90 Deg

**Figure 4. Crosstalk vs Frequency**

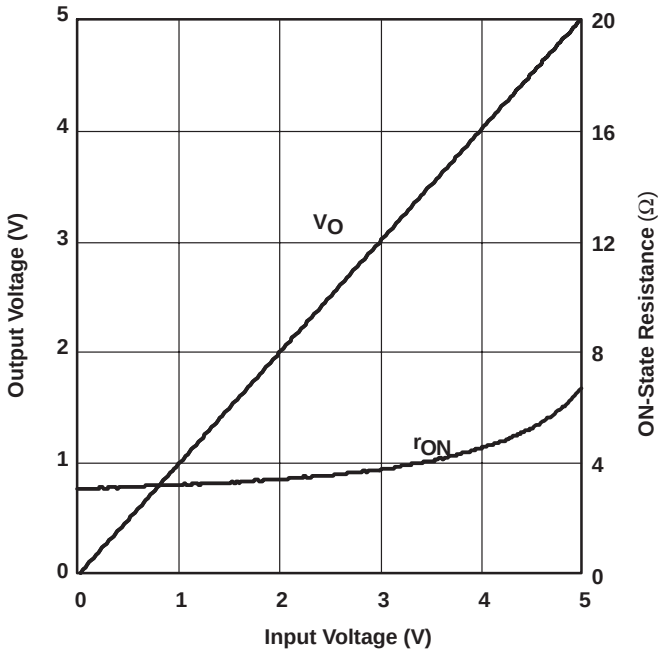
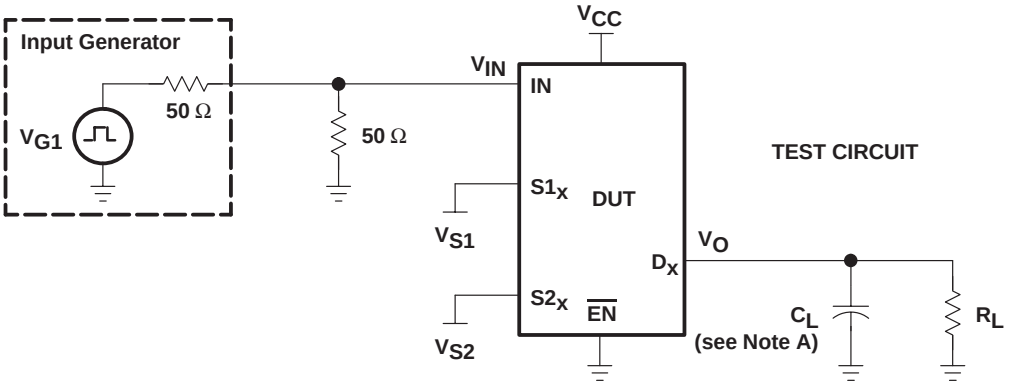
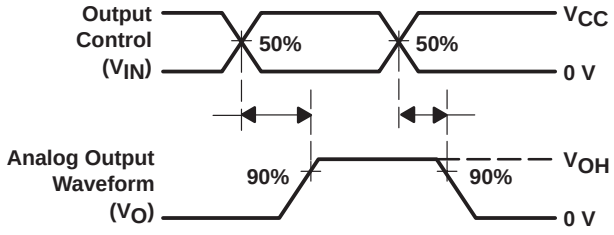



**Figure 5. Output Voltage/ON-State Resistance vs Input Voltage**

## PARAMETER MEASUREMENT INFORMATION




| TEST | $V_{CC}$ | $R_L$ | $C_L$ | $V_{S1}$ | $V_{S2}$ |
|---|---|---|---|---|---|
| $t_{pds}$ | 3.3 V ± 0.3 V | 75 | 20 pF | GND | $V_{CC}$ |
| | 3.3 V ± 0.3 V | 75 | 20 pF | $V_{CC}$ | GND |

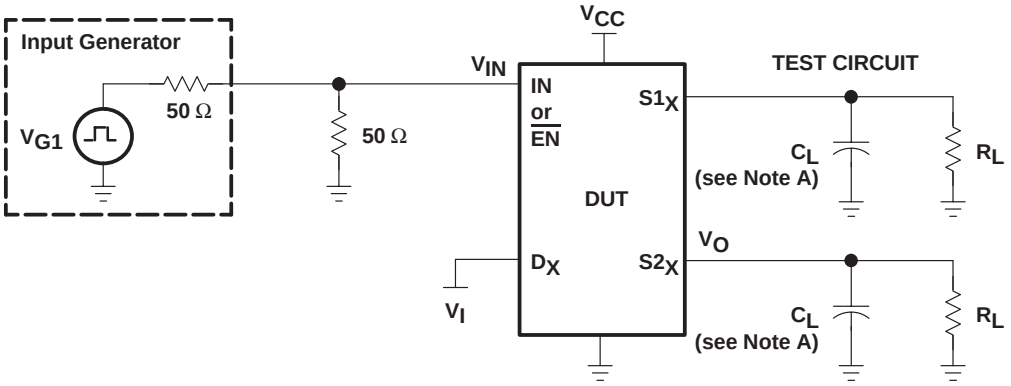



**VOLTAGE WAVEFORMS**
**$t_{pd(s)}$ TIMES**

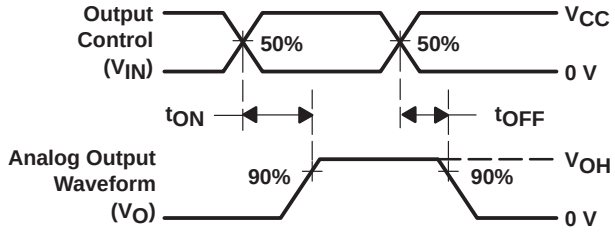
NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
C. The outputs are measured one at a time, with one transition per measurement.

**Figure 6. Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION




| TEST | $V_{CC}$ | $R_L$ | $C_L$ | $V_I$ |
|---|---|---|---|---|
| $t_{ON}/t_{OFF}$ | 3.3 V ± 0.3 V | 75 Ω | 20 pF | $V_{CC}$ |

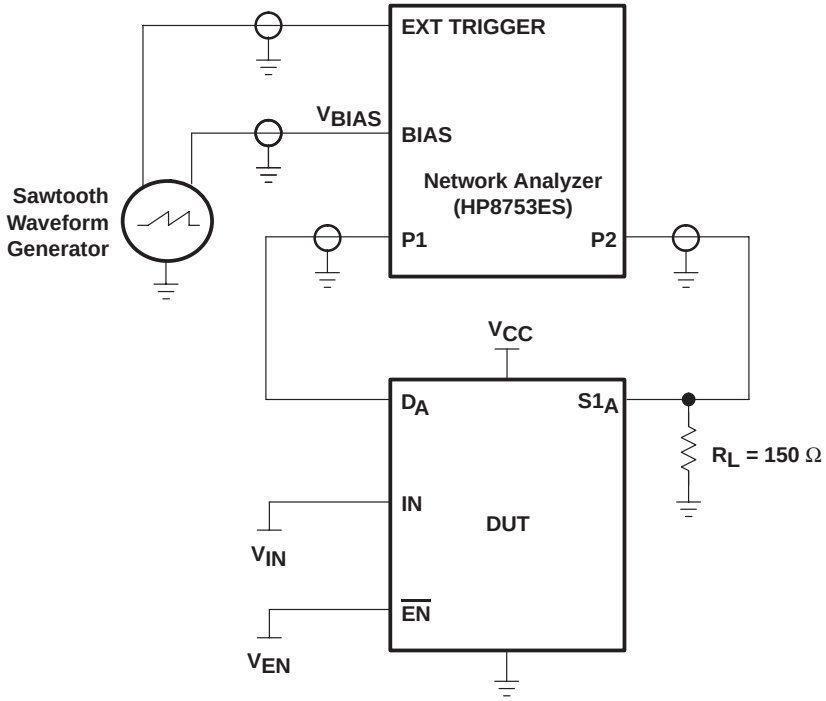



VOLTAGE WAVEFORMS
$t_{ON}$ AND $t_{OFF}$ TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
C. The outputs are measured one at a time, with one transition per measurement.

**Figure 7. Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION




NOTE: For additional information on measurement method, refer to the TI application report, *Measuring Differential Gain and Phase*, literature number SLOA040.

**Figure 8. Test Circuit for Differential Gain/Phase Measurement**

Differential gain and phase is measured at the output of the ON channel. For example, when $V_{IN}$ = 0, $V_{EN}$ = 0, and $D_A$ is the input, the output is measured at $S1_A$.

### HP8753ES setup

Average = 20
RBW = 300 Hz
ST = 1.381 s
P1 = −7 dBM
CW frequency = 3.58 MHz

### sawtooth waveform generator setup

$V_{BIAS}$ = 0 to 1 V
Frequency = 0.905 Hz

## PARAMETER MEASUREMENT INFORMATION

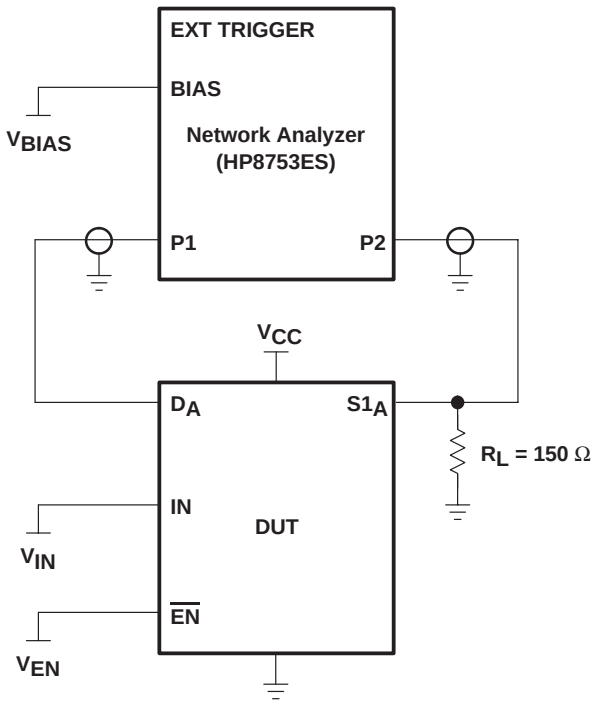


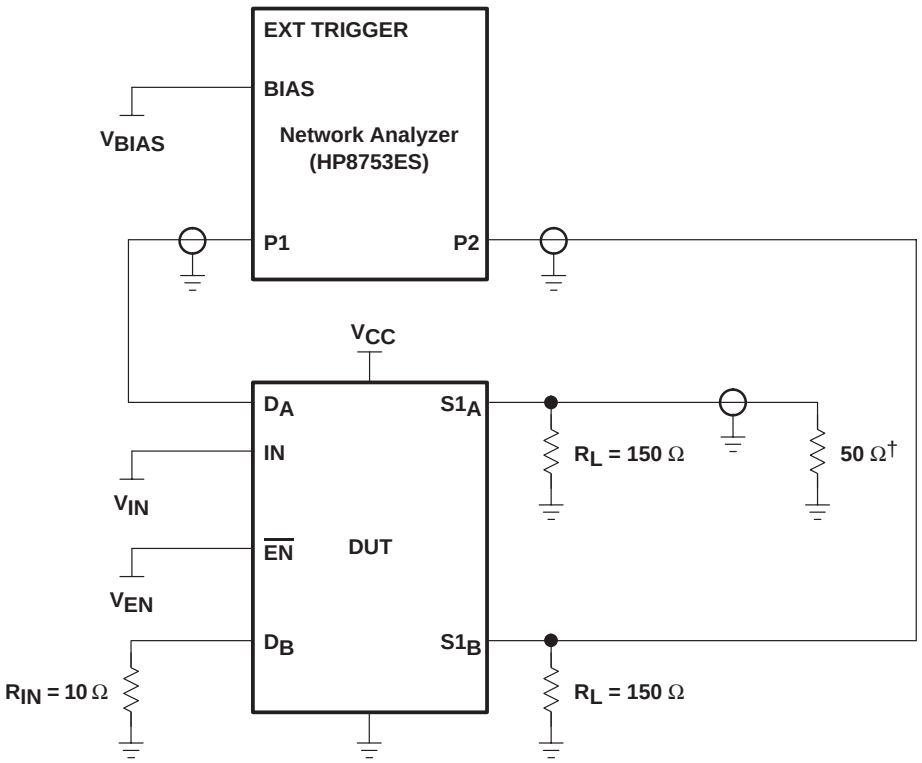

**Figure 9. Test Circuit for Frequency Response ($B_W$)**

The frequency response is measured at the output of the ON channel. For example, when $V_{IN}$ = 0, $V_{EN}$ = 0, and $D_A$ is the input, the output is measured at $S1_A$. All unused analog I/O ports are left open.

### HP8753ES setup

Average = 4
RBW = 3 kHz
$V_{BIAS}$ = 0.35 V
ST = 2 s
P1 = 0 dBM

## PARAMETER MEASUREMENT INFORMATION




† A 50-Ω termination resistor is needed for the network analyzer.

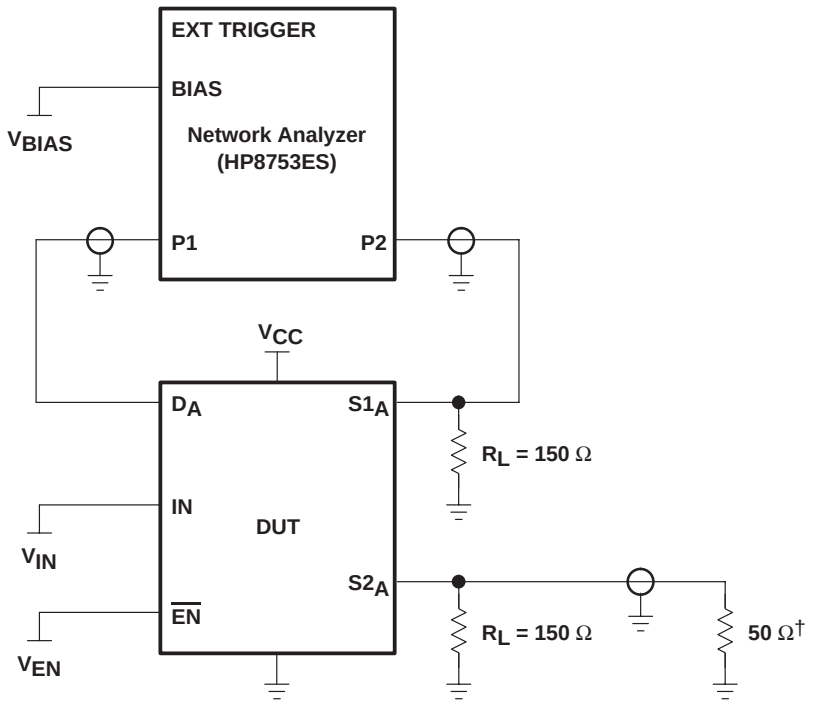
**Figure 10. Test Circuit for Crosstalk ($X_{TALK}$)**

The crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_{IN}$ = 0, $V_{EN}$ = 0, and $D_A$ is the input, the output is measured at $S1_B$. All unused analog input (D) ports and output (S) ports are connected to GND through 10-Ω and 50-Ω pulldown resistors, respectively.

### HP8753ES setup

Average = 4
RBW = 3 kHz
$V_{BIAS}$ = 0.35 V
ST = 2 s
P1 = 0 dBM

## PARAMETER MEASUREMENT INFORMATION




† A 50-Ω termination resistor is needed for the network analyzer.

**Figure 11. Test Circuit for OFF Isolation ($O_{IRR}$)**

The OFF isolation is measured at the output of the OFF channel. For example, when $V_{IN} = V_{CC}$, $V_{EN} = 0$, and $D_A$ is the input, the output is measured at $S1_A$. All unused analog input (D) ports are left open, and output (S) ports are connected to GND through 50-Ω pulldown resistors.

### HP8753ES setup

Average = 4
RBW = 3 kHz
$V_{BIAS}$ = 0.35 V
ST = 2 s
P1 = 0 dBM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TS3V340D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS3V340DBQR | ACTIVE | SSOP/ QSOP | DBQ | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| TS3V340DBQRE4 | ACTIVE | SSOP/ QSOP | DBQ | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| TS3V340DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS3V340DGVR | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS3V340DGVRE4 | ACTIVE | TVSOP | DGV | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS3V340DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS3V340DRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS3V340PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS3V340PWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS3V340PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS3V340PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TS3V340RGYR | ACTIVE | QFN | RGY | 16 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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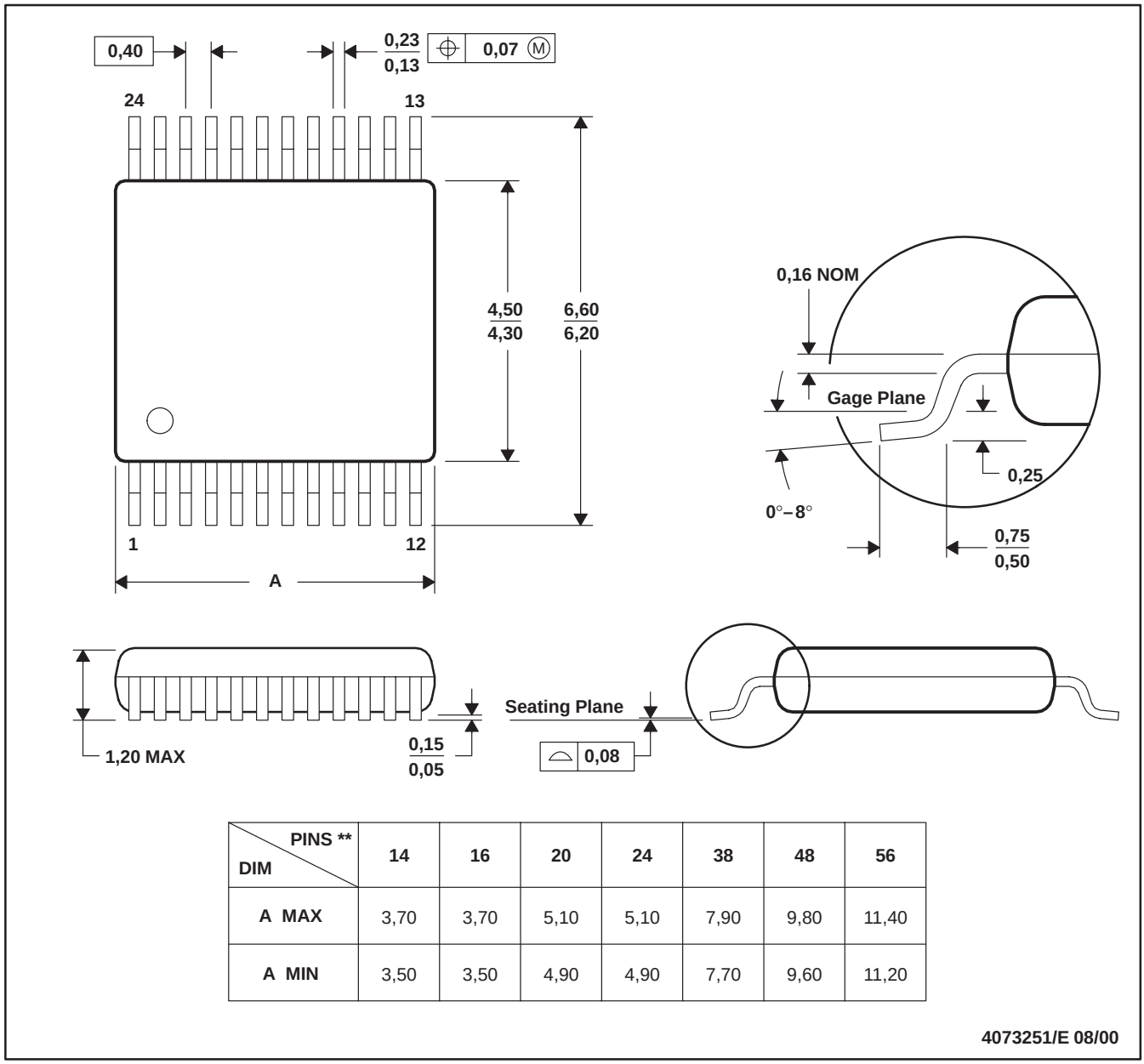
**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

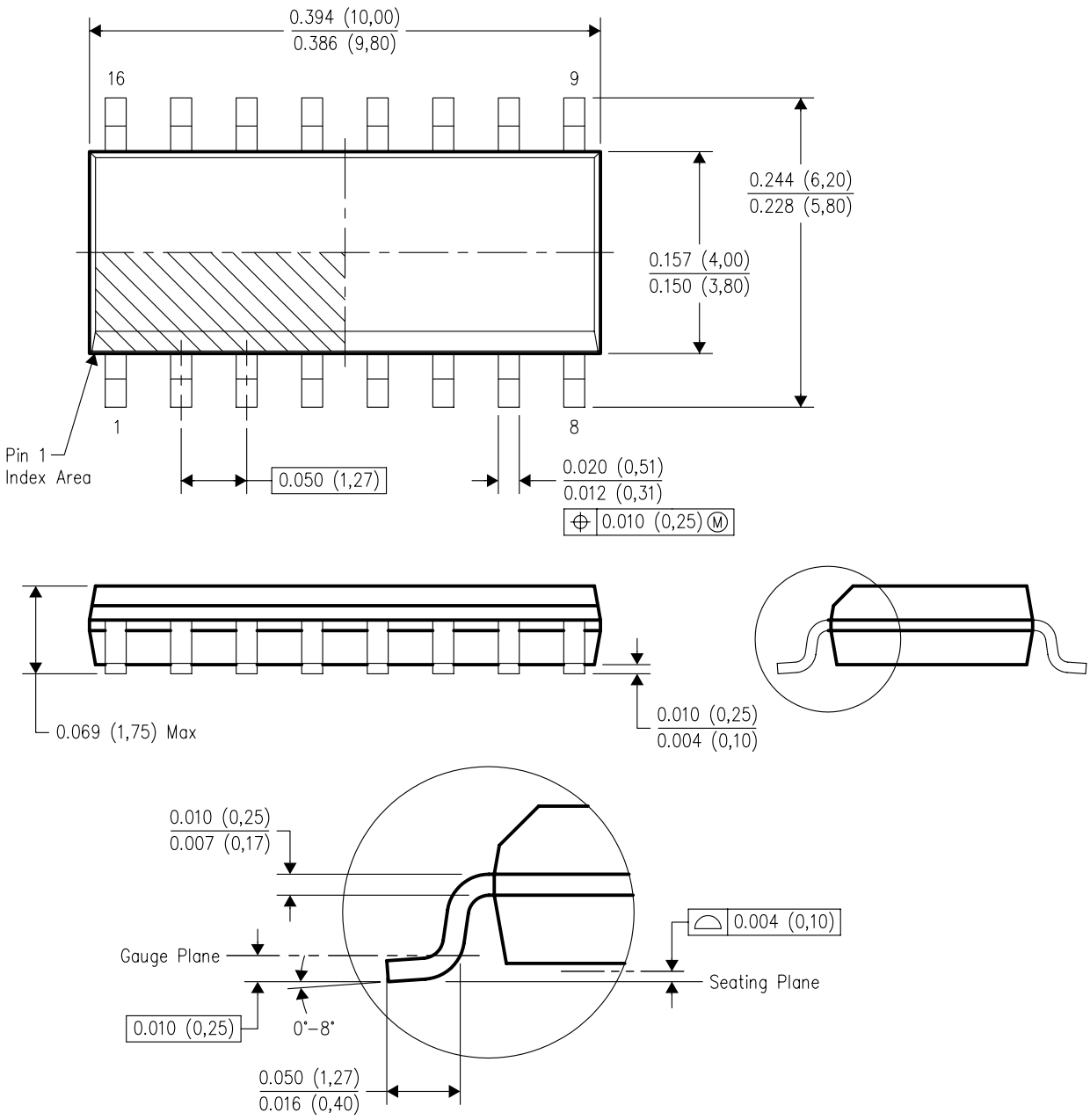



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

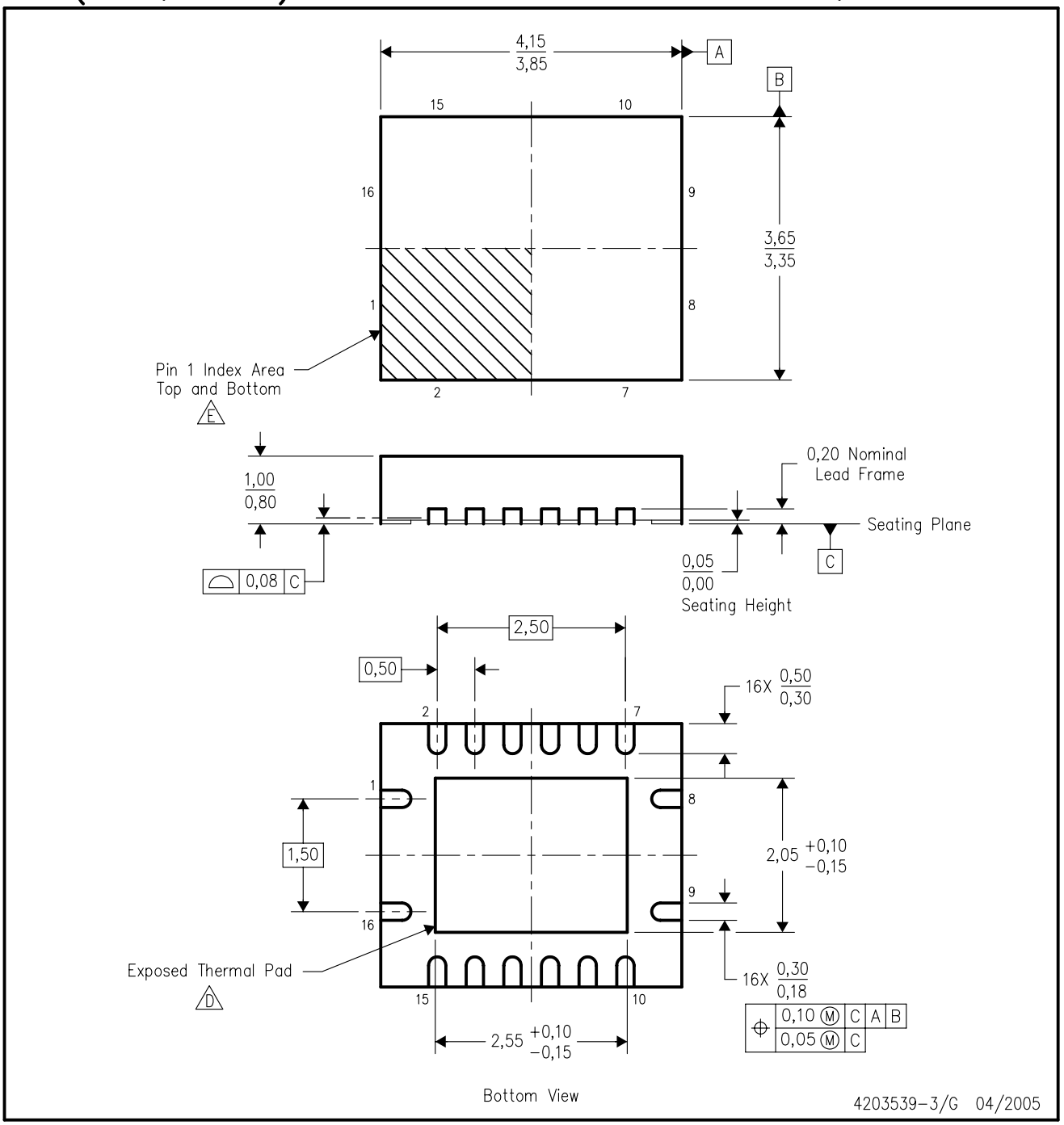
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

## D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



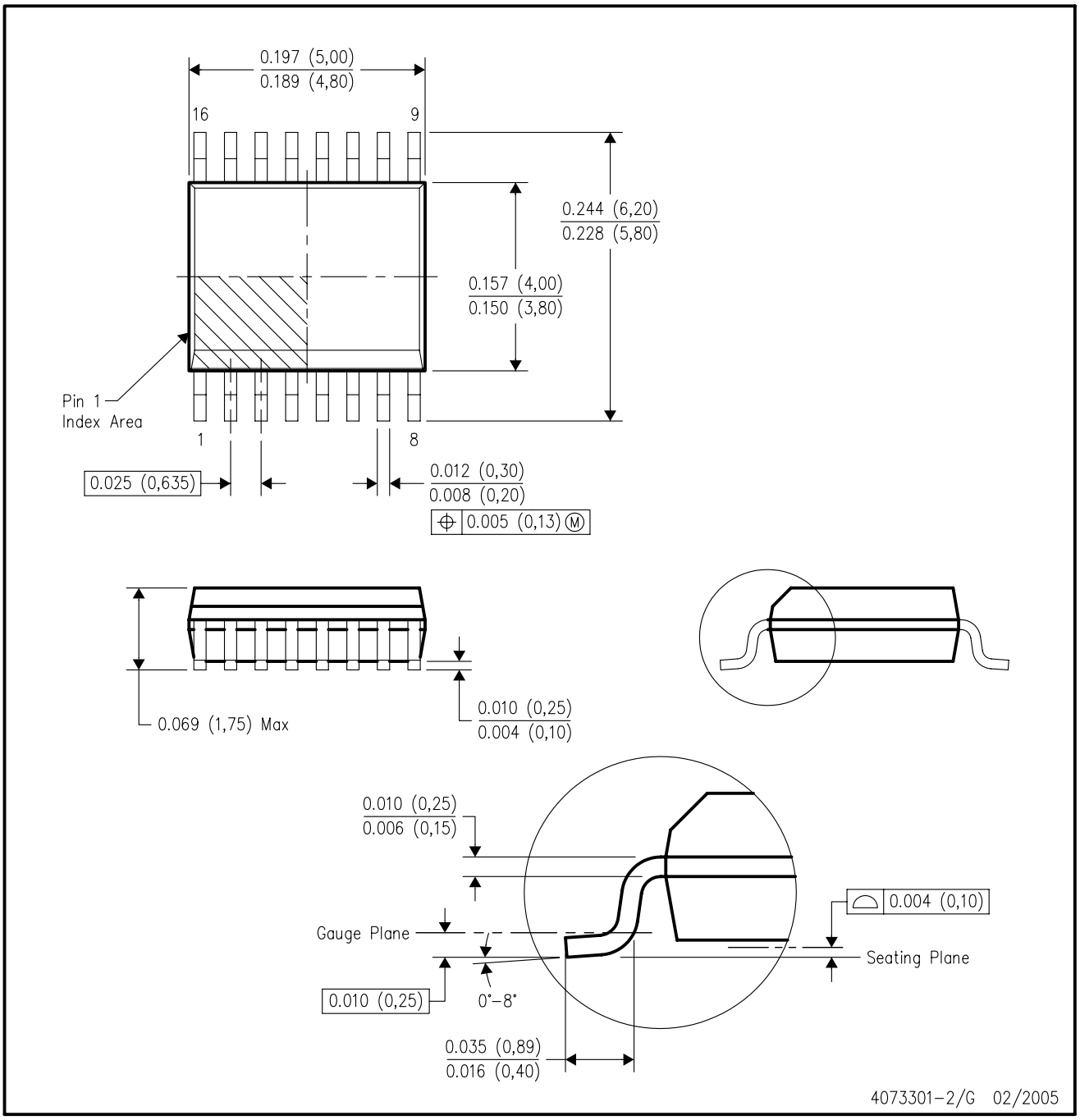

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

RGY (R–PQFP–N16) PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BB.

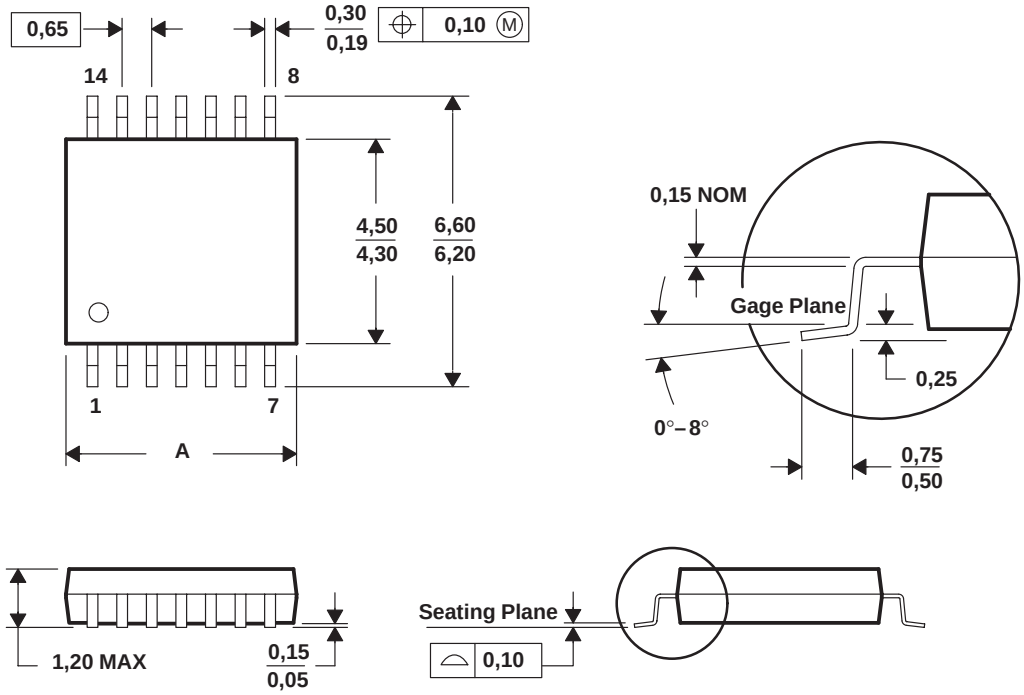
## DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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