VITELIC

V53C104 FAMILY
HIGH PERFORMANCE, LOW POWER
256K X 4 BIT FAST PAGE MODE
CMOS DYNAMIC RAM

PRELIMINARY

HIGH PERFORMANCE V53C104	85/85L	10/10L	12/12L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	85 ns	100 ns	120 ns
Max. Column Address Access Time, (t_{CAA})	40 ns	45 ns	55 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	55 ns	65 ns	75 ns
Min. Read/Write Cycle Time, (t_{RC})	160 ns	190 ns	220 ns

LOW POWER V53C104L	85L	10L	12L
Max. CMOS Standby Current, (I_{DD6})	1.5 mA	1.5 mA	1.5 mA

Features

- Low power dissipation for V53C104-12
  - Operating Current—70 mA max.
  - TTL Standby Current—3.5 mA max.
- Low CMOS Standby Current
  - V53C104—3 mA max.
  - V53C104L—1.5 mA max.
- Read-Modify-Write, $\overline{RAS}$-only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Fast Page Mode operation for a sustained data rate greater than 18 MHz
- 512 Refresh cycles/8 ms
- Standard package is 20 pin Plastic DIP. Consult factory on SOJ and ZIP packages.
- Industrial temperature range (I), –40 to +85°C, consult factory

Description

The Vitelic V53C104 is a high speed 262144 x 4 bit CMOS dynamic random access memory. Fabricated with Vitelic's VICMOS technology, the V53C104 offers a combination of size and features unattainable with NMOS technology: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request extended refresh for very low data retention power (V53C104L).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 512 (x4) bits within a row with cycle times as short as 55 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C104 ideally suited for graphics, digital signal processing and high performance computing systems.

The V53C104L (-12) offers a maximum data retention power of 10 mW when operating in CMOS standby mode and performing $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. For Selected V53C104L devices with Refresh Interval longer than 8 ms, consult factory.

Device Usage Chart

Operating Temperature Range	Package Outline			Access Time (ns)			Power		Temperature Mark
	P	K	Z	85	100	120	Low	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	•	Blank

VITELIC

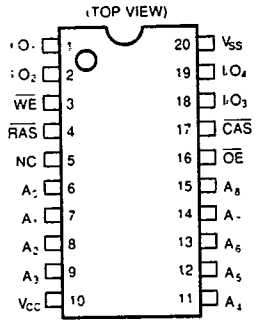
V53C104

Description	Pkg.	Pin Count
Plastic DIP	P	20
SOJ	K	26
Plastic ZIP	Z	20

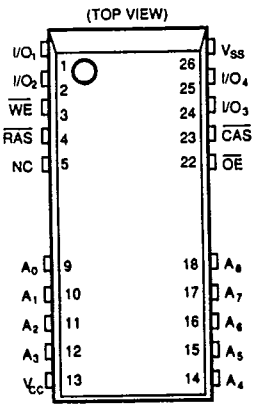
V 5 3 C 1 0 4 _ _ _ _ _

- FAMILY: 53
- DEVICE: C104
- PKG.: P (PLASTIC DIP), K (SOJ), Z (PLASTIC ZIP)
- SPEED (t_{RAC}): -85 (85 ns), -10 (100 ns), -12 (120 ns)
- PWR.: BLANK (NORMAL), L (LOW POWER)
- TEMP.: BLANK (0°C to 70°C)

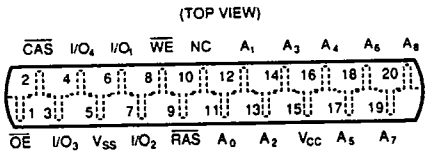
20 Lead Plastic DIP PIN CONFIGURATION Top View



26 Lead SOJ Package PIN CONFIGURATION Top View



20 Lead Plastic ZIP PIN CONFIGURATION Top View



PIN NAMES

A_0 ~ A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1 ~ I/O_4	Data Input, Output
V_{CC}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Ambient Temperature
Under Bias .....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} .....–1.0 V to +7.0 V
Voltage on V_{DD} relative to V_{SS}.....–1.0 V to +7.0 V
Data Output Current .....50 mA
Power Dissipation .....1.0 W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

T_A = 25°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, D_{IN}	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	4	5	pF
C_{OUT}	Output	4	6	pF

* Note: Capacitance is sampled and not 100% tested

DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C104			V53C104L			Unit	Test Conditions	Notes
			Min.	Typ.	Max.	Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10		10	−10		10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10		10	−10		10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	−85			95			95	V	$t_{RC} = t_{RC}$ (min.)	1, 2
		−10			80			80			
		−12			70			70			
I_{DD2}	V_{DD} Supply Current, TTL Standby				3.5			2.0	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	−85			95			95	mA	$t_{RC} = t_{RC}$ (min.)	2
		−10			80			80			
		−12			70			70			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	−85			50			50	mA	Minimum Cycle	1, 2
		−10			40			40			
		−12			35			35			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled				4			2.5	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby				3			1.5	mA	$\overline{RAS} \ge V_{DD}$ −0.2 V, CAS at V_{IH} all other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage		−1		0.8	−1		0.8	V		3
V_{IH}	Input High Voltage		2.4		V_{DD}+1	2.4		V_{DD}+1	V		3
V_{OL}	Output Low Voltage				0.4			0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4			2.4			V	I_{OH} = −5 mA	

VITELIC V53C104

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	85/L		10/L		12/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	85	85K	100	85K	120	85K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	160		190		220		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	65		80		90		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	85		100		120		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	30		35		40		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	55	25	65	30	80	ns	
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	4
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		20		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		20		25		ns	
12	$t_{CL1RH1(R)}$	t_{RSHr}	$\overline{RAS}$ Hold Time (Read Cycle)	30		35		40		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15		15		15		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	0		0		0		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		20		25		30	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		30		35		40	ns	6,7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		85		100		120	ns	6,8,9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		40		45		55	ns	6,7, 10

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	85/L		100/L		120/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		ns	17
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	20	0	25	0	30	ns	17
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	60		70		80		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	45	20	55	25	65	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH\,w}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	30		35		40		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		35		40	80	ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		20		25		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		20		25		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	60		70		80		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35		40		ns	
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data in Hold Time	15		20		25		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	20		25		30		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	25		30		35		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	225		265		305		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	150		175		205		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	60		70		80		ns	12

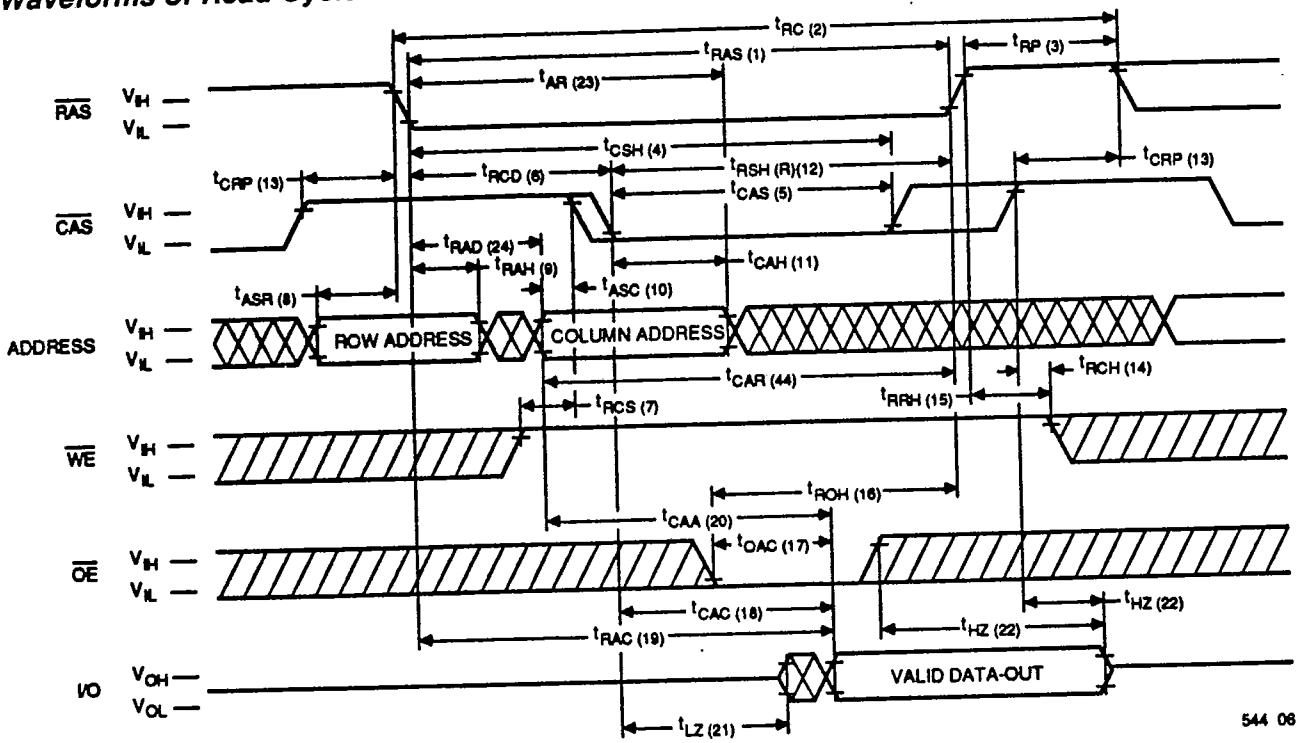
AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	85/L		10/L		12/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	115		135		160		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	95		110		125		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	70		80		85		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	55		65		75		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	15		20		25		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	40		45		55		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		50		55		65	ns	7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	60		70		80		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	25		30		40		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	115		135		155		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	15
		t_{RI}	Refresh Interval (512 Cycles)		8		8		8	ms	17

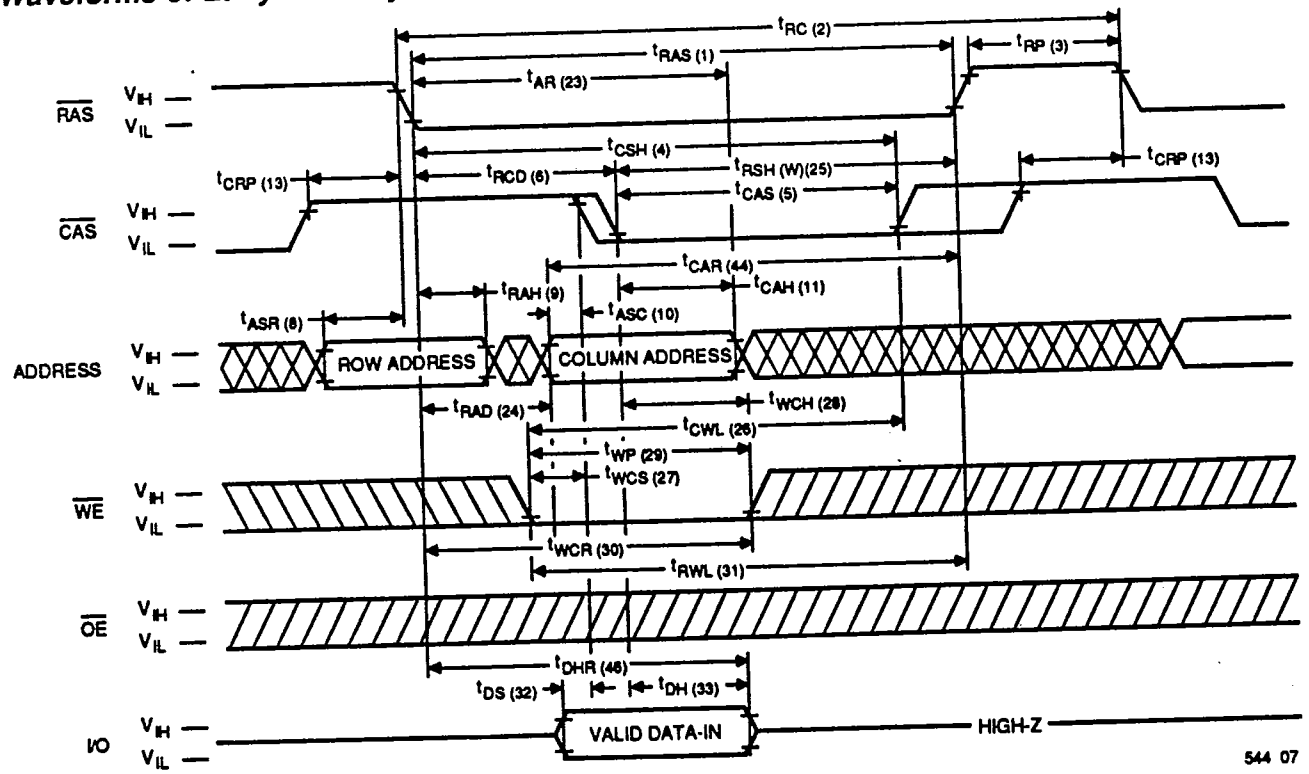
Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longer of t_{CAA}, t_{CAC} or t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

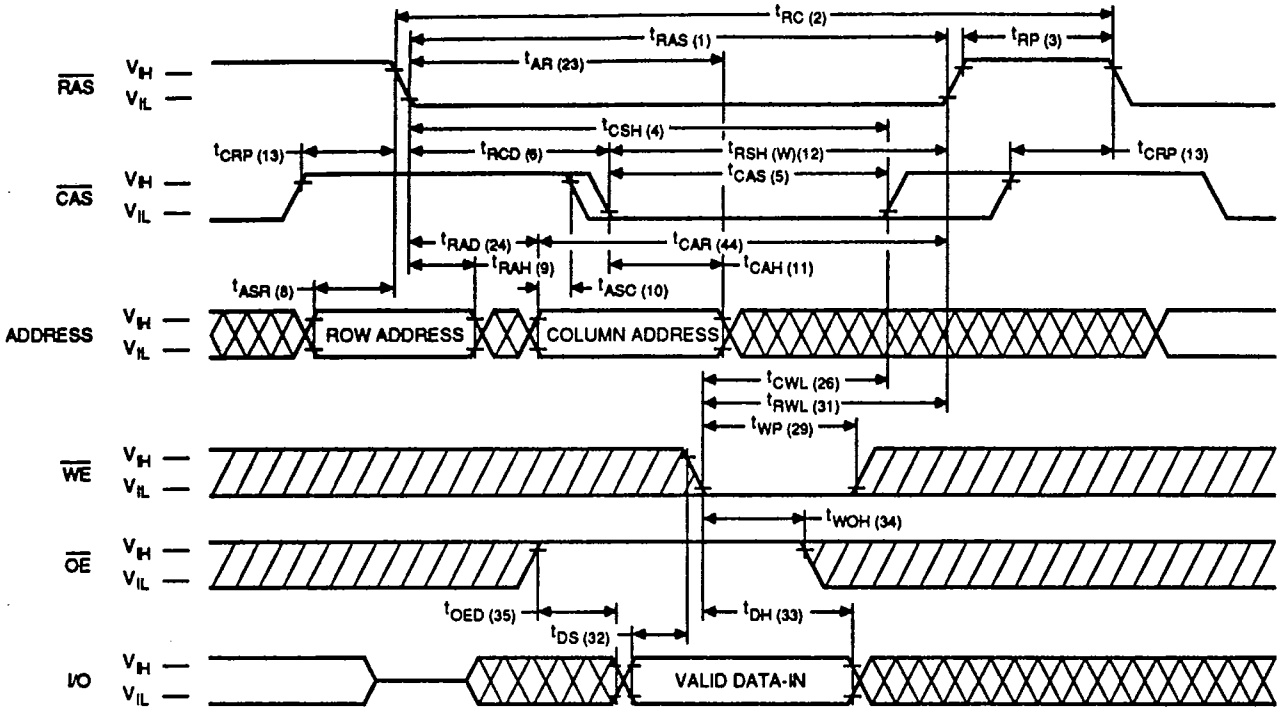
Waveforms of Read Cycle



Waveforms of Early Write Cycle

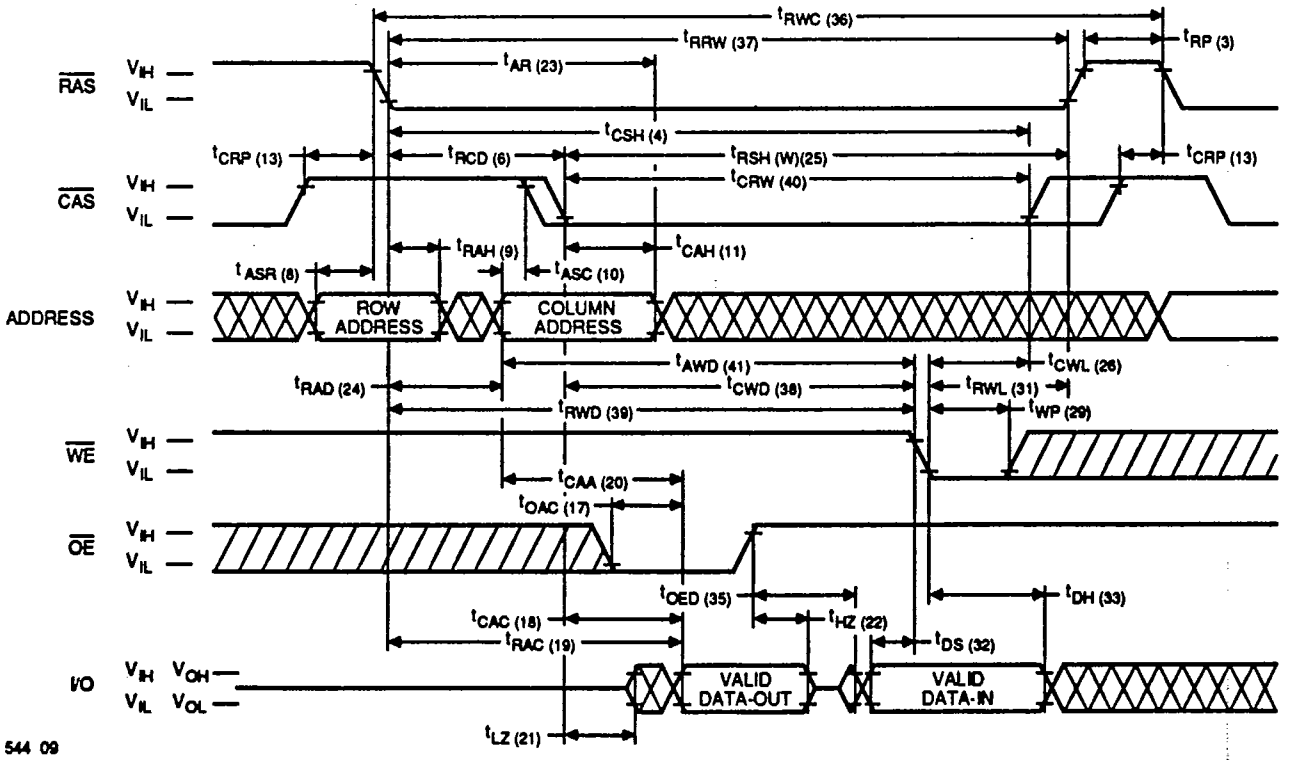


Waveforms of $\overline{OE}$ Controlled Write Cycle



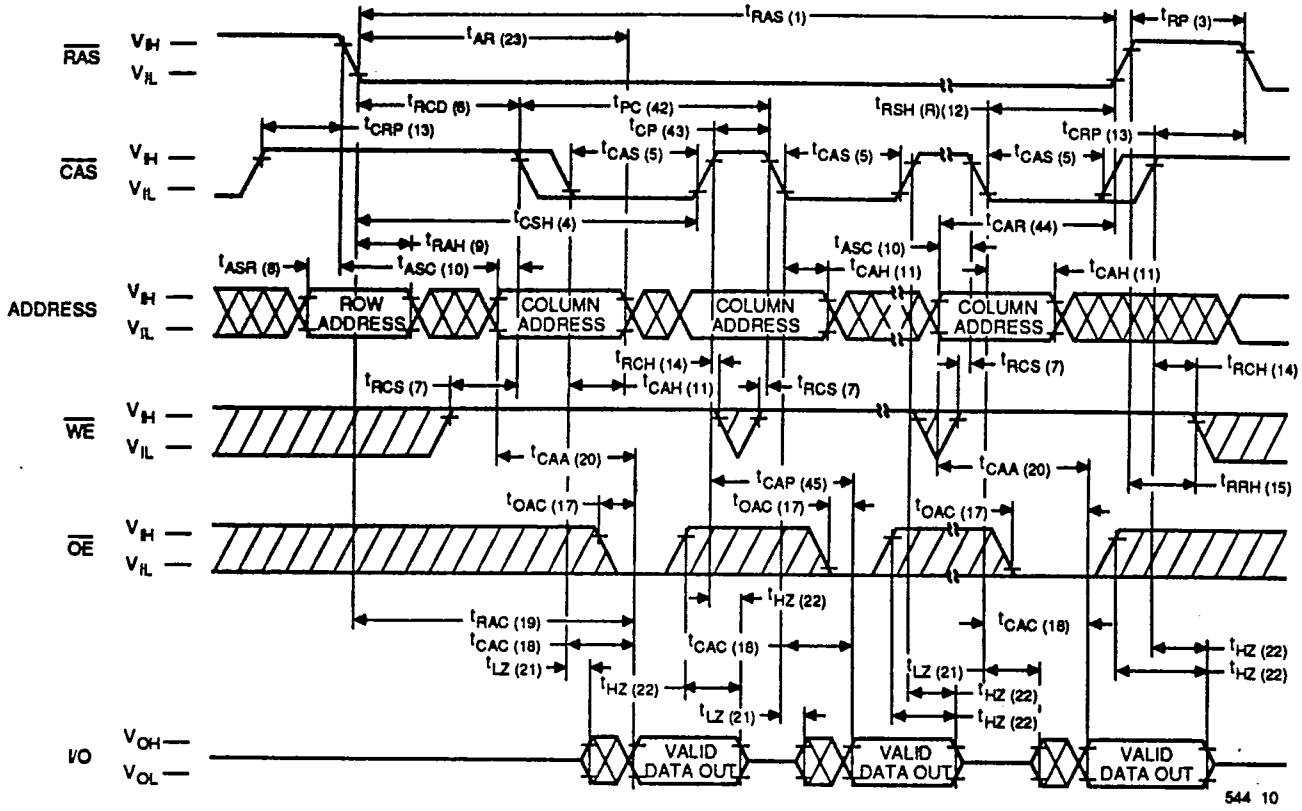
544 08

Waveforms of Read-Modify-Write Cycle

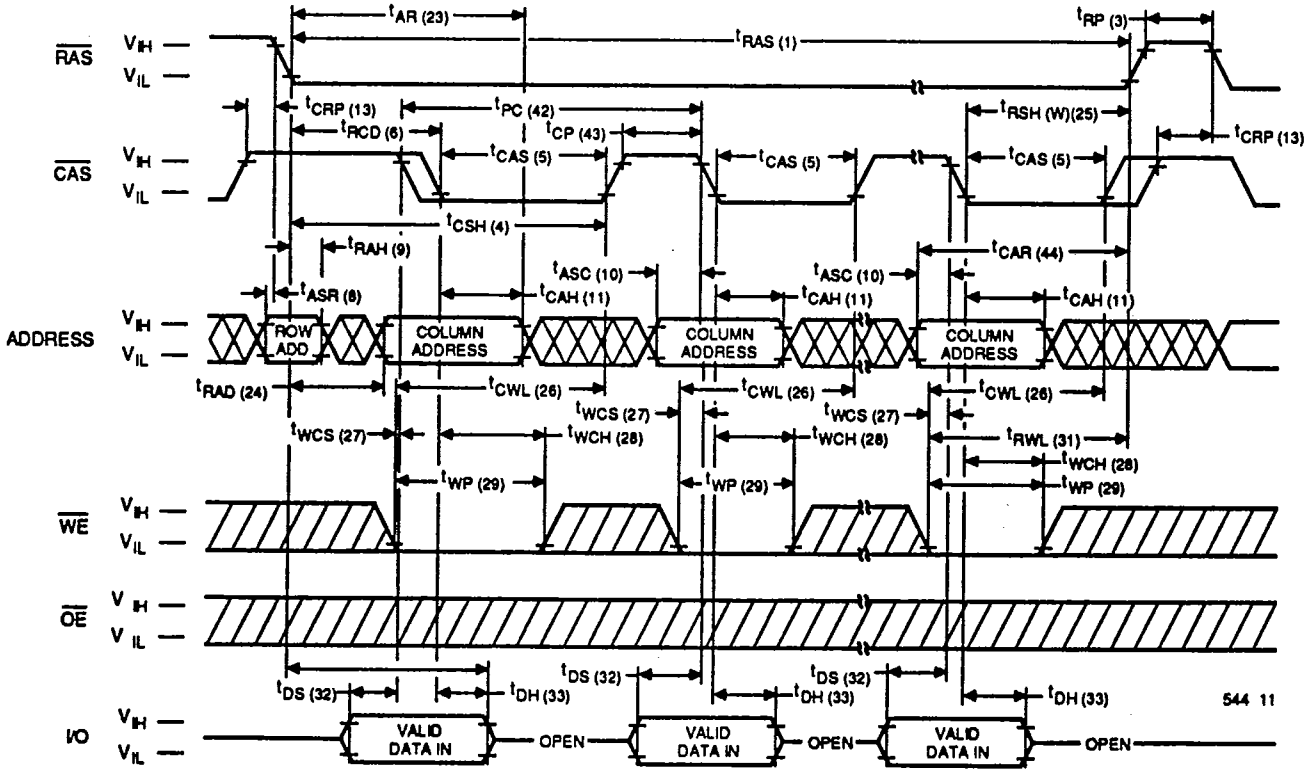


544 09

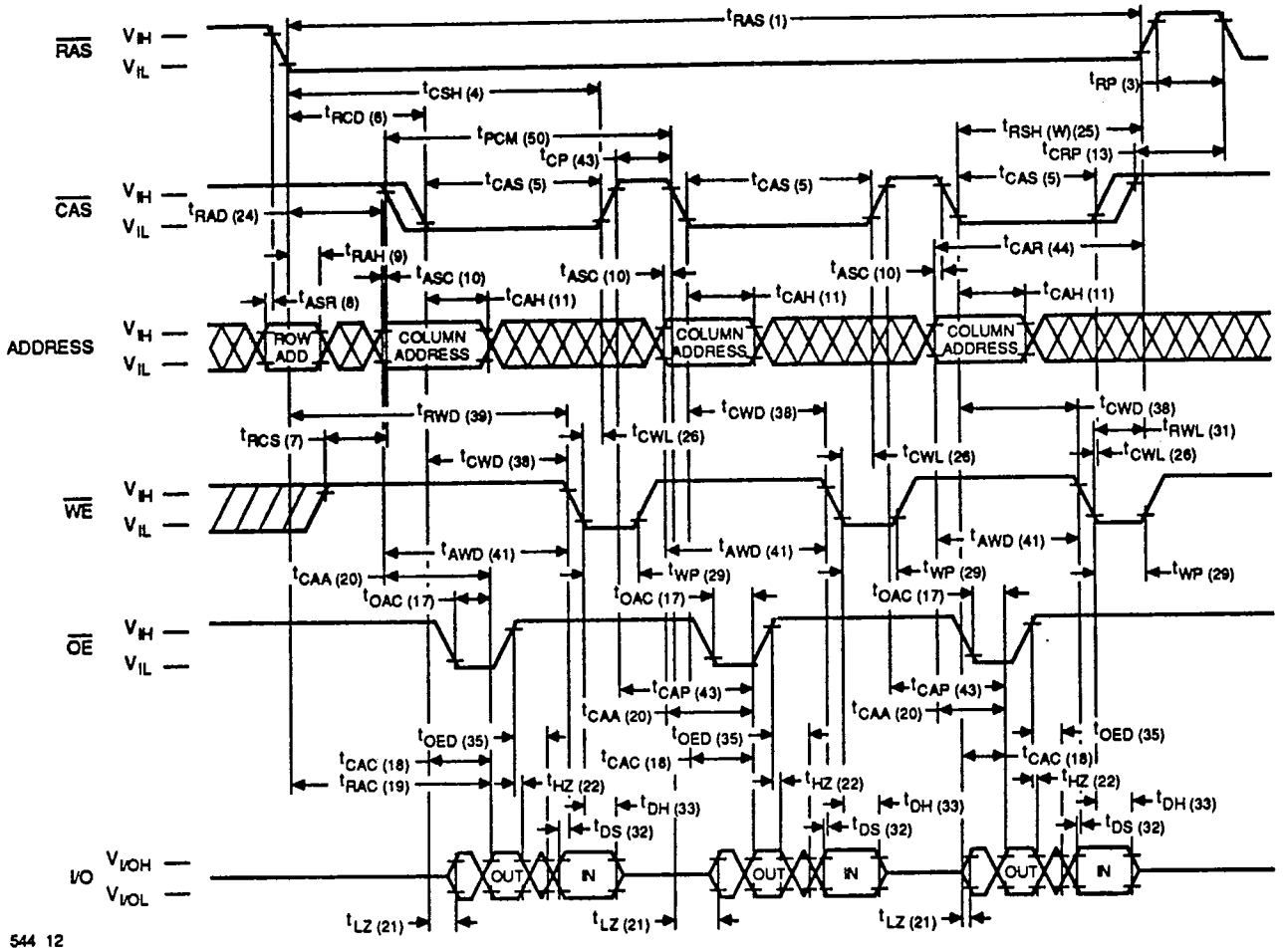
Waveforms of Fast Page Mode Read Cycle



Waveforms of Fast Page Mode Write Cycle

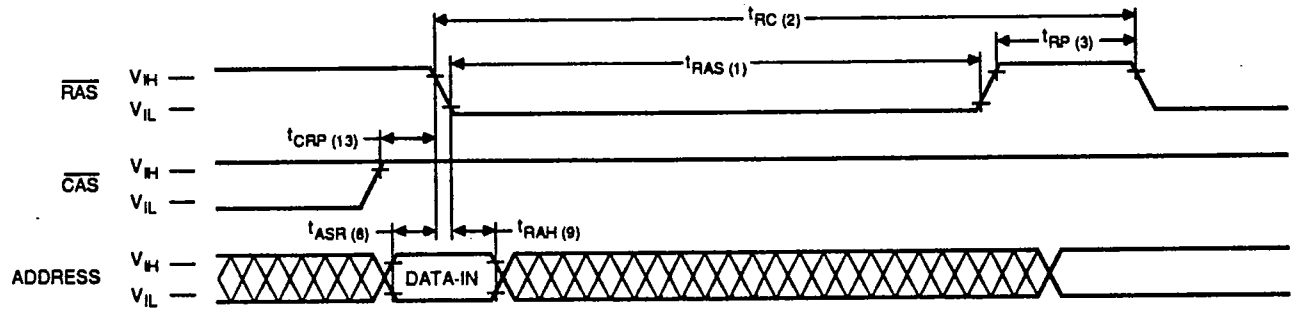


Waveforms of Fast Page Mode Read-Write Cycle



544 12

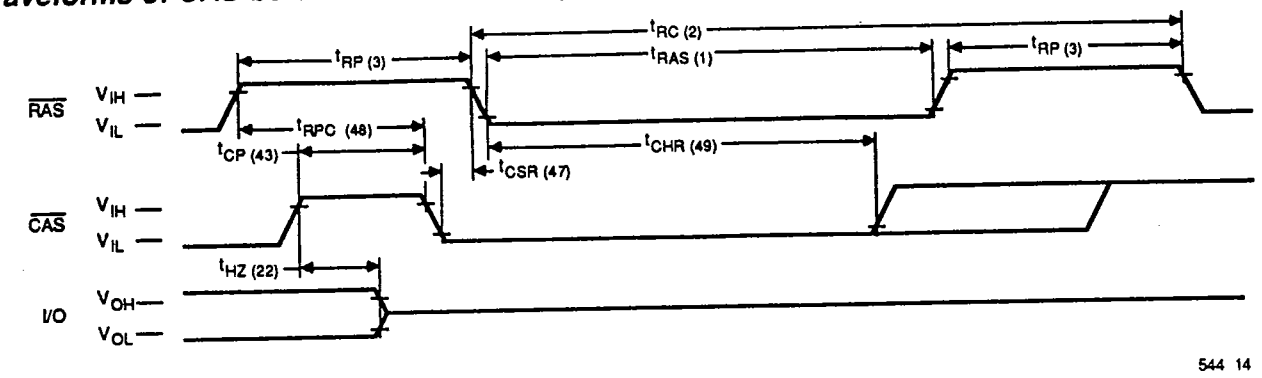
Waveforms of RAS-Only Refresh Cycle



544 13

NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

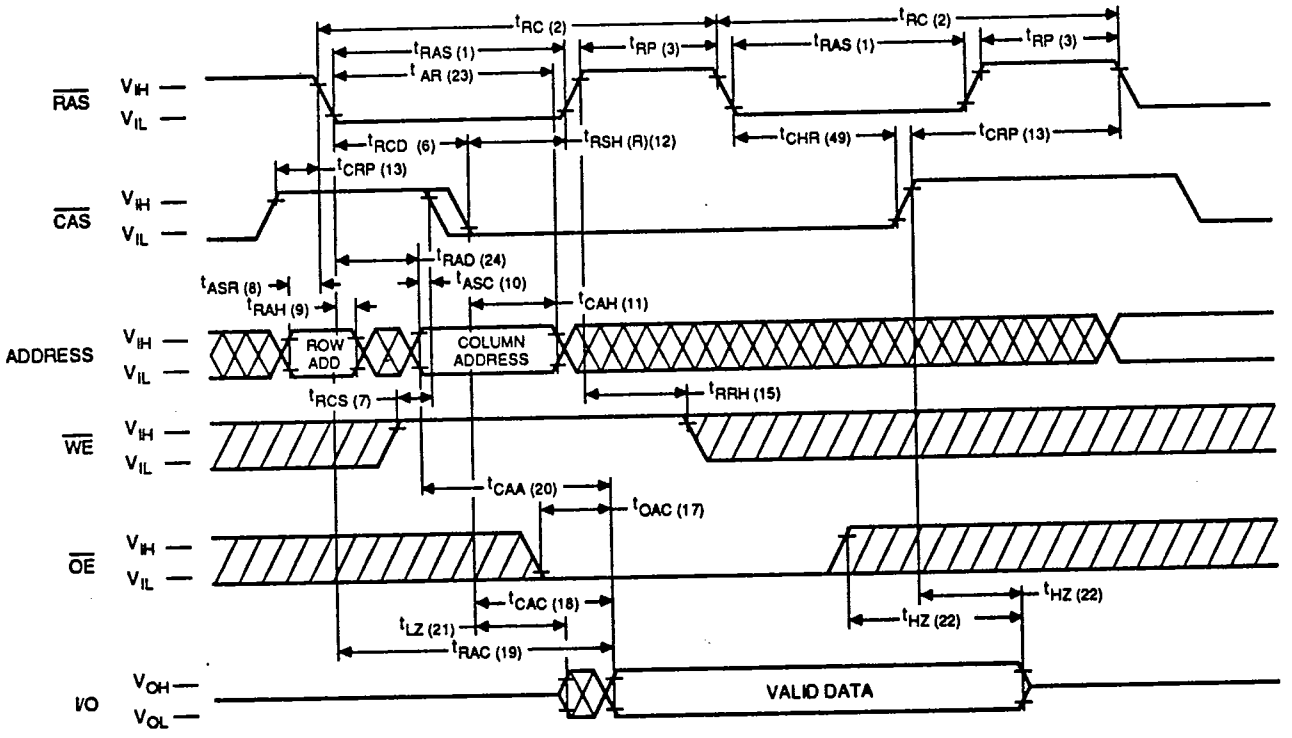
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



544 14

NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_7 = Don't care

Waveforms of Hidden Refresh Cycle (Read)



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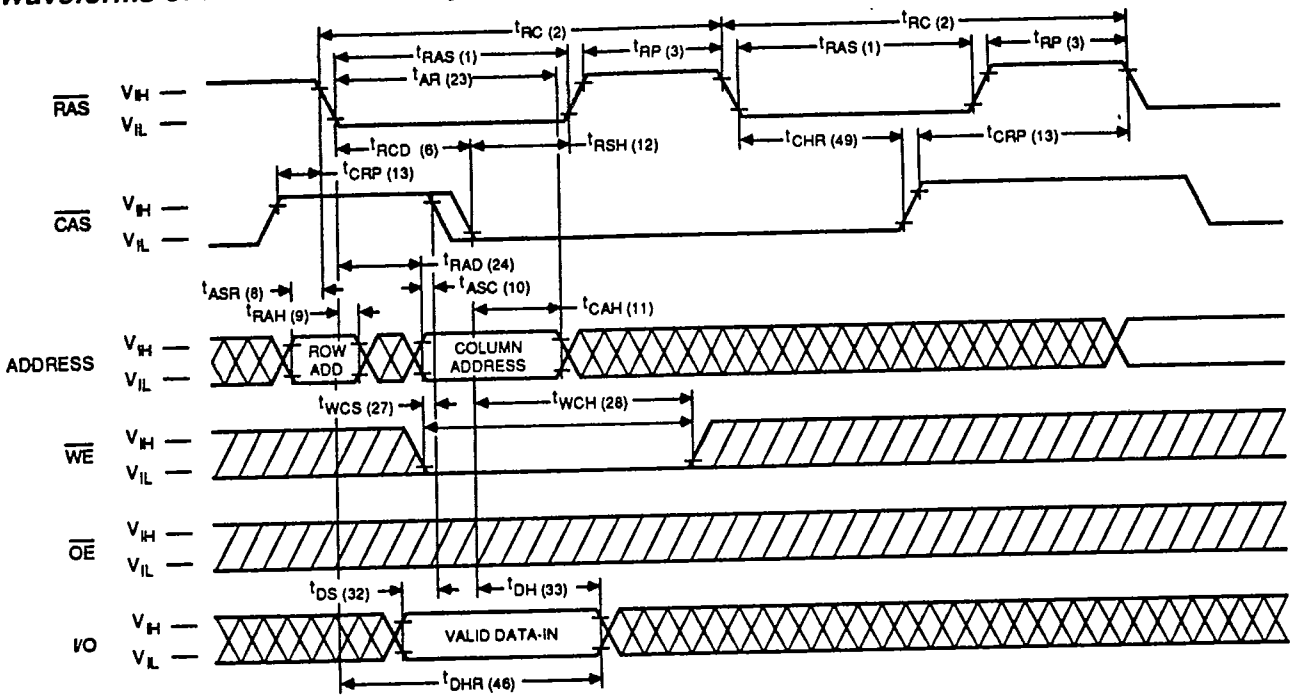
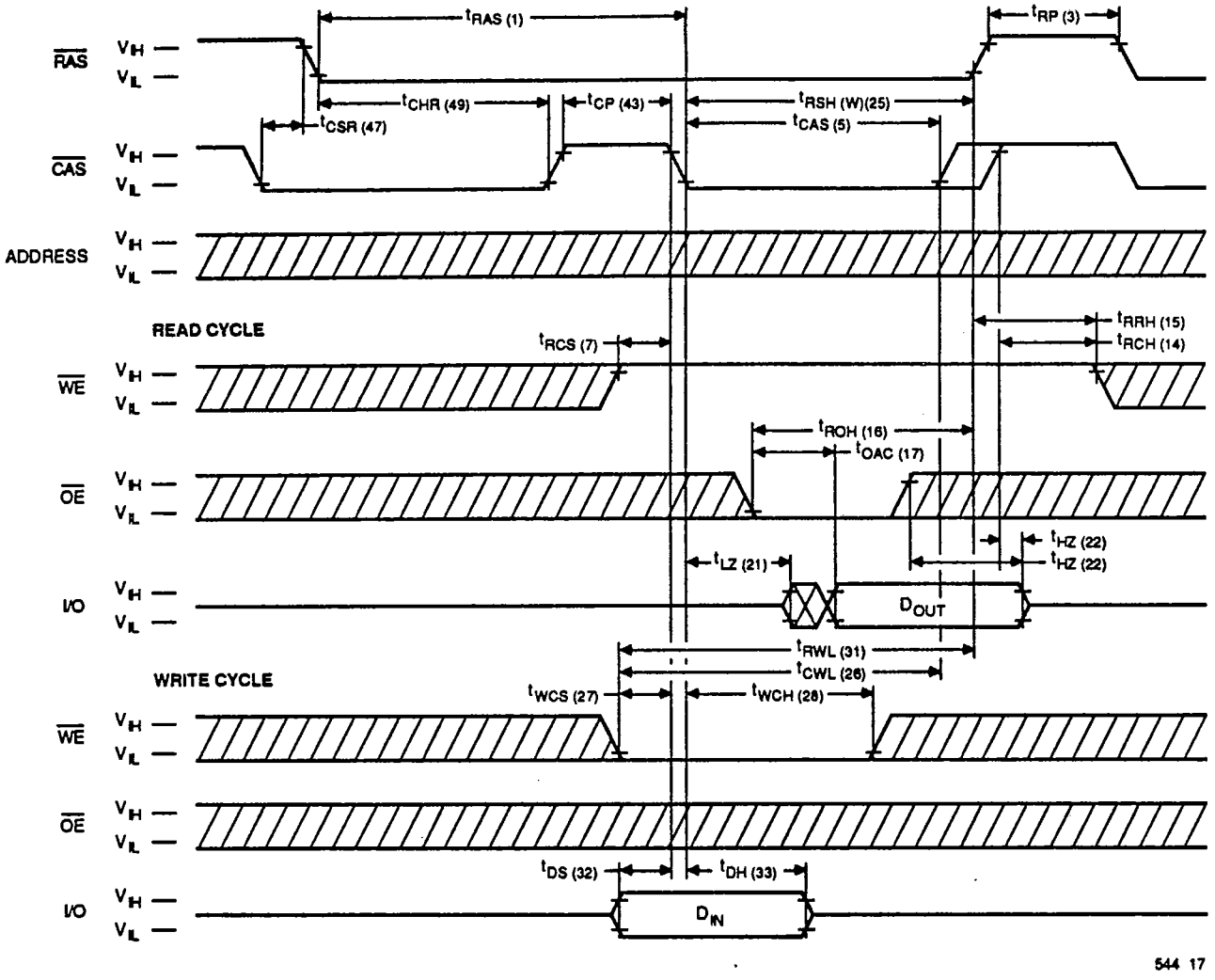
Waveforms of Hidden Refresh Cycle (Write)



544 16

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Functional Description

The V53C104 is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C104 reads and writes data by multiplexing a 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The colunm address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A0 through A8) with $\overline{RAS}$ at least once every 8 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C104 will use the output of an internal 9-bit counter as the source or row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output will remain in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C104 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C104 power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{ACTIVE}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Fast Page Mode Operation

Fast Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of over 18 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

Data Output Operation

The V53C104 Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power On

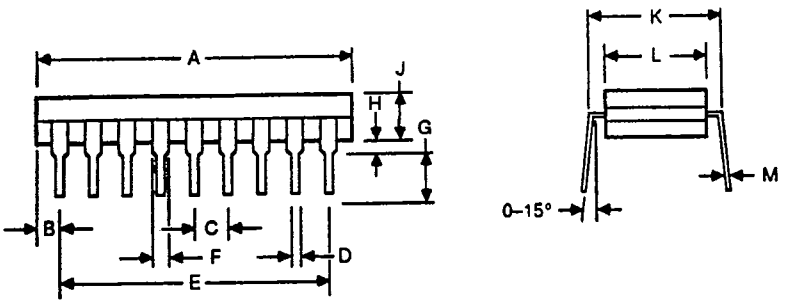
After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a RAS clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During power on, the V_{DD} current requirement of the V53C104 is dependant on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power On to avoid current surges.

Table 1. Vitelic V53C104 Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controllled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

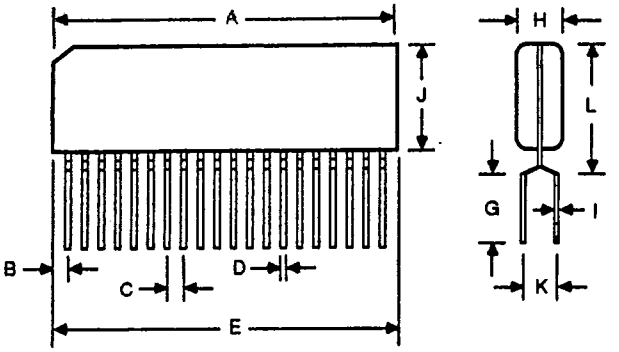
Package Outline



526 18

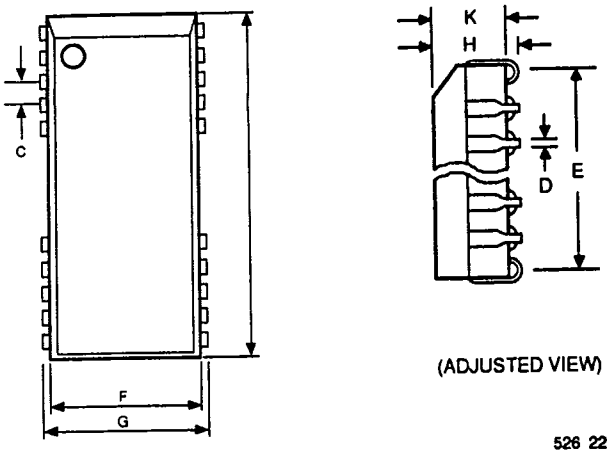
20 Pin Plastic DIP

Dimension	Inches	Millimeters
A	.920 max.	23.368 max.
B	.060	1.524
C	.090/.110	2.286/2.794
D	.015/.020	.381/.508
E	.900	22.86
F	.040/.065	1.016/1.651
G	.125/.150	3.175/3.810
H	.005/.050	.127/1.270
I	—	—
J	.130/.180	3.302/4.572
K	.330 max.	8.382 max.
L	.300 max.	7.62 max.
M	.009/.012	.229/.305
N	—	—



20 Pin ZIP Package

Dimension	Inches	Millimeters
A	1.055 max.	26.80 max.
B	.053	1.346
C	.050	1.27
D	.016/.024	.40/.60
E	.950	24.13
F	—	—
G	.118 min.	3.0 min.
H	.104/.120	2.65/3.05
I	.008/.012	0.20/0.30
J	.270/.300	6.858/7.62
K	.100	2.54
L	.345 max.	8.763 max.
M	—	—
N	—	—



(ADJUSTED VIEW)

526 22

26 SOJ

Dimension	Inches	Millimeters
A	.487/.493	12.37/12.52
B	.045 x 45°	1.14 x 45°
C	.050 Typ.	1.27 Typ.
D	.017	.043
E	.457/.463	11.61/11.76
F	.287/.293	7.29/7.44
G	.317/.327	8.05/8.31
H	.133/.139	3.38/3.53
I	—	—
J	.517/.527	13.13/13.39
K	.110	2.79
L	.257/.263	6.53/6.69
M	—	—
N	—	—