

**MOSEL VITELIC**

**V53C8126H  
ULTRA-HIGH PERFORMANCE,  
128K X 8 BIT FAST PAGE MODE  
CMOS DYNAMIC RAM**

**PRELIMINARY**

HIGH PERFORMANCE	35	40	45	50
Max. $\overline{\text{RAS}}$ Access Time, ( $t_{\text{RAC}}$ )	35 ns	40 ns	45 ns	50 ns
Max. Column Address Access Time, ( $t_{\text{CAA}}$ )	18 ns	20 ns	22 ns	24 ns
Min. Fast Page Mode Cycle Time, ( $t_{\text{PC}}$ )	21 ns	23 ns	25 ns	28 ns
Min. Read/Write Cycle Time, ( $t_{\text{RC}}$ )	70 ns	75 ns	80 ns	90 ns

**Features**

- 128K x 8-bit organization
- $\overline{\text{RAS}}$  access time: 35, 40, 45, 50 ns
- Fast Page Mode supports sustained I/O data rates up to 40 MHz
- Read-Modify-Write,  $\overline{\text{RAS}}$ -Only Refresh,  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh capability
- Refresh Interval
  - V53C8126H – 512 cycles/8 ms
- Available in 26/24 pin 300 mil SOJ and 28 pin TSOP package

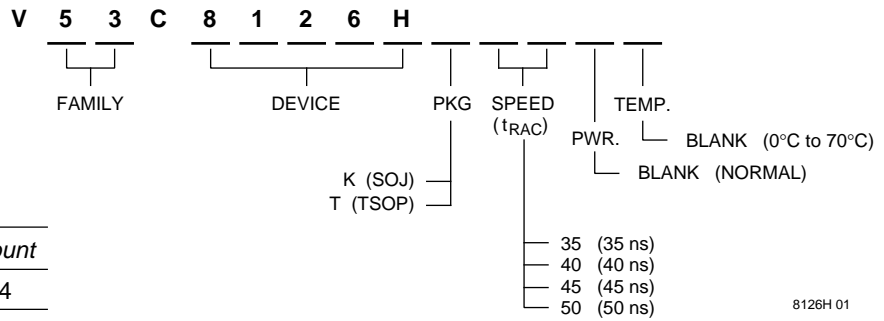
**Description**

The V53C8126H is a high speed 131,072 x 8 bit CMOS dynamic random access memory. The V53C8126H offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 256 columns (x8) bits within a row with cycle times as short as 21 ns. Because of static circuitry, the  $\overline{\text{CAS}}$  clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C8126H ideally suited for graphics, digital signal processing and high performance peripherals.

**Device Usage Chart**

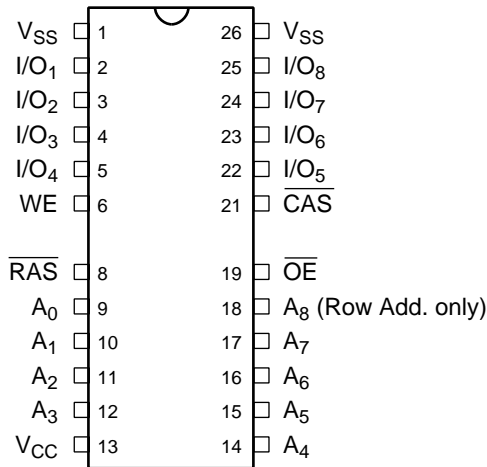
Operating Temperature Range	Package Outline		Access Time (ns)				Power	Temperature Mark
	K	T	35	40	45	50	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	Blank



Description	Pkg.	Pin Count
SOJ	K	26/24

8126H 01

**26/24 Lead SOJ  
PIN CONFIGURATION  
Top View**



8126H 02

**28 Lead TSOP  
PIN CONFIGURATION  
Top View**



8125H 03

**Pin Names**

$A_0-A_8$	Address Inputs ( $A_8$ : Row Address only)
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$I/O_1-I/O_8$	Data Input, Output
$V_{CC}$	+5V Supply
$V_{SS}$	0V Supply
NC	No Connect

**Absolute Maximum Ratings\***

Ambient Temperature

Under Bias ..... -10°C to +80°C

Storage Temperature (plastic) .... -55°C to +125°C

Voltage Relative to  $V_{SS}$  ..... -1.0 V to +7.0 V

Data Output Current ..... 50 mA

Power Dissipation ..... 1.0 W

\*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

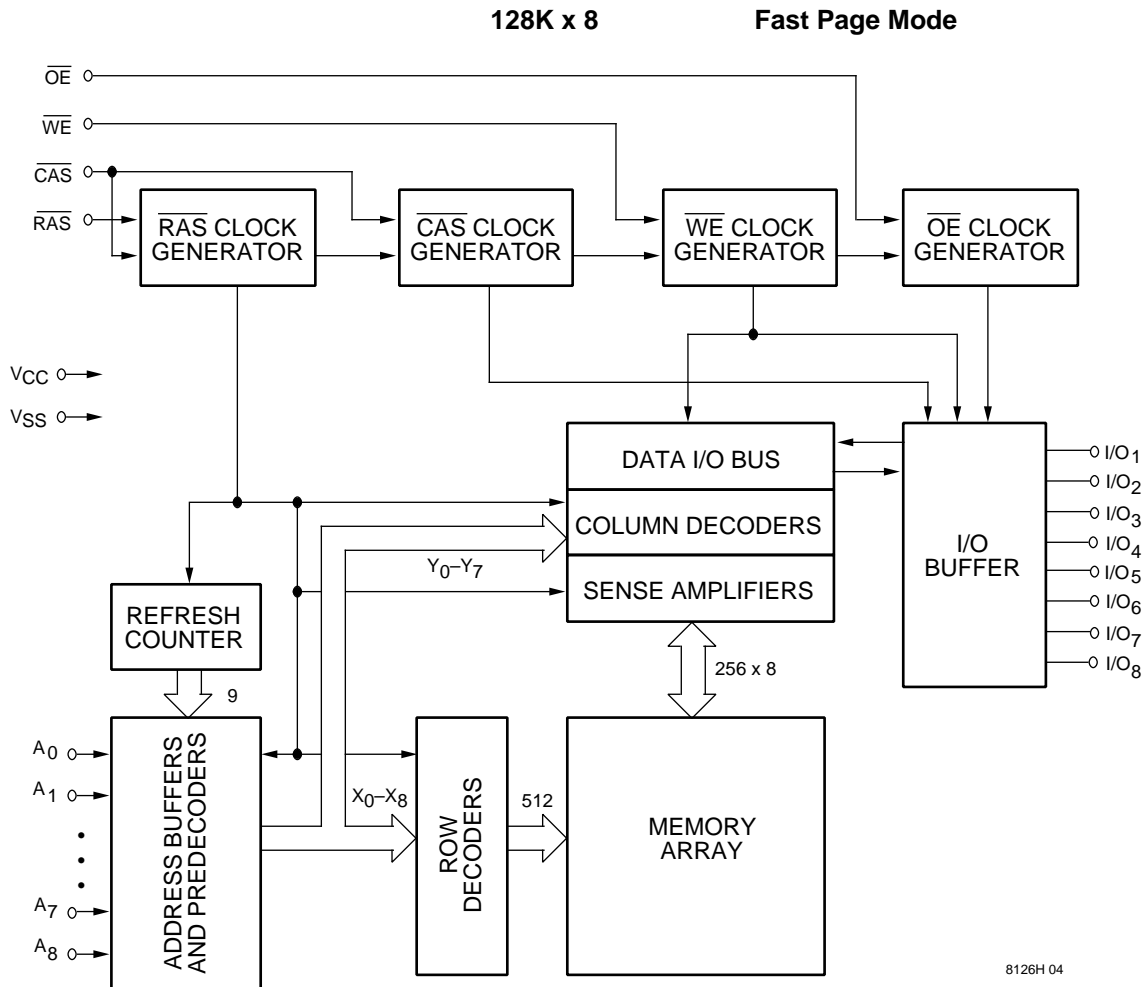
**Capacitance\***

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$

Symbol	Parameter	Typ.	Max.	Unit
$C_{IN1}$	Address Input	3	4	pF
$C_{IN2}$	$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{OE}$	4	5	pF
$C_{OUT}$	Data Input/Output	5	7	pF

\* Note: Capacitance is sampled and not 100% tested

**Block Diagram**



8126H 04

**DC and Operating Characteristics (1-2)**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ , unless otherwise specified.

Symbol	Parameter	Access Time	V53C8126H			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
$I_{LI}$	Input Leakage Current (any input pin)		-10		10	$\mu\text{A}$	$V_{SS} \leq V_{IN} \leq V_{CC}$	
$I_{LO}$	Output Leakage Current (for High-Z State)		-10		10	$\mu\text{A}$	$V_{SS} \leq V_{OUT} \leq V_{CC}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$ at $V_{IH}$	
$I_{CC1}$	$V_{CC}$ Supply Current, Operating	35			160	mA	$t_{RC} = t_{RC}(\text{min.})$	1, 2
		40			150			
		45			145			
		50			135			
$I_{CC2}$	$V_{CC}$ Supply Current, TTL Standby				4	mA	$\overline{\text{RAS}}, \overline{\text{CAS}}$ at $V_{IH}$ other inputs $\geq V_{SS}$	
$I_{CC3}$	$V_{CC}$ Supply Current, $\overline{\text{RAS}}$ -Only Refresh	35			160	mA	$t_{RC} = t_{RC}(\text{min.})$	2
		40			150			
		45			145			
		50			135			
$I_{CC4}$	$V_{CC}$ Supply Current, Fast Page Mode Operation	35			95	mA	Minimum Cycle	1, 2
		40			90			
		45			85			
		50			80			
$I_{CC5}$	$V_{CC}$ Supply Current, Standby, Output Enabled				2	mA	$\overline{\text{RAS}} = V_{IH}, \overline{\text{CAS}} = V_{IL}$ other inputs $\geq V_{SS}$	1
$I_{CC6}$	$V_{CC}$ Supply Current, CMOS Standby				1	mA	$\overline{\text{RAS}} \geq V_{CC} - 0.2\text{ V},$ $\overline{\text{CAS}} \geq V_{CC} - 0.2\text{ V},$ All other inputs $\geq V_{SS}$	
$V_{IL}$	Input Low Voltage		-1		0.8	V		3
$V_{IH}$	Input High Voltage		2.4		$V_{CC} + 1$	V		3
$V_{OL}$	Output Low Voltage				0.4	V	$I_{OL} = 4.2\text{ mA}$	
$V_{OH}$	Output High Voltage		2.4			V	$I_{OH} = -5\text{ mA}$	

**AC Characteristics**

T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 5 V ±10%, V<sub>SS</sub> = 0V unless otherwise noted  
 AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	35		40		45		50		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t <sub>RL1RH1</sub>	t <sub>RAS</sub>	$\overline{\text{RAS}}$ Pulse Width	35	75K	40	75K	45	75K	50	75K	ns	
2	t <sub>RL2RL2</sub>	t <sub>RC</sub>	Read or Write Cycle Time	70		75		80		90		ns	
3	t <sub>RH2RL2</sub>	t <sub>RP</sub>	$\overline{\text{RAS}}$ Precharge Time	25		25		25		30		ns	
4	t <sub>RL1CH1</sub>	t <sub>CSH</sub>	$\overline{\text{CAS}}$ Hold Time	35		40		45		50		ns	
5	t <sub>CL1CH1</sub>	t <sub>CAS</sub>	$\overline{\text{CAS}}$ Pulse Width	12		12		13		14		ns	
6	t <sub>RL1CL1</sub>	t <sub>RCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	16	23	17	28	18	32	19	36	ns	
7	t <sub>WH2CL2</sub>	t <sub>RCS</sub>	Read Command Setup Time	0		0		0		0		ns	4
8	t <sub>AVRL2</sub>	t <sub>ASR</sub>	Row Address Setup Time	0		0		0		0		ns	
9	t <sub>RL1AX</sub>	t <sub>RAH</sub>	Row Address Hold Time	6		7		8		9		ns	
10	t <sub>AVCL2</sub>	t <sub>ASC</sub>	Column Address Setup Time	0		0		0		0		ns	
11	t <sub>CL1AX</sub>	t <sub>CAH</sub>	Column Address Hold Time	4		5		6		7		ns	
12	t <sub>CL1RH1(R)</sub>	t <sub>RSH (R)</sub>	$\overline{\text{RAS}}$ Hold Time (Read Cycle)	12		12		13		14		ns	
13	t <sub>CH2RL2</sub>	t <sub>CRP</sub>	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5		5		5		5		ns	
14	t <sub>CH2WX</sub>	t <sub>RCH</sub>	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	0		0		0		0		ns	5
15	t <sub>RH2WX</sub>	t <sub>RRH</sub>	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	0		0		0		0		ns	5
16	t <sub>OEL1RH2</sub>	t <sub>ROH</sub>	$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	8		8		9		10		ns	
17	t <sub>GL1QV</sub>	t <sub>OAC</sub>	Access Time from $\overline{\text{OE}}$		12		12		13		14	ns	
18	t <sub>CL1QV</sub>	t <sub>CAC</sub>	Access Time from $\overline{\text{CAS}}$		12		12		13		14	ns	6, 7
19	t <sub>RL1QV</sub>	t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}$		35		40		45		50	ns	6, 8, 9
20	t <sub>AVQV</sub>	t <sub>CAA</sub>	Access Time from Column Address		18		20		22		24	ns	6, 7, 10
21	t <sub>CL1QX</sub>	t <sub>LZ</sub>	$\overline{\text{OE}}$ or $\overline{\text{CAS}}$ to Low-Z Output	0		0		0		0		ns	16
22	t <sub>CH2QZ</sub>	t <sub>HZ</sub>	$\overline{\text{OE}}$ or $\overline{\text{CAS}}$ to High-Z Output	0	6	0	6	0	7	0	8	ns	16
23	t <sub>RL1AX</sub>	t <sub>AR</sub>	Column Address Hold Time from $\overline{\text{RAS}}$	28		30		35		40		ns	
24	t <sub>RL1AV</sub>	t <sub>RAD</sub>	$\overline{\text{RAS}}$ to Column Address Delay Time	11	17	12	20	13	23	14	26	ns	11
25	t <sub>CL1RH1(W)</sub>	t <sub>RSH (W)</sub>	$\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ Hold Time in Write Cycle	12		12		13		14		ns	
26	t <sub>WL1CH1</sub>	t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time	12		12		13		14		ns	

**AC Characteristics (Cont'd)**

#	JEDEC Symbol	Symbol	Parameter	35		40		45		50		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
27	t <sub>WL1CL2</sub>	t <sub>WCS</sub>	Write Command Setup Time	0		0		0		0		ns	12, 13
28	t <sub>CL1WH1</sub>	t <sub>WCH</sub>	Write Command Hold Time	5		5		6		7		ns	
29	t <sub>WL1WH1</sub>	t <sub>WP</sub>	Write Pulse Width	5		5		6		7		ns	
30	t <sub>RL1WH1</sub>	t <sub>WCR</sub>	Write Command Hold Time from $\overline{\text{RAS}}$	28		30		35		40		ns	
31	t <sub>WL1RH1</sub>	t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time	12		12		13		14		ns	
32	t <sub>DVWL2</sub>	t <sub>DS</sub>	Data in Setup Time	0		0		0		0		ns	14
33	t <sub>WL1DX</sub>	t <sub>DH</sub>	Data in Hold Time	4		5		6		7		ns	14
34	t <sub>WL1GL2</sub>	t <sub>WOH</sub>	Write to $\overline{\text{OE}}$ Hold Time	5		6		7		8		ns	14
35	t <sub>GH2DX</sub>	t <sub>OED</sub>	$\overline{\text{OE}}$ to Data Delay Time	5		6		7		8		ns	14
36	t <sub>RL2RL2 (RMW)</sub>	t <sub>RWC</sub>	Read-Modify-Write Cycle Time	105		110		115		130		ns	
37	t <sub>RL1RH1 (RMW)</sub>	t <sub>RRW</sub>	Read-Modify-Write Cycle $\overline{\text{RAS}}$ Pulse Width	70		75		80		87		ns	
38	t <sub>CL1WL2</sub>	t <sub>CWD</sub>	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	28		30		32		34		ns	12
39	t <sub>RL1WL2</sub>	t <sub>RWD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay in Read-Modify-Write Cycle	54		58		62		68		ns	12
40	t <sub>CL1CH1</sub>	t <sub>CRW</sub>	$\overline{\text{CAS}}$ Pulse Width (RMW)	46		48		50		52		ns	
41	t <sub>AVWL2</sub>	t <sub>AWD</sub>	Col. Address to $\overline{\text{WE}}$ Delay	35		38		41		42		ns	12
42	t <sub>CL2CL2</sub>	t <sub>PC</sub>	Fast Page Mode Read or Write Cycle Time	21		23		25		28		ns	
43	t <sub>CH2CL2</sub>	t <sub>CP</sub>	$\overline{\text{CAS}}$ Precharge Time	4		5		6		7		ns	
44	t <sub>AVRH1</sub>	t <sub>CAR</sub>	Column Address to $\overline{\text{RAS}}$ Setup Time	18		20		22		24		ns	
45	t <sub>CH2QV</sub>	t <sub>CAP</sub>	Access Time from Column Precharge		20		22		24		27	ns	7
46	t <sub>RL1DX</sub>	t <sub>DHR</sub>	Data in Hold Time Referenced to $\overline{\text{RAS}}$	28		30		35		40		ns	
47	t <sub>CL1RL2</sub>	t <sub>CSR</sub>	$\overline{\text{CAS}}$ Setup Time $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh	10		10		10		10		ns	
48	t <sub>RH2CL2</sub>	t <sub>RPC</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	0		0		0		0		ns	
49	t <sub>RL1CH1</sub>	t <sub>CHR</sub>	$\overline{\text{CAS}}$ Hold Time $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh	8		8		10		12		ns	
50	t <sub>CL2CL2 (RMW)</sub>	t <sub>PCM</sub>	Fast Page Mode Read-Modify-Write Cycle Time	58		60		65		70		ns	

**AC Characteristics** (Cont'd)

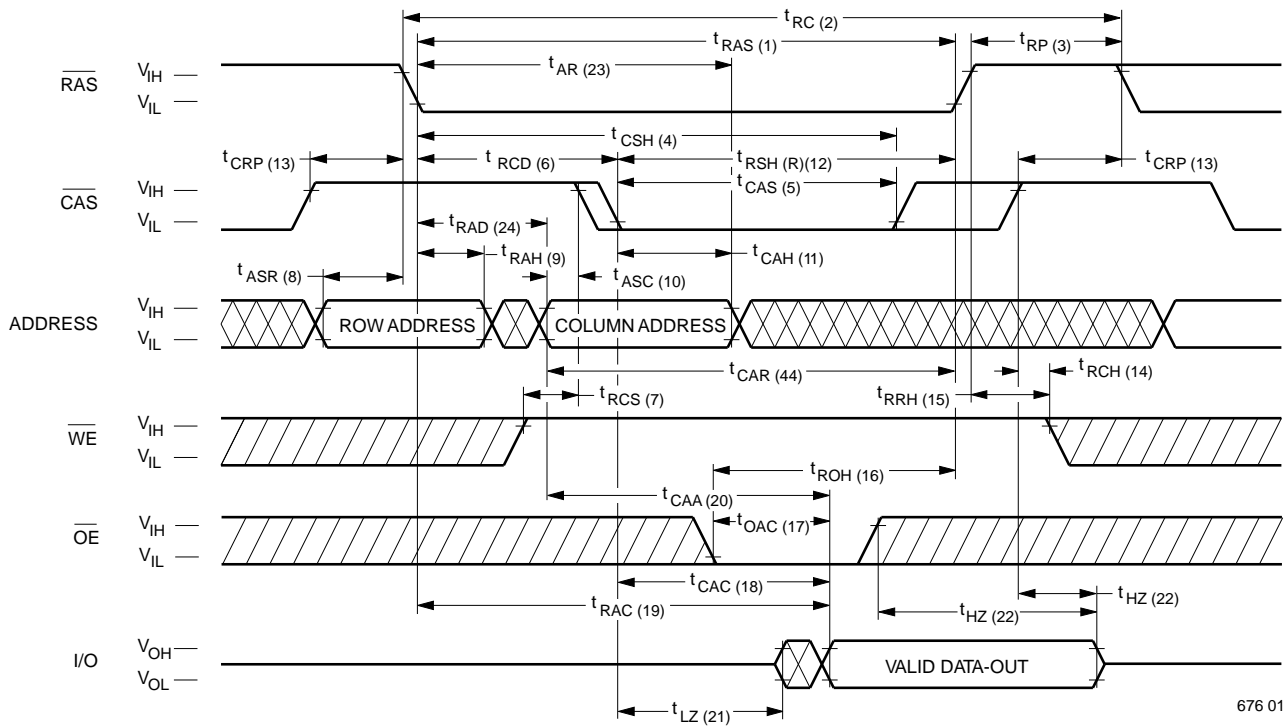
#	JEDEC Symbol	Symbol	Parameter	35		40		45		50		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
	$t_T$	$t_T$	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
		$t_{REF}$	Refresh Interval (512 Cycles)		8		8		8		8	ms	17

**Notes:**

1.  $I_{CC}$  is dependent on output loading when the device output is selected. Specified  $I_{CC}$  (max.) is measured with the output open.
2.  $I_{CC}$  is dependent upon the number of address transitions. Specified  $I_{CC}$  (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified  $V_{IL}$  (min.) is steady state operating. During transitions,  $V_{IL}$  (min.) may undershoot to  $-1.0$  V for a period not to exceed 20 ns. All AC parameters are measured with  $V_{IL}$  (min.)  $\geq V_{SS}$  and  $V_{IH}$  (max.)  $\leq V_{CC}$ .
4.  $t_{RCD}$  (max.) is specified for reference only. Operation within  $t_{RCD}$  (max.) limits insures that  $t_{RAC}$  (max.) and  $t_{CAA}$  (max.) can be met. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max.), the access time is controlled by  $t_{CAA}$  and  $t_{CAC}$ .
5. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 50 pF.
7. Access time is determined by the longest of  $t_{CAA}$ ,  $t_{CAC}$  and  $t_{CAP}$ .
8. Assumes that  $t_{RAD} \leq t_{RAD}$  (max.). If  $t_{RAD}$  is greater than  $t_{RAD}$  (max.),  $t_{RAC}$  will increase by the amount that  $t_{RAD}$  exceeds  $t_{RAD}$  (max.).
9. Assumes that  $t_{RCD} \leq t_{RCD}$  (max.). If  $t_{RCD}$  is greater than  $t_{RCD}$  (max.),  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds  $t_{RCD}$  (max.).
10. Assumes that  $t_{RAD} \geq t_{RAD}$  (max.).
11. Operation within the  $t_{RAD}$  (max.) limit ensures that  $t_{RAC}$  (max.) can be met.  $t_{RAD}$  (max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max.) limit, the access time is controlled by  $t_{CAA}$  and  $t_{CAC}$ .
12.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are not restrictive operating parameters.
13.  $t_{WCS}$  (min.) must be satisfied in an Early Write Cycle.
14.  $t_{DS}$  and  $t_{DH}$  are referenced to the latter occurrence of  $\overline{CAS}$  or  $\overline{WE}$ .
15.  $t_T$  is measured between  $V_{IH}$  (min.) and  $V_{IL}$  (max.). AC-measurements assume  $t_T = 5$  ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200  $\mu$ s pause and 8  $\overline{RAS}$ -containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

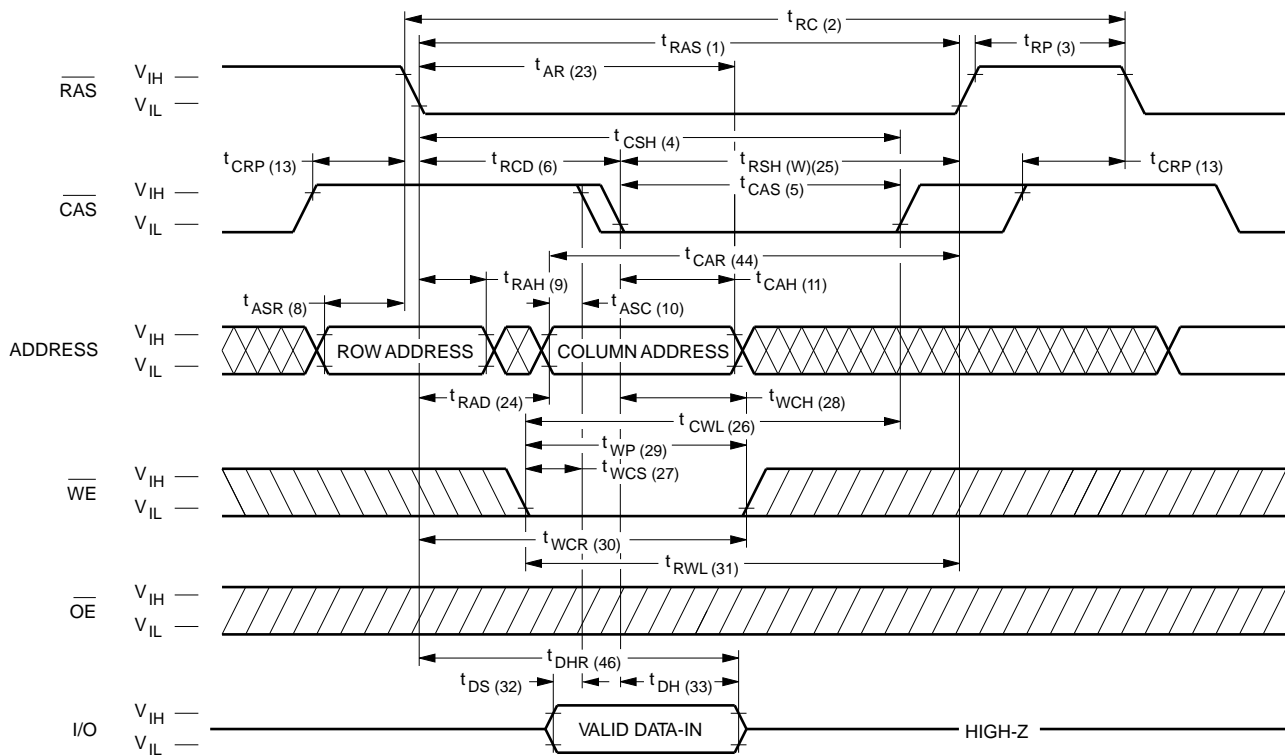


Waveforms of Read Cycle



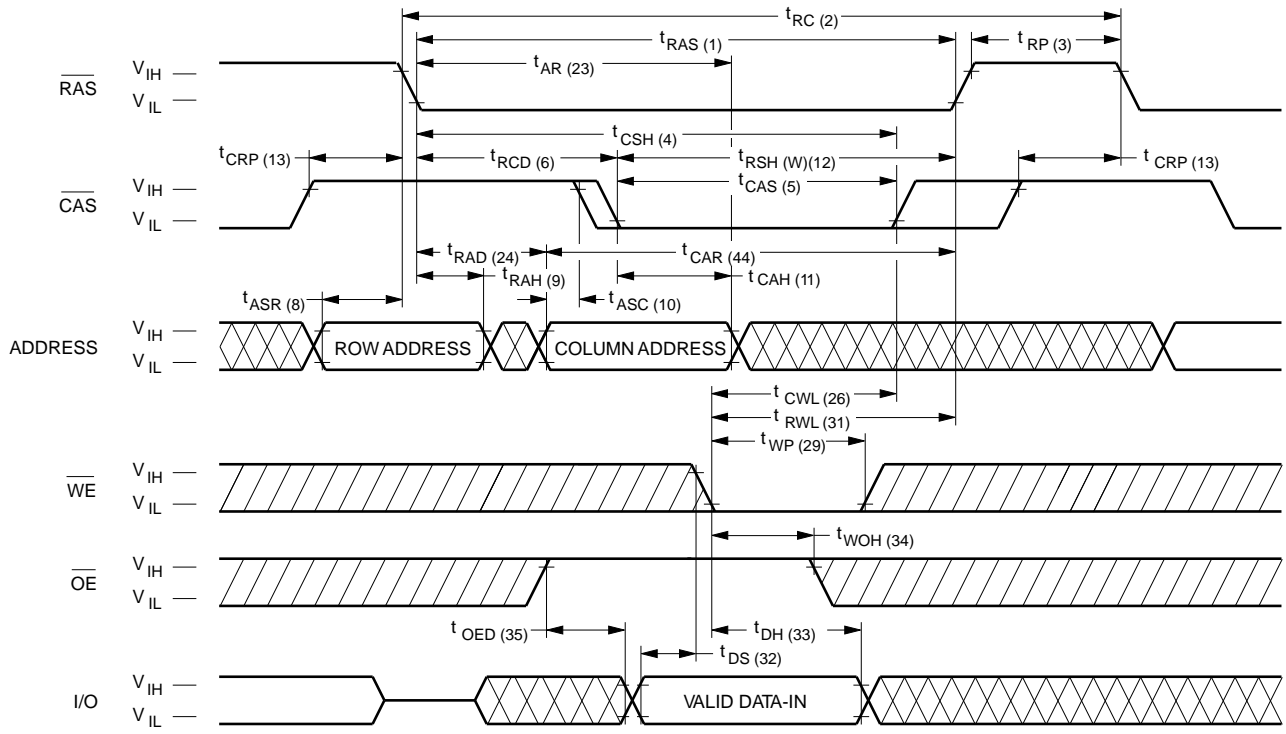
676 01

Waveforms of Early Write Cycle



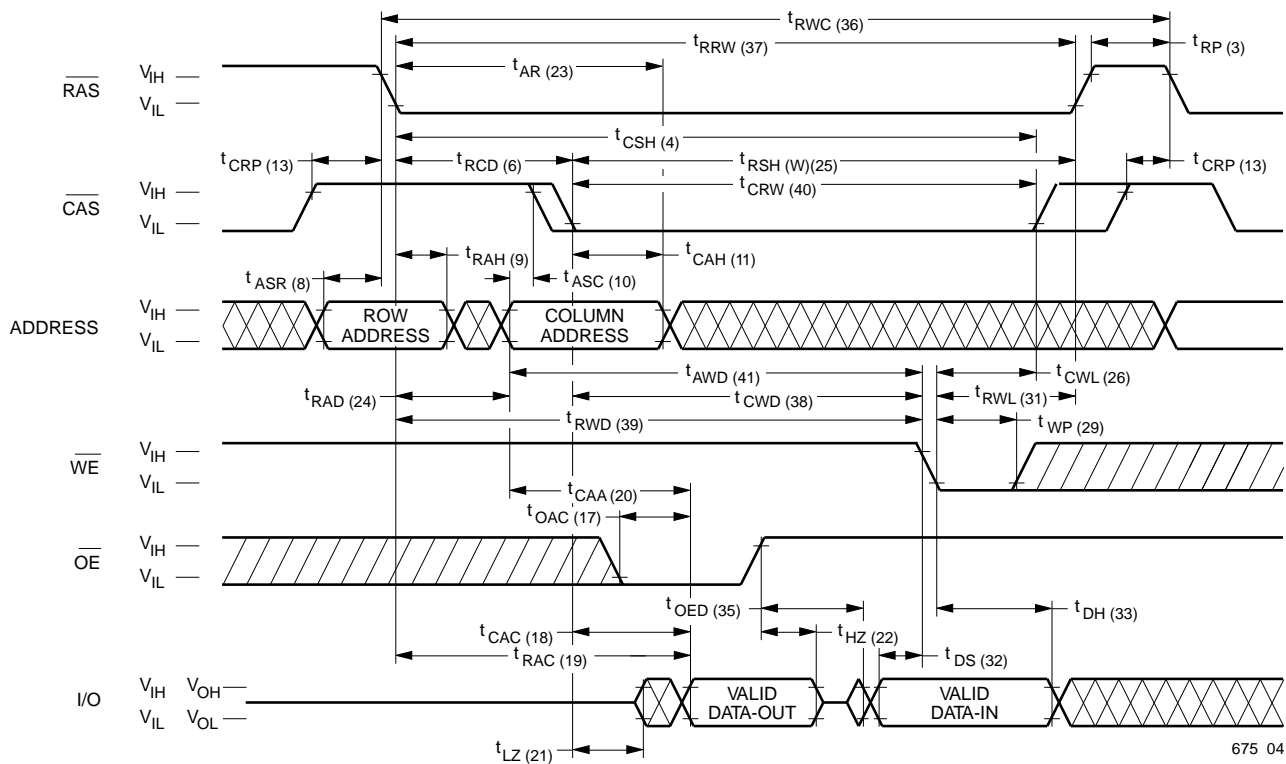
676 02

Waveforms of OE-Controlled Write Cycle



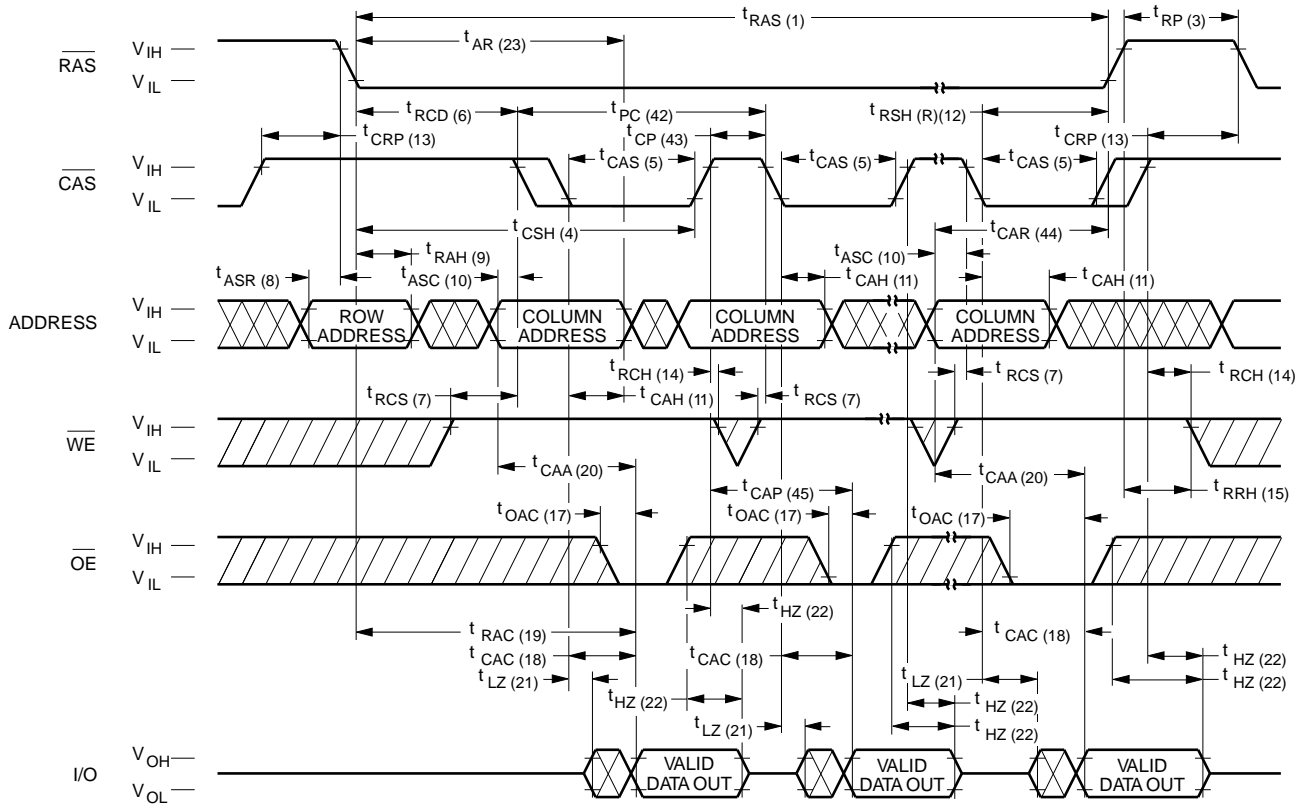
676 03

Waveforms of Read-Modify-Write Cycle



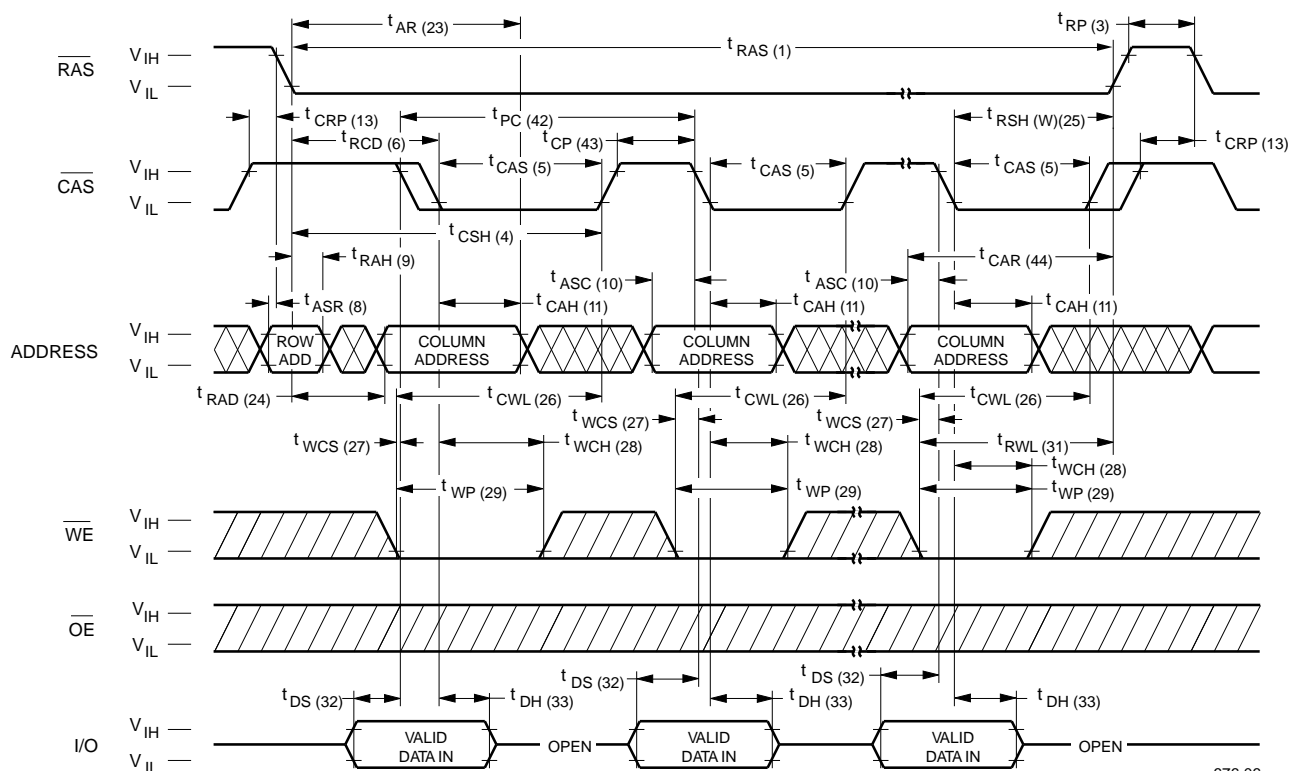
675 04

Waveforms of Fast Page Mode Read Cycle



676 05

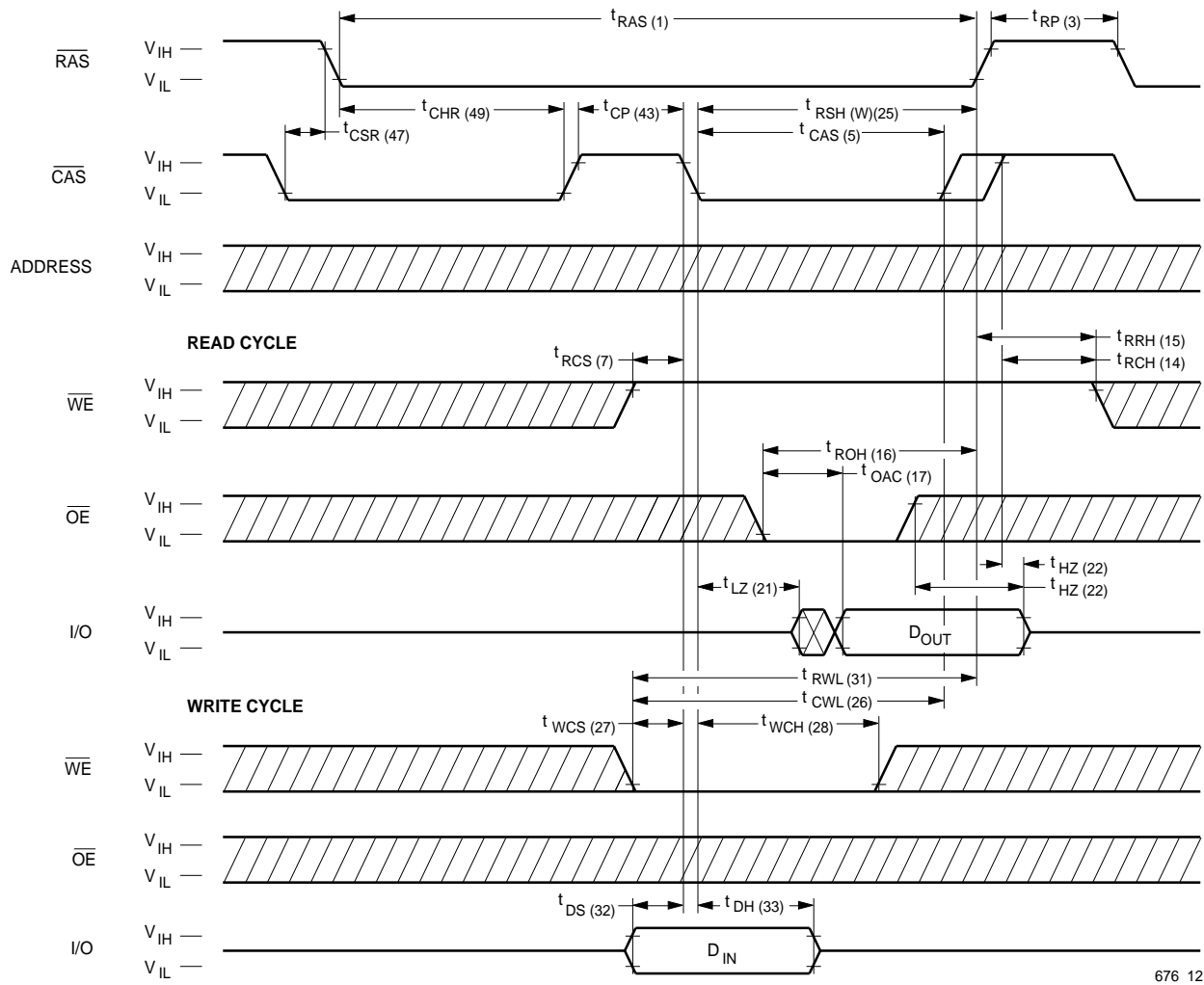
Waveforms of Fast Page Mode Write Cycle



676 06

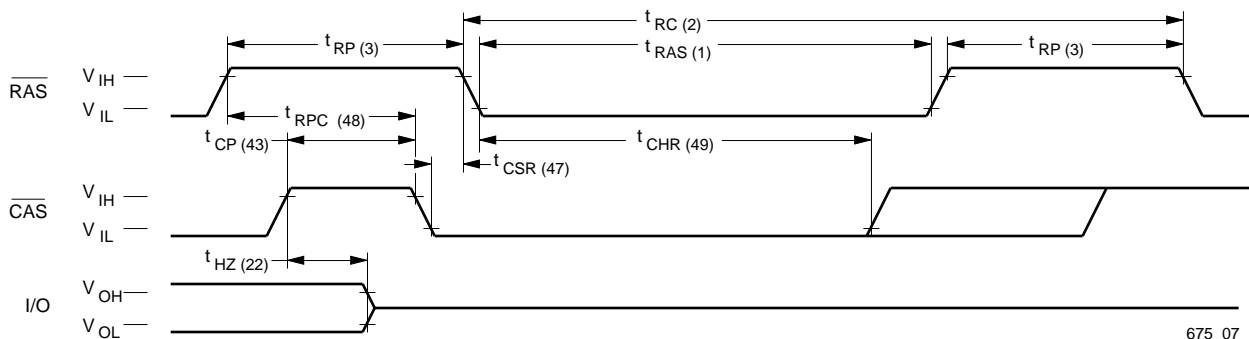


Waveforms of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Counter Test Cycle



676 12

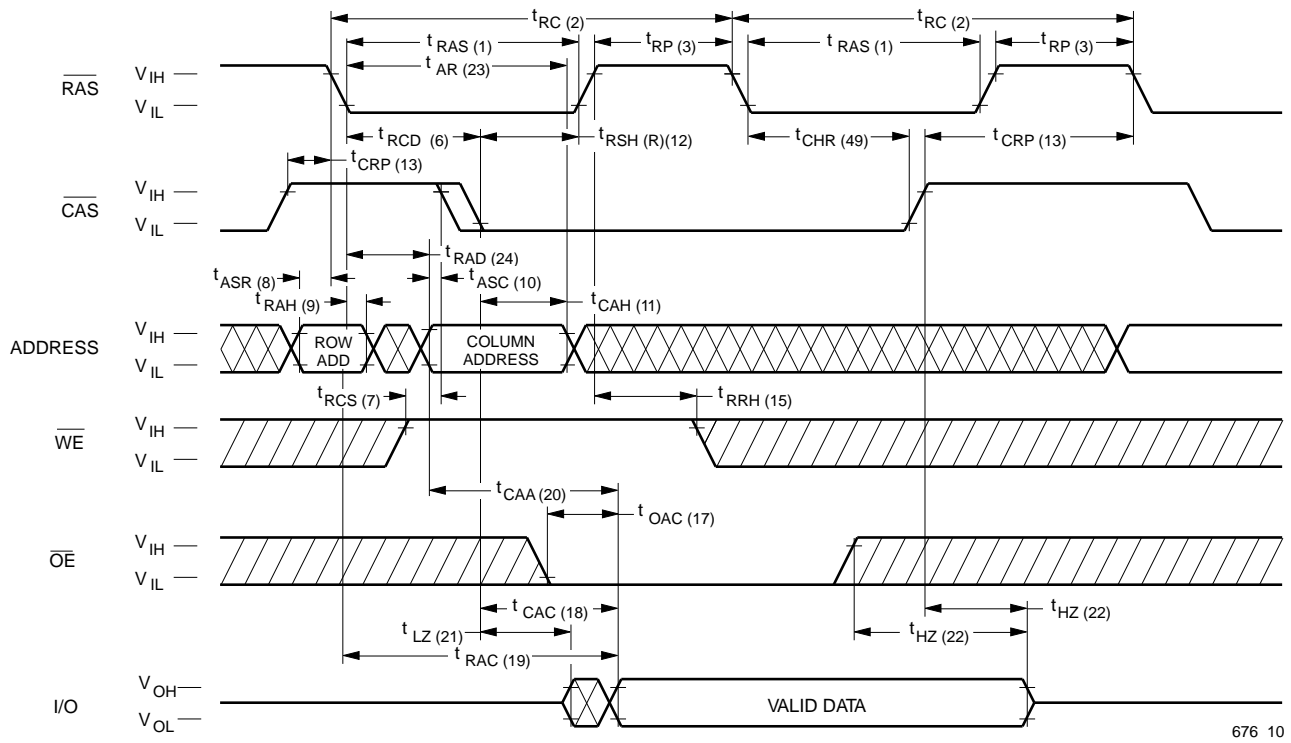
Waveforms of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Cycle



675 07

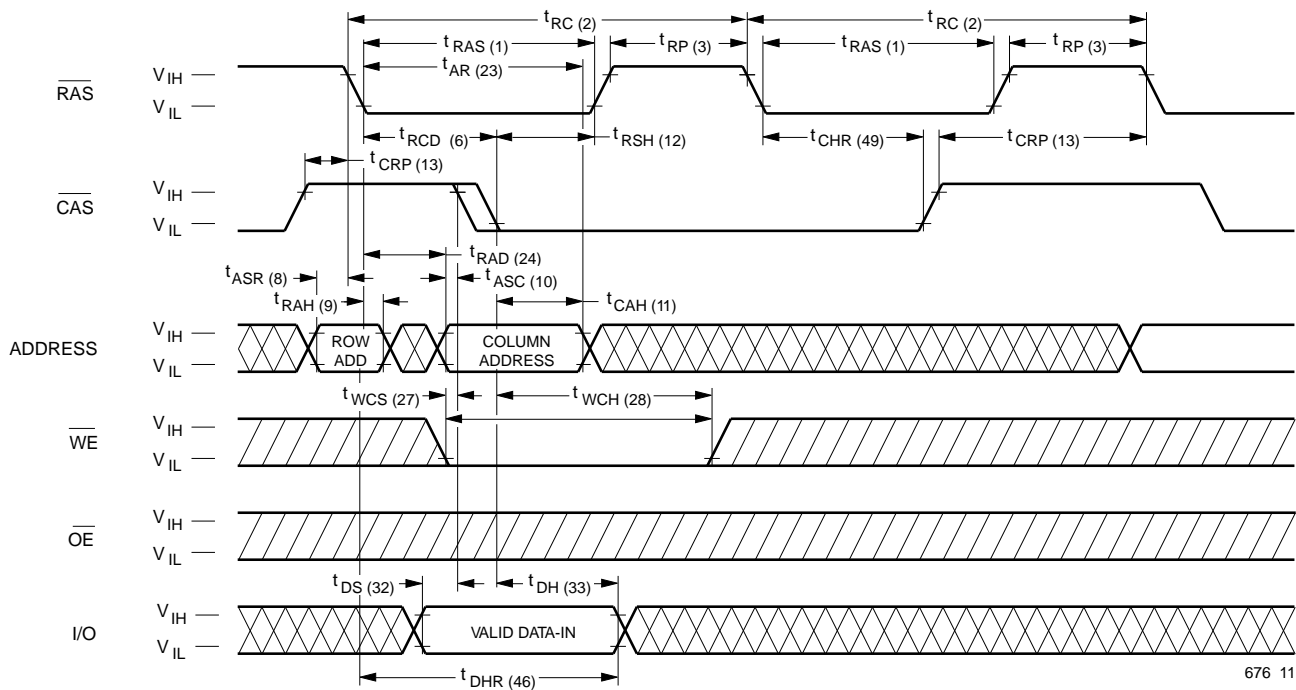
NOTE:  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $A_0$ - $A_7$  = Don't care

Waveforms of Hidden Refresh Cycle (Read)



676 10

Waveforms of Hidden Refresh Cycle (Write)



676 11

### Functional Description

The V53C8126H is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C8126H reads and writes data by multiplexing an 17-bit address into a 9-bit row and an 8-bit column address. The row address is latched by the Row Address Strobe ( $\overline{\text{RAS}}$ ). The column address “flows through” an internal address buffer and is latched by the Column Address Strobe ( $\overline{\text{CAS}}$ ). Because access time is primarily dependent on a valid column address rather than the precise time that the  $\overline{\text{CAS}}$  edge occurs, the delay time from  $\overline{\text{RAS}}$  to  $\overline{\text{CAS}}$  has little effect on the access time.

### Memory Cycle

A memory cycle is initiated by bringing  $\overline{\text{RAS}}$  low. Any memory cycle, once initiated, must not be ended or aborted before the minimum  $t_{\text{RAS}}$  time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time  $t_{\text{RP}}/t_{\text{CP}}$  has elapsed.

### Read Cycle

A Read cycle is performed by holding the Write Enable ( $\overline{\text{WE}}$ ) signal High during a  $\overline{\text{RAS}}/\overline{\text{CAS}}$  operation. The column address must be held for a minimum specified by  $t_{\text{AR}}$ . Data Out becomes valid only when  $t_{\text{OAC}}$ ,  $t_{\text{RAC}}$ ,  $t_{\text{CAA}}$  and  $t_{\text{CAC}}$  are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by  $t_{\text{CAA}}$  when  $t_{\text{RAC}}$ ,  $t_{\text{CAC}}$  and  $t_{\text{OAC}}$  are all satisfied.

### Write Cycle

A Write Cycle is performed by taking  $\overline{\text{WE}}$  and  $\overline{\text{CAS}}$  low during a  $\overline{\text{RAS}}$  operation. The column address is latched by  $\overline{\text{CAS}}$ . The Write Cycle can be  $\overline{\text{WE}}$  controlled or  $\overline{\text{CAS}}$  controlled depending on whether  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$  falls later. Consequently, the input data must be valid at or before the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. In the  $\overline{\text{CAS}}$ -controlled Write Cycle, when the leading edge of  $\overline{\text{WE}}$  occurs prior to the  $\overline{\text{CAS}}$  low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$  will maintain the output in the High-Z state.

In the  $\overline{\text{WE}}$  controlled Write Cycle,  $\overline{\text{OE}}$  must be in the high state and  $t_{\text{OED}}$  must be satisfied.

### Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses ( $A_0$  through  $A_8$ ) with  $\overline{\text{RAS}}$  at least once every 8 ms. Any Read, Write, Read-Modify-Write or  $\overline{\text{RAS}}$ -only cycle refreshes the addressed row.
2. Using a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Cycle. If  $\overline{\text{CAS}}$  makes a transition from low to high to low after the previous cycle and before  $\overline{\text{RAS}}$  falls,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is activated. The V53C8126H uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  is a “refresh-only” mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  counter test mode is provided to ensure reliable operation of the internal refresh counter.

### Fast Page Mode Operation

Fast Page Mode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining  $\overline{\text{RAS}}$  low while performing successive  $\overline{\text{CAS}}$  cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while  $\overline{\text{CAS}}$  is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of  $\overline{\text{CAS}}$ , eliminating  $t_{\text{ASC}}$  and  $t_{\text{T}}$  from the critical timing path.  $\overline{\text{CAS}}$  latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is  $t_{\text{CAA}}$  or  $t_{\text{CAP}}$  controlled. If the column address is valid prior to the rising edge of  $\overline{\text{CAS}}$ , the access time is referenced to the  $\overline{\text{CAS}}$  rising edge and is specified by  $t_{\text{CAP}}$ . If the column address is valid after the rising  $\overline{\text{CAS}}$  edge, access is timed from the occurrence of a valid address and is specified by  $t_{\text{CAA}}$ . In both cases, the falling edge of  $\overline{\text{CAS}}$  latches the address and enables the output.

Fast Page Mode provides sustained data rates up to 40 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{256}{t_{\text{RC}} + 255 \times t_{\text{PC}}}$$

### Data Output Operation

The V53C8126H Input/Output is controlled by  $\overline{\text{OE}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  and  $\overline{\text{RAS}}$ . A  $\overline{\text{RAS}}$  low transition enables the transfer of data to and from the selected row address in the Memory Array. A  $\overline{\text{RAS}}$  high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a  $\overline{\text{RAS}}$  low transition, a  $\overline{\text{CAS}}$  low transition or  $\overline{\text{CAS}}$  low level enables the internal I/O path. A  $\overline{\text{CAS}}$  high transition or a  $\overline{\text{CAS}}$  high level disables the I/O path and the output driver if it is enabled. A  $\overline{\text{CAS}}$  low transition while  $\overline{\text{RAS}}$  is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding  $\overline{\text{OE}}$  high. The

$\overline{\text{OE}}$  signal has no effect on any data stored in the output latches. A  $\overline{\text{WE}}$  low level can also disable the output drivers when  $\overline{\text{CAS}}$  is low. During a Write cycle, if  $\overline{\text{WE}}$  goes low at a time in relationship to  $\overline{\text{CAS}}$  that would normally cause the outputs to be active, it is necessary to use  $\overline{\text{OE}}$  to disable the output drivers prior to the  $\overline{\text{WE}}$  low transition to allow Data In Setup Time ( $t_{\text{DS}}$ ) to be satisfied.

### Power-On

After application of the  $V_{\text{CC}}$  supply, an initial pause of 200  $\mu\text{s}$  is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a  $\overline{\text{RAS}}$  clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the  $V_{\text{CC}}$  current requirement of the V53C8126H is dependent on the input levels of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . If  $\overline{\text{RAS}}$  is low during Power-On, the device will go into an active cycle and  $I_{\text{DD}}$  will exhibit current transients. It is recommended that  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  track with  $V_{\text{CC}}$  or be held at a valid  $V_{\text{IH}}$  during Power-On to avoid current surges.

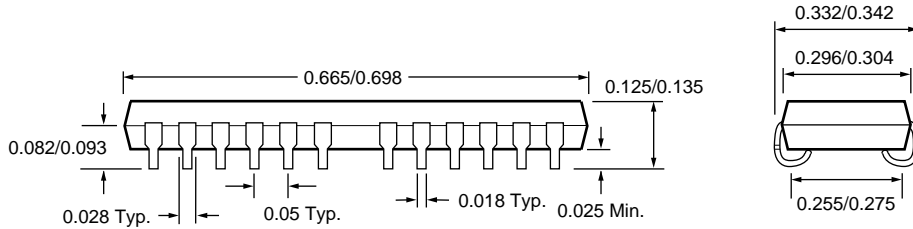
**Table 1. V53C8126H Data Output Operation for Various Cycle Types**

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{\text{CAS}}$ -Controlled Write Cycle (Early Write)	High-Z
$\overline{\text{WE}}$ -Controlled Write Cycle (Late Write)	$\overline{\text{OE}}$ Controlled. High $\overline{\text{OE}} = \text{High-Z I/Os}$
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{\text{RAS}}$ -only Refresh	High-Z
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle	Data remains as in previous cycle
$\overline{\text{CAS}}$ -only Cycles	High-Z

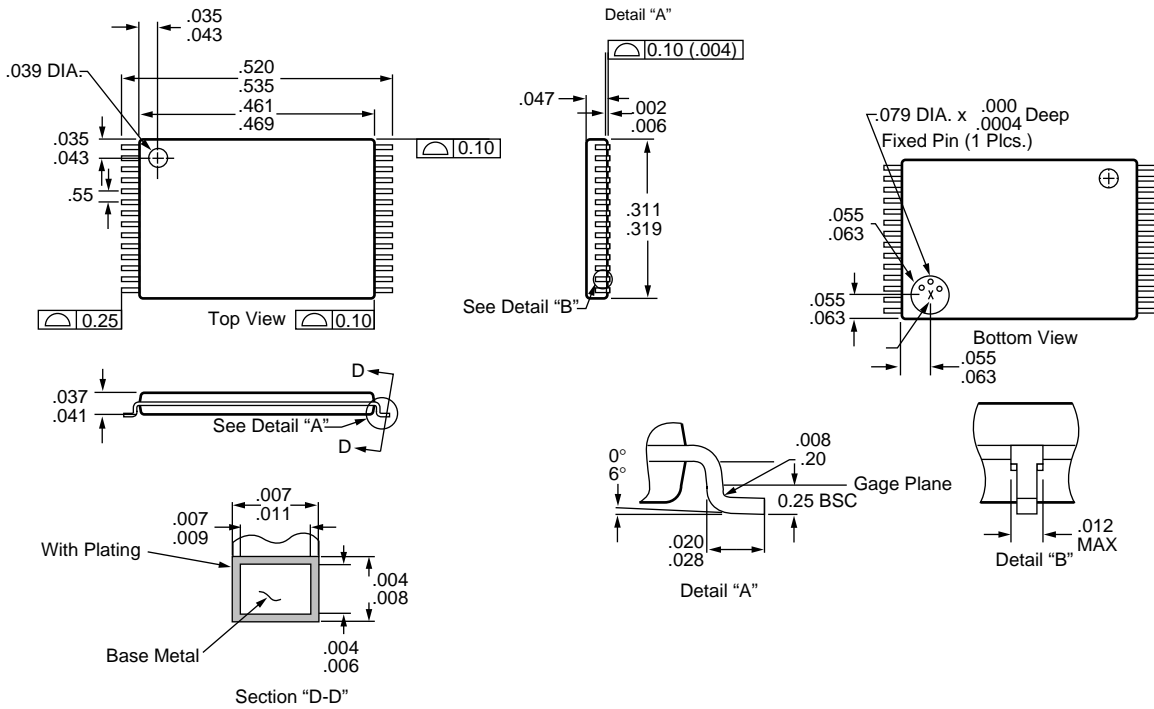


**Package Diagrams**

**26/24-pin 300 mil SOJ**



**28-pin TSOP-I**



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