

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)**  
 $< 0.8 \text{ V}$  at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)**  
 $> 2 \text{ V}$  at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200 \text{ pF}$ ,  $R = 0$ )**
- **Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Packages, Chip Carriers (FK), and DIPs (J)**

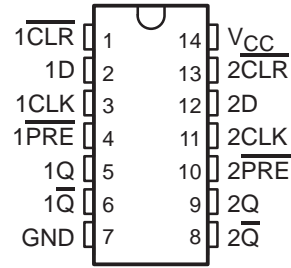
### description

These dual positive-edge-triggered D-type flip-flops are designed for 2-V to 5.5-V  $V_{CC}$  operation.

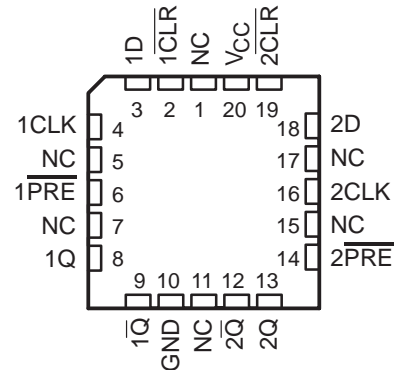
A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) inputs sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The SN54LV74A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LV74A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54LV74A ... J OR W PACKAGE  
 SN74LV74A ... D, DB, DGV, NS, OR PW PACKAGE  
 (TOP VIEW)



SN54LV74A ... FK PACKAGE  
 (TOP VIEW)



NC – No internal connection



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# SN54LV74A, SN74LV74A

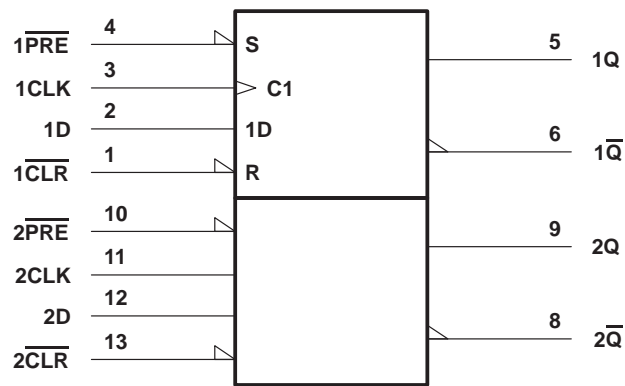
## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

SCLS381D – AUGUST 1997 – REVISED JUNE 1998

FUNCTION TABLE					
INPUTS				OUTPUTS	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>†</sup>	H <sup>†</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\overline{\text{Q}}_0$

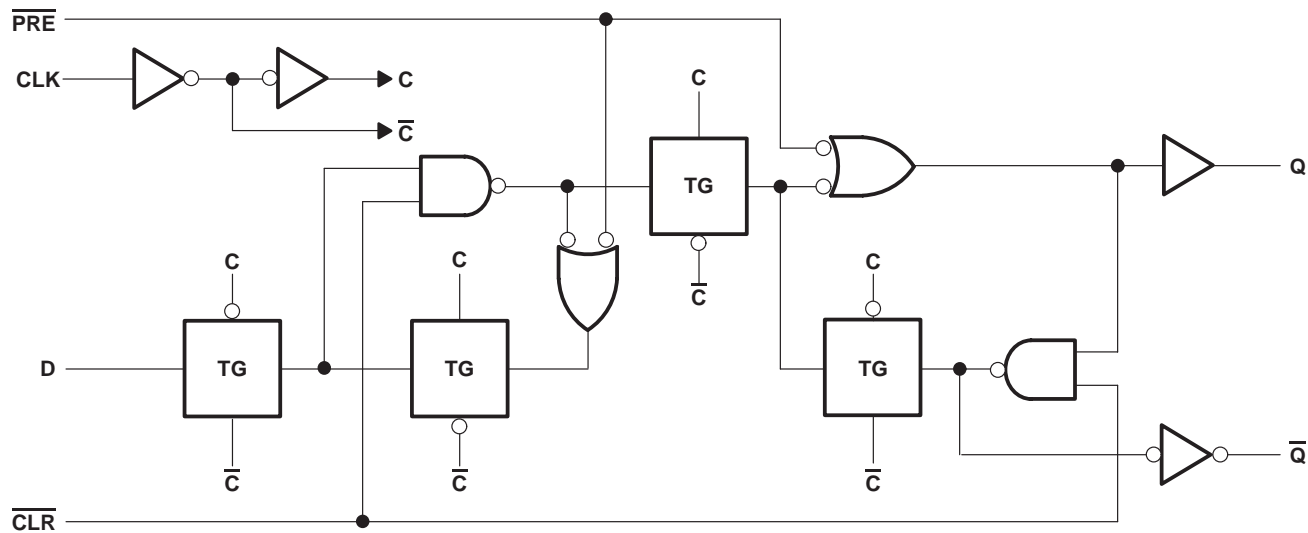
<sup>†</sup> This configuration is unstable; that is, it does not persist when  $\overline{\text{PRE}}$  or  $\overline{\text{CLR}}$  returns to its inactive (high) level.

### logic symbol<sup>‡</sup>



<sup>‡</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, DGV, J, NS, PW, and W packages.

### logic diagram, each flip-flop (positive logic)



# SN54LV74A, SN74LV74A

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	127°C/W
DB package	158°C/W
DGV package	182°C/W
NS package	127°C/W
PW package	170°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. This value is limited to 7 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51.

### recommended operating conditions (see Note 4)

			SN54LV74A		SN74LV74A		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage		2	5.5	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
$V_I$	Input voltage		0	5.5	0	5.5	V
$V_O$	Output voltage		0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V		–50		–50	μA
		$V_{CC} = 2.3$ V to 2.7 V		–2		–2	
		$V_{CC} = 3$ V to 3.6 V		–6		–6	
		$V_{CC} = 4.5$ V to 5.5 V		–12		–12	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V		50		50	μA
		$V_{CC} = 2.3$ V to 2.7 V		2		2	
		$V_{CC} = 3$ V to 3.6 V		6		6	
		$V_{CC} = 4.5$ V to 5.5 V		12		12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	0	200	0	200	ns/V
		$V_{CC} = 3$ V to 3.6 V	0	100	0	100	
		$V_{CC} = 4.5$ V to 5.5 V	0	20	0	20	
$T_A$	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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# SN54LV74A, SN74LV74A

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV74A			SN74LV74A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> -0.1			V <sub>CC</sub> -0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			2			
	I <sub>OH</sub> = -6 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = -12 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V	0.4			0.4			
	I <sub>OL</sub> = 6 mA	3 V	0.44			0.44			
	I <sub>OL</sub> = 12 mA	4.5 V	0.55			0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V	±1			±1			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	20			20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	5			5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	2.1			2.1			pF
		5 V	2.1			2.1			

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

PARAMETER			T <sub>A</sub> = 25°C		SN54LV74A		SN74LV74A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	PRE or CLR low	8		9		9		ns
		CLK	8		9		9		
t <sub>su</sub>	Setup time before CLK↑	Data	8		9		9		ns
		PRE or CLR inactive	7		7		7		
t <sub>h</sub>	Hold time, data after CLK↑		0.5		0.5		0.5		ns

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER			T <sub>A</sub> = 25°C		SN54LV74A		SN74LV74A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	PRE or CLR low	6		7		7		ns
		CLK	6		7		7		
t <sub>su</sub>	Setup time before CLK↑	Data	6		7		7		ns
		PRE or CLR inactive	5		5		5		
t <sub>h</sub>	Hold time, data after CLK↑		0.5		0.5		0.5		ns

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# SN54LV74A, SN74LV74A

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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**timing requirements over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER			$T_A = 25^\circ\text{C}$		SN54LV74A		SN74LV74A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_W$	Pulse duration	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	5		5		5		ns
		CLK	5		5		5		
$t_{su}$	Setup time before CLK $\uparrow$	Data	5		5		5		ns
		$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	3		3		3		
$t_h$	Hold time, data after CLK $\uparrow$		0.5		0.5		0.5		ns

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV74A		SN74LV74A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}^*$	50	100		40		40		MHz
			$C_L = 50\text{ pF}$	30	70		25		25		
$t_{pd}^*$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 15\text{ pF}$	9.8	14.8		1	17	1	17	ns
	CLK			11.1	16.4		1	19	1	19	
$t_{pd}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 50\text{ pF}$	13	17.4		1	20	1	20	ns
	CLK			14.2	20		1	23	1	23	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV74A		SN74LV74A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}^*$	80	140		70		70		MHz
			$C_L = 50\text{ pF}$	50	90		45		45		
$t_{pd}^*$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 15\text{ pF}$	6.9	12.3		1	14.5	1	14.5	ns
	CLK			7.9	11.9		1	14	1	14	
$t_{pd}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 50\text{ pF}$	9.2	15.8		1	18	1	18	ns
	CLK			10.2	15.4		1	17.5	1	17.5	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV74A		SN74LV74A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$f_{max}$			$C_L = 15\text{ pF}^*$	130	180		110		110		MHz
			$C_L = 50\text{ pF}$	90	140		75		75		
$t_{pd}^*$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 15\text{ pF}$	5	7.7		1	9	1	9	ns
	CLK			5.6	7.3		1	8.5	1	8.5	
$t_{pd}$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or $\overline{Q}$	$C_L = 50\text{ pF}$	6.6	9.7		1	11	1	11	ns
	CLK			7.2	9.3		1	10.5	1	10.5	

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# SN54LV74A, SN74LV74A

## DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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**noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)**

PARAMETER	SN74LV74A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.1	0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		−0.04	−0.8	V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		3.2		V
$V_{IH(D)}$ High-level dynamic input voltage	2.31			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

**operating characteristics,  $T_A = 25^\circ\text{C}$**

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	21	pF
		5 V	23	

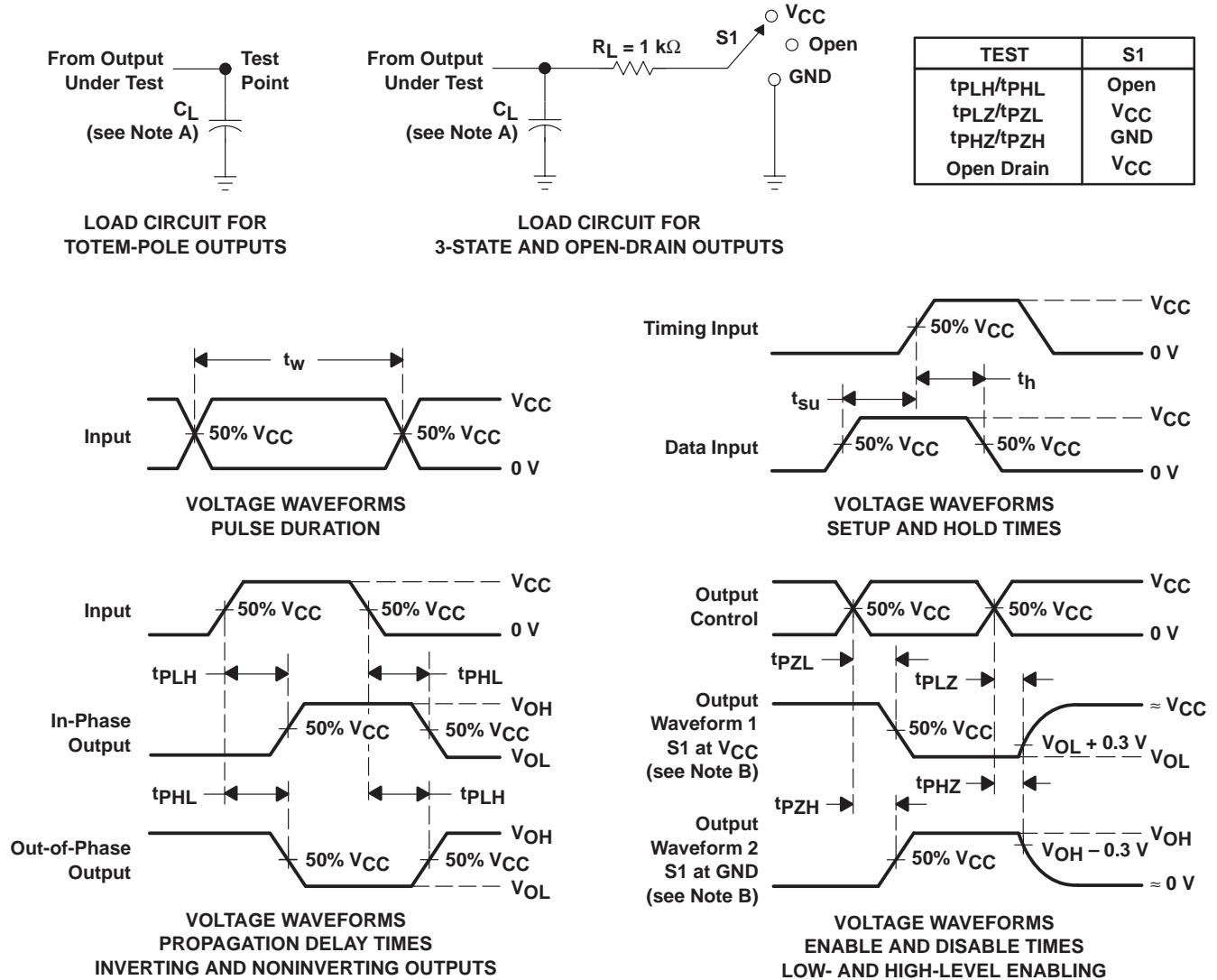


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# SN54LV74A, SN74LV74A DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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