PRELIMINARY‡

128Mb: x4, x8, x16
DDR333 SDRAM Addendum

DOUBLE DATA RATE (DDR) SDRAM

MT46V32M4 – 8 Meg x 4 x 4 banks
MT46V16M8 – 4 Meg x 8 x 4 banks
MT46V8M16 – 2 Meg x 16 x 4 banks

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/dramds

FEATURES

- 167 MHz Clock, 333 Mb/s/p data rate
- V_{DD} = +2.5V ±0.2V, $V_{DD}Q$ = +2.5V ±0.2V
- Bidirectional data strobe (DQS) transmitted/ received with data, i.e., source-synchronous data capture (x16 has two - one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two - one per byte)
- Programmable burst lengths: 2, 4, or 8
- Concurrent Auto Precharge option supported
- Auto Refresh and Self Refresh Modes
- FBGA package available
- 2.5V I/O (SSTL_2 compatible)
- ^{t}RAS lockout (^{t}RAP = ^{t}RCD)
- Backwards compatible with DDR200 and DDR266

OPTIONS — PART NUMBER

- Configuration
  - 32 Meg x 4 (8 Meg x 4 x 4 banks) — 32M4
  - 16 Meg x 8 (4 Meg x 8 x 4 banks) — 16M8
  - 8 Meg x 16 (2 Meg x 16 x 4 banks) — 8M16
- Plastic Package
  - 66-Pin TSOP (OCPL) — TG
  - 60-Ball FBGA (16x9mm) — FJ
- Timing - Cycle Time
  - 6ns @ CL = 2.5 (DDR333B–FBGA)[1] — -6
  - 6ns @ CL = 2.5 (DDR333B–TSOP)[1] — -6T
  - 7.5ns @ CL = 2 (DDR266A)[2] — -75Z
- Self Refresh
  - Standard — none

NOTE: 1. Supports PC2700 modules with 2.5-3-3 timing
2. Supports PC2100 modules with 2-3-3 timing

DDR333 COMPATIBILITY

DDR333 meets or surpasses all DDR266 timing requirements thus assuring full backwards compatibility with current DDR designs. In addition, these devices support concurrent auto-precharge and ^{t}RAS lockout for improved timing performance. The 128Mb, DDR333 device will support an (^{t}REFI) average periodic refresh interval of 15.6µs.

The standard 66-pin TSOP package is offered for point-to-point applications where the FBGA package is intended for the multi-drop systems.

The Micron 128Mb data sheet provides full specifications and functionality unless specified herein.

CONFIGURATION

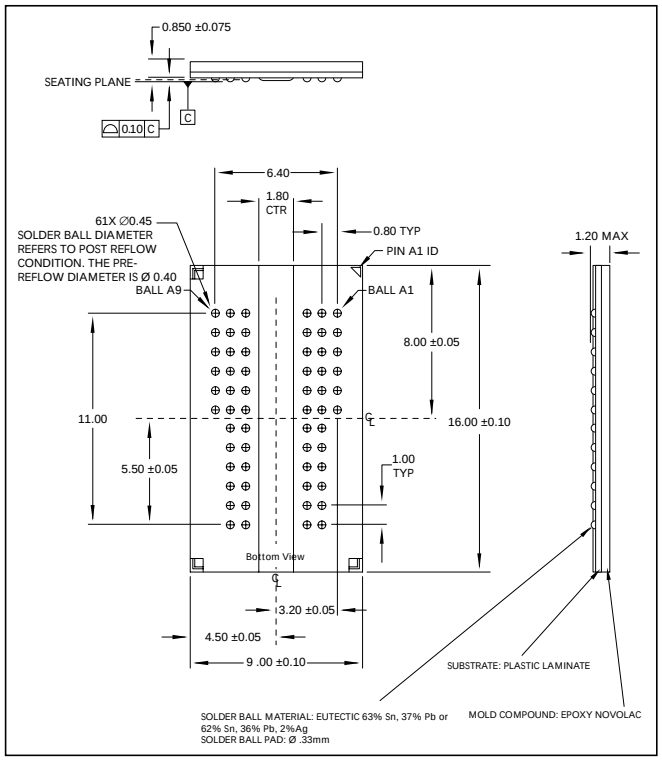
Architecture	32 Meg x 4	16 Meg x 8	8 Meg x 16
Configuration	8 Meg x 4 x 4 banks	4 Meg x 8 x 4 banks	2 Meg x 16 x 4 banks
Refresh Count	4K	4K	4K
Row Addressing	4K (A0–A11)	4K (A0–A11)	4K (A0–A11)
Bank Addressing	4 (BA0, BA1)	4 (BA0, BA1)	4 (BA0, BA1)
Column Addressing	2K (A0–A9, A11)	1K (A0–A9)	512 (A0– A8)

KEY TIMING PARAMETERS[3]

SPEED GRADE	CLOCK RATE		DATA-OUT WINDOW[2]	ACCESS WINDOW	DQS-DQ SKEW
	CL = 2[1]	CL = 2.5[1]			
-6	133 MHz	167 MHz	2.15ns	±0.70ns	+0.35ns
-6T	133 MHz	167 MHz	2.0ns	±0.75ns	+0.45ns
-75Z	133 MHz	133 MHz	2.5ns	±0.75ns	+0.50ns

NOTE: 1. CL = CAS (Read) Latency
2. With a 50/50 clock duty cycle and a minimum clock rate @ CL = 2 (-75Z) and CL = 2.5 (-6, -6T).
3. Slower speeds are included in the 128Mb base data sheet (-75, -8).

FBGA 60-BALL PACKAGE DIMENSION



FBGA PACKAGE MARKING

Due to the physical size of the FBGA package, the full ordering part number is not printed on the package. Instead the following package code is utilized.

Top mark contains five fields 12345

- Field 1 (Product Family)
  - DRAM D
  - DRAM - ES Z
- Field 2 (Product Type)
  - 2.5 Volt, DDR SDRAM, 60-ball L
- Field 3 (Width)
  - x4 devices B
  - x8 devices C
  - x16 devices D
- Field 4 (Density / Size)
  - 128Mb F
- Filed 5 (Speed Grade)
  - -6 J
  - -75Z P
  - -75 F
  - -8 C

Example top mark for a MT46V32M4FJ-6: DLBFJ

FBGA PACKAGE PINOUT

x4 (Top View)

	1	2	3	4	5	6	7	8	9
A	VSSQ	NC	VSS				VDD	NC	VDDQ
B	NC	VDDQ	DQ3				DQ0	VSSQ	NC
C	NC	VSSQ	NC				NC	VDDQ	NC
D	NC	VDDQ	DQ2				DQ1	VSSQ	NC
E	NC	VSSQ	DQS				NC	VDDQ	NC
F	VREF	VSS	DM				NC	VDD	A13
G		CK	CK#				WE#	CAS#	
H		A12	CKE				RAS#	CS#	
J		A11	A9				BA1	BA0	
K		A8	A7				A0	A10	
L		A6	A5				A2	A1	
M		A4	VSS				VDD	A3	

x8 (Top View)

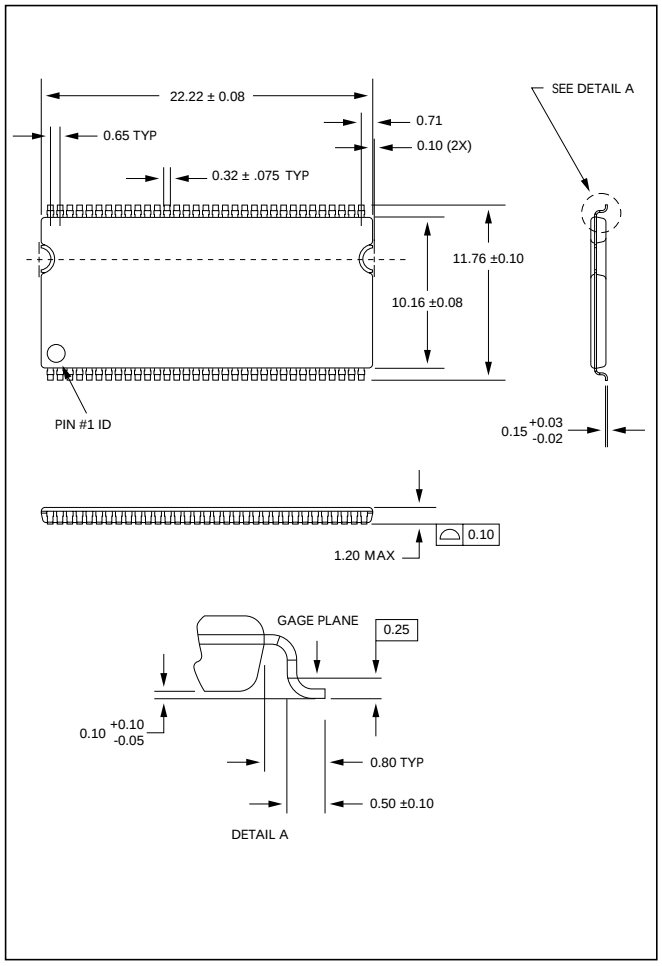
	1	2	3	4	5	6	7	8	9
A	VSSQ	DQ7	VSS				VDD	DQ0	VDDQ
B	NC	VDDQ	DQ6				DQ1	VSSQ	NC
C	NC	VSSQ	DQ5				DQ2	VDDQ	NC
D	NC	VDDQ	DQ4				DQ3	VSSQ	NC
E	NC	VSSQ	DQS				NC	VDDQ	NC
F	VREF	VSS	DM				NC	VDD	A13
G		CK	CK#				WE#	CAS#	
H		A12	CKE				RAS#	CS#	
J		A11	A9				BA1	BA0	
K		A8	A7				A0	A10	
L		A6	A5				A2	A1	
M		A4	VSS				VDD	A3	

x16 (Top View)

	1	2	3	4	5	6	7	8	9
A	VSSQ	DQ15	VSS				VDD	DQ0	VDDQ
B	DQ14	VDDQ	DQ13				DQ2	VSSQ	DQ1
C	DQ12	VSSQ	DQ11				DQ4	VDDQ	DQ3
D	DQ10	VDDQ	DQ9				DQ6	VSSQ	DQ5
E	DQ8	VSSQ	UDQS				LDQS	VDDQ	DQ7
F	VREF	VSS	UDM				LDM	VDD	A13
G		CK	CK#				WE#	CAS#	
H		A12	CKE				RAS#	CS#	
J		A11	A9				BA1	BA0	
K		A8	A7				A0	A10	
L		A6	A5				A2	A1	
M		A4	VSS				VDD	A3	

‡ THIS DATA SHEET CONTAINS THE PRESENT DESCRIPTION OF A PRODUCT IN DEFINITION WITH NO FORMAL DESIGN IN PROGRESS.

66-PIN TSOP PACKAGE DIMENSION



66-PIN TSOP PACKAGE PIN ASSIGMENT

(TOP VIEW)

x4	x8	x16			x16	x8	x4
VDD	VDD	VDD	1 •	66	VSS	VSS	VSS
NC	DQ0	DQ0	2	65	DQ15	DQ7	NC
VDDQ	VDDQ	VDDQ	3	64	VSSQ	VSSQ	VSSQ
NC	NC	DQ1	4	63	DQ14	NC	NC
DQ0	DQ1	DQ2	5	62	DQ13	DQ6	DQ3
VSSQ	VSSQ	VSSQ	6	61	VDDQ	VDDQ	VDDQ
NC	NC	DQ3	7	60	DQ12	NC	NC
NC	DQ2	DQ4	8	59	DQ11	DQ5	NC
VDDQ	VDDQ	VDDQ	9	58	VSSQ	VSSQ	VSSQ
NC	NC	DQ5	10	57	DQ10	NC	NC
DQ1	DQ3	DQ6	11	56	DQ9	DQ4	DQ2
VSSQ	VSSQ	VSSQ	12	55	VDDQ	VDDQ	VDDQ
NC	NC	DQ7	13	54	DQ8	NC	NC
NC	NC	NC	14	53	NC	NC	NC
VDDQ	VDDQ	VDDQ	15	52	VSSQ	VSSQ	VSSQ
NC	NC	LDQS	16	51	UDQS	DQS	DQS
NC	NC	NC	17	50	DNU	DNU	DNU
VDD	VDD	VDD	18	49	VREF	VREF	VREF
DNU	DNU	DNU	19	48	VSS	VSS	VSS
NC	NC	LDM	20	47	UDM	DM	DM
WE#	WE#	WE#	21	46	CK#	CK#	CK#
CAS#	CAS#	CAS#	22	45	CK	CK	CK
RAS#	RAS#	RAS#	23	44	CKE	CKE	CKE
CS#	CS#	CS#	24	43	NC	NC	NC
NC	NC	NC	25	42	A12	A12	A12
BA0	BA0	BA0	26	41	A11	A11	A11
BA1	BA1	BA1	27	40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28	39	A8	A8	A8
A0	A0	A0	29	38	A7	A7	A7
A1	A1	A1	30	37	A6	A6	A6
A2	A2	A2	31	36	A5	A5	A5
A3	A3	A3	32	35	A4	A4	A4
VDD	VDD	VDD	33	34	VSS	VSS	VSS

NOTE: 1. All dimensions in millimeters.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

PIN DESCRIPTIONS

BALL / PIN NUMBERS				
FBGA	TSOP	SYMBOL	TYPE	DESCRIPTION
G2, G3	45, 46	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS) is referenced to the crossings of CK and CK#.
H3	44	CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied.
H8	24	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
H7, G8, G7	23, 22, 21	RAS#,CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
3F F7, 3F	47 20, 47	DM LDM, UDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. For the x16 , LDM is DM for DQ0-DQ7 and UDM is DM for DQ8-DQ15. Pin 20 is a NC on x4 and x8
J8,J7	26, 27	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
K7, L8, L7 M8, M2, L3 L2, K3, K2 J3, K8, J2	29-32 32, 35, 36 36, 38, 39 40, 29, 41	A0, A1, A2 A3, A4, A5 A6, A7, A8 A9, A10, A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.

(continued on next page)

PIN DESCRIPTIONS (continued)

BALL / PIN NUMBERS				
FBGA	**TSOP**	**SYMBOL**	**TYPE**	**DESCRIPTION**
A8, B9, B7 C9, C7, D9 D7, E9, E1 D3, D1, C3 C1, B3, B1, A2	2, 4, 5, 7, 8, 10 11, 13, 54 56, 57, 59 60, 62, 63, 65	DQ0-2 DQ3-5 DQ6-8 DQ9-11 DQ12-14 DQ15	I/O	Data Input/Output: Data bus for **x16**
A8, B7, C7, D7, D3, C3, B3, A2	2, 5, 8, 11, 56, 59 62, 65	DQ0-2 DQ3-5 DQ6-7	I/O	Data Input/Output: Data bus for **x8**
B7, D7, D3, B3	5, 11, 56 62	DQ0-2 DQ2	I/O	Data Input/Output: Data bus for **x4**
E3 E7, E3	51 16, 51	DQS LDQS, UDQS	I/O	Data Strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data. For the x16 , LDQS is DQS for DQ0-DQ7 and UDQS IS DQS for DQ8-DQ15. Pin 16 (H7) is NC on x4 and x8.
	14, 17, 25, 43, 53	NC	-	No Connect: These pins should be left unconnected.
	19, 50	DNU	–	Do Not Use: Must float to minimize noise on Vref
B2, D2, C8, E8, A9	3, 9, 15, 55, 61	$V_{DD}Q$	Supply	DQ Power Supply: +2.5V ±0.2V. Isolated on the die for improved noise immunity.
A1, E2, B8, D8	6, 12, 52, 58, 64	$V_{SS}Q$	Supply	DQ Ground. Isolated on the die for improved noise immunity.
F8, M7, A7	1, 18, 33	V_{DD}	Supply	Power Supply: +2.5V ±0.2V.
A1, A3, F2, M3	34, 48, 66	V_{SS}	Supply	Ground.
F1	49	V_{REF}	Supply	SSTL_2 reference voltage.
F9	17	A13	I	Address input A13 for 1Gb devices.
H2	42	A12	I	For 256Mb and greater devices.

GENERAL DESCRIPTION

The DDR333 SDRAM is a high-speed CMOS, dynamic random-access memory that operates at a frequency of 167 MHz (^{t}CK=6ns) with a peak data transfer rate of 333Mb/s/p. DDR333 continues to use the JEDEC standard SSTL_2 interface and the *2n*-prefetch architecture.

The standard DDR200/DDR266 data sheets also pertain to the DDR333 device and should be referenced for a complete description of DDR SDRAM functionality and operating modes. However, to meet the faster DDR333 operating frequencies, some of the AC timing parameters are slightly tighter. This addendum data sheet will concentrate on the key differences required to support the enhanced speeds.

In addition to the standard 66-pin TSOP package, a 60-ball FBGA package is utilized for DDR333. This JEDEC-defined package promotes better package parasitic parameters and a smaller footprint.

CAPACITANCE (FBGA)

(Notes: 1-5, 14-17, 33; notes appear in DDR200/266 data sheets)
(0°C ≤ T_A ≤ 70°C; $V_{DD}Q$ = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance:					
DQs, DQS, DM (for x4 or x8 devices)	DC_{IO}	–	0.50	pF	13, 24
DQ0-DQ7, LDQS, LDM (for lower byte of x16 devices),	DC_{IO}	–	0.50	pF	13, 24
DQ8-DQ15, UDQS, UDM (for upper byte of x16 devices)	DC_{IO}	–	0.50	pF	13, 29
Delta Input Capacitance: Command and Address	DC_{I1}	–	0.50	pF	13, 29
Delta Input Capacitance: CK, CK#	DC_{I2}	–	0.25	pF	13, 29
Input/Output Capacitance: DQs, DQS, DM (LDQS, LDM, UDM)	C_{IO}	3.50	4.00	pF	13
Input Capacitance: Command and Address	C_{I1}	1.50	2.50	pF	13
Input Capacitance: CK, CK#	C_{I2}	1.50	2.50	pF	13
Input Capacitance: CKE	C_{I3}	1.50	2.50	pF	13

CAPACITANCE (TSOP)

(Notes: 1-5, 14-17, 33; notes appear in DDR200/266 data sheets)
(0°C ≤ T_A ≤ 70°C; $V_{DD}Q$ = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Delta Input/Output Capacitance:					
DQs, DQS, DM (for x4 or x8 devices)	DC_{IO}	–	0.50	pF	13, 24
DQ0-DQ7, LDQS, LDM (for lower byte of x16 devices),	DC_{IO}	–	0.50	pF	13, 24
DQ8-DQ15, UDQS, UDM (for upper byte of x16 devices)	DC_{IO}	–	0.50	pF	13, 24
Delta Input Capacitance: Command and Address	DC_{I1}	–	0.50	pF	13, 29
Delta Input Capacitance: CK, CK#	DC_{I2}	–	0.25	pF	13, 29
Input/Output Capacitance: DQs, DQS, DM (LDQS, LDM, UDM)	C_{IO}	4.0	5.0	pF	13
Input Capacitance: Command and Address	C_{I1}	2.0	3.0	pF	13
Input Capacitance: CK, CK#	C_{I2}	2.0	3.0	pF	13
Input Capacitance: CKE	C_{I3}	2.0	3.0	pF	13

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 1-5, 14-17, 33; notes appear in DDR200/266 data sheets)
(0°C ≤ T_A ≤ 70°C; $V_{DD}Q$ = +2.5V ±0.2V, V_{DD} = +2.5V ±0.2V)

AC CHARACTERISTICS			-6 (FBGA)		-6T (TSOP)		-75Z			
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access window of DQs from CK/CK#		^tAC	-0.7	+0.7	-0.7	+0.7	-0.75	+0.75	ns	
CK high-level width		^tCH	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	30
CK low-level width		^tCL	0.45	0.55	0.45	0.55	0.45	0.55	^tCK	30
Clock cycle time	CL = 2.5	^tCK (2.5)	6	13	6	13	7.5	13	ns	45,52
	CL = 2	^tCK (2)	7.5	13	7.5	13	7.5	13	ns	45,52
DQ and DM input hold time relative to DQS		^tDH	0.45		0.45		0.50		ns	26,31
DQ and DM input setup time relative to DQS		^tDS	0.45		0.45		0.50		ns	26,31
DQ and DM input pulse width (for each input)		^tDIPW	1.75		1.75		1.75		ns	31
Access window of DQS from CK/CK#		^tDQSCK	-0.60	+0.60	-0.60	+0.60	-0.75	+0.75	ns	
DQS input high pulse width		^tDQSH	0.35		0.35		0.35		^tCK	
DQS input low pulse width		^tDQSL	0.35		0.35		0.35		^tCK	
DQS-DQ skew, DQS to last DQ valid, per group, per access		^tDQSQ		0.35		0.45		0.50	ns	25, 26
Write command to first DQS latching transition		^tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	^tCK	
DQS falling edge to CK rising - setup time		^tDSS	0.2		0.2		0.2		^tCK	
DQS falling edge from CK rising - hold time		^tDSH	0.2		0.2		0.2		^tCK	
Half clock period		^tHP	^tCH,^tCL		^tCH,^tCL		^tCH,^tCL		ns	34
Data-out high-impedance window from CK/CK#		^tHZ		+0.70		+0.70		+0.75	ns	18,42
Data-out low-impedance window from CK/CK#		^tLZ	-0.70		-0.70		-0.75		ns	18,43
Address and control input hold time (fast slew rate)		^tIH_F	0.75		0.75		0.90		ns	14
Address and control input setup time (fast slew rate)		^tIS_F	0.75		0.75		0.90		ns	14
Address and control input hold time (slow slew rate)		^tIH_S	0.80		0.80		1		ns	14
Address and control input setup time (slow slew rate)		^tIS_S	0.80		0.80		1		ns	14
Address and control input pulse width		^tIPW	2.2		2.2		2.2		ns	
LOAD MODE REGISTER command cycle time		^tMRD	12		12		15		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access		^tQH	^tHP - ^tQHS		^tHP - ^tQHS		^tHP - ^tQHS		ns	25, 26
Data Hold Skew Factor		^tQHS		0.50		0.60		0.75	ns	
ACTIVE to AUTOPRECHARGE command		^tRAP	18		18		20		ns	46
ACTIVE to PRECHARGE command		^tRAS	42	70,000	42	70,000	40	120,000	ns	35
ACTIVE to ACTIVE/AUTO REFRESH command period		^tRC	60		60		65		ns	
AUTO REFRESH command period		^tRFC	72		72		75		ns	50
ACTIVE to READ or WRITE delay		^tRCD	18		18		20		ns	
PRECHARGE command period		^tRP	18		18		20		ns	
DQS read preamble		^tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	^tCK	42
DQS read postamble		^tRPST	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	12		12		15		ns	
DQS write preamble		^tWPRE	0.25		0.25		0.25		^tCK	
DQS write preamble setup time		^tWPRES	0		0		0		ns	20, 21
DQS write postamble		^tWPST	0.4	0.6	0.4	0.6	0.4	0.6	^tCK	19
Write recovery time		^tWR	15		15		15		ns	
Internal WRITE to READ command delay		^tWTR	1		1		1		^tCK	
Data valid output window		na	^tQH - ^tDQSQ		^tQH - ^tDQSQ		^tQH - ^tDQSQ		ns	25
REFRESH to REFRESH command interval		^tREFC		140.6		140.6		140.6	µs	23
Average periodic refresh interval		^tREFI		15.6		15.6		15.6	µs	23
Terminating voltage delay to V_{DD}		^tVTD	0		0		0		ns	
Exit SELF REFRESH to non-READ command		^tXSNR	75		75		75		ns	
Exit SELF REFRESH to READ command		^tXSRD	200		200		200		^tCK	

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‡ THIS DATA SHEET CONTAINS THE PRESENT DESCRIPTION OF A PRODUCT IN DEFINITION WITH NO FORMAL DESIGN IN PROGRESS.