SC2677

Dual Synchronous Voltage Mode Controller with Current Sharing Circuitry

POWER MANAGEMENT

Description

The SC2677 is a versatile 2 phase, synchronous, voltage mode PWM controller that may be used in two distinct ways. First, the SC2677 is ideal for applications where point of use output power exceeds any single input power budget. Alternatively, the SC2677 can be used as a dual switcher. The SC2677 features a temperature compensated voltage reference, an under voltage lockout over current protection and internal level-shifted, high-side drive circuitry.

In current sharing configuration, the SC2677 can produce a single output voltage from two separate voltage sources (which can be different voltage levels) while maintaining current sharing between the channels. Current sharing is programmable to allow loading each input supply as required by the application.

In dual switcher configuration, two feedback paths are provided for independent control of the separate outputs. The device will provide a regulated output from flexibly configured inputs (3.3V, 5V, 12V), provided 5V is present for V_{CC}. The phasing between the two switchers is adjustable to minimize the input and output ripple.

Features

- 300kHz to 1MHz externally programmable frequency operation
- Soft Start and Enable function
- Power Good output provided
- Under voltage short circuit protection
- Phase-shifted switchers minimize ripple
- High efficiency operation, >90%
- Programmable output(s) as low as 0.5V
- Industrial temperature range
- TSSOP-20 package
- Bias voltage as low as 4.5V
- Adjustable phase shift between channels

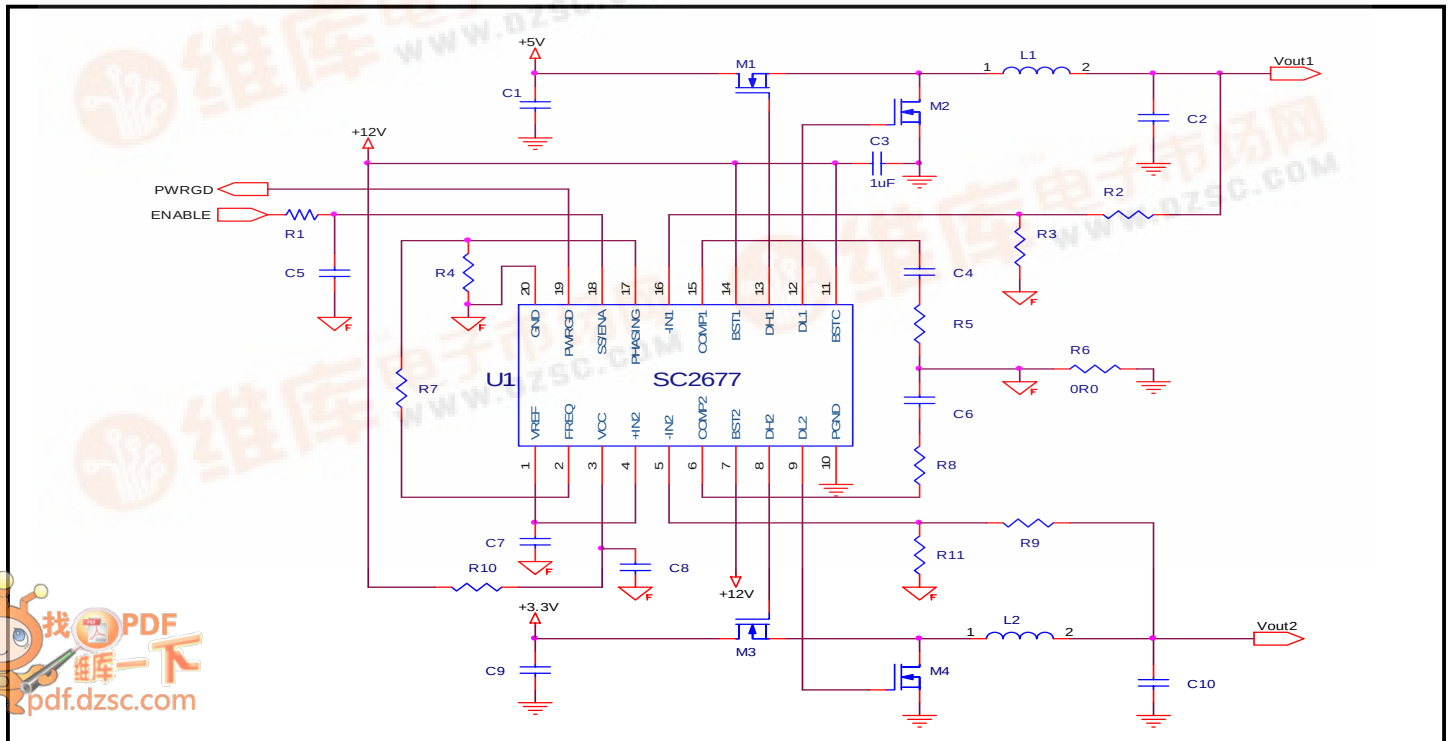
Two Phase, Current Sharing Controller

- Flexible, same or separate V_{IN}
- Programmable current sharing
- Thermal distribution via multi-phase output

Applications

- Graphics cards
- Peripheral add-in card
- Dual-Phase power supply
- Power supplies requiring two outputs

Simplified Application Schematic



Absolute Maximum Rating

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Limits	Units
V_{CC} to GND	V_{IN}	-0.3 to 15	V
PGND to GND		± 1	V
BST1, BST2 to GND		-0.3 to 20	V
BSTC to GND		-0.3 to 20	V
-IN1, +/-IN2 to GND		7	V
COMP1, COMP2 to GND		7	V
DH1, DH2 to GND		-0.3 to 20	V
DL1, DL2 to GND		-0.3 to BSTC + 0.3	V
		-3 peak (50nS) (1)	V
PWRGD to GND		V_{CC} + 0.3	V
PHASING		7	V
SS/ENA to GND		-0.3 to 7	V
Thermal Resistance Junction to Case	θ_{JC}	17	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	90	°C/W
Operating Ambient Temperature Range	T_A	0 to 70	°C
Operating Junction Temperature Range	T_J	0 to 125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	°C

Electrical Characteristics

Unless Specified: V_{CC} = 4.75 to 5.25V, GND = PGND = 0V, FB = V_O, T_J = 25°C, V_{BSTC} = V_{BST} = 12V

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage	V_{OUT} = V_{FB}	0.495	0.500	0.505	V
Supply Voltage	V_{CC}	4.5		15	V
Supply Current	V_{CC} = 5.0		10		mA
UVLO	V_{CC} Ramp up Threshold		2.84		V
UVLO Hysteresis	V_{CC}		100		mV
Reference			0.5		V
Reference Load Regulation	V_{REF} source 10uA ~ 100uA			0.2	%
Reference Line Regulation	5V < V_{CC} < 15V			0.7	%
Output Line Regulation	5V < V_{IN} < 15V			0.7	%
Gain (Gm) (Error Amplifier)	COMP pin source 100uA	4	5	6	mA/V
Bias Current Offset (Slave Error Amplifier)		-2	-1	0	mV
Max Current (Error Amplifier)	Source	200	250		uA
	Sink	400	460		uA
Input Bias Current	-IN1, +IN2, -IN2			2	µA
Short Circuit Protection Threshold		45	55	65	%
Oscillator Frequency Range		300		1000	kHz

Electrical Characteristics (Cont.)

Unless Specified: V_{CC} = 4.75 to 5.25V, GND = PGND = 0V, FB = V_O, T_J = 25°C, V_{BSTC} = V_{BST} = 12V

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	R_{SET} = 2.5kohm	450	500	550	kHz
Oscillator Max Duty Cycle	F_{OSC} = 500kHz	86	90		%
Phasing of DH2 and DL1	$V_{PHASING}$ = 0.585V		180		°C
DH Sink Current	DH - PGND = 3.5V	1.7			A
DH Sink Current	DH - PGND = 2.5V	0.85			A
DH Source Current	BSTH - DH = 3.75V	1.7			A
DH Source Current	BSTH - DH = 3V	0.85			A
DL Sink Current	DL - PGNG = 3.5V	1.7			A
DL Sink Current	DL - PGND = 2.5V	0.85			A
DL Source Current	BSTL - DL = 3.75V	1.7			A
DL Source Current	BSTL - DL = 3V	0.85			A
Dead Time	Note 5	50	85	120	ns
Soft Start Charge Current (2)			50		µA
Soft Start Enable	0% duty cycle		400		mV
Soft Start End	100% duty cycle		825		mV
Soft Start Transition Threshold(2)	Synchronous mode		1.22		V
Power Good Threshold	V_{OUT} ramping up	83%	88%	93%	V_{OUT}
Power Good Pull Down	Sink Current = 2mA			0.4	V

NOTES:

(1) Measured from 50% to 50% pulse amplitude.

(2) The soft start pin sources 50µA to an external capacitor. The converter operates in synchronous mode above the soft start transition threshold and in asynchronous mode below it.

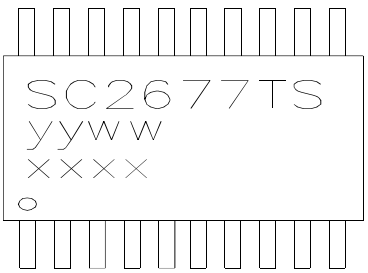
(3) Power good is an open collector output which is pulled low when the output voltage is under 75%.

(4) This device is ESD sensitive. Use of standard ESD handling precautions is required.

(5) 120ns maximum at 70°C.

Marking Information

(TSSOP-20)

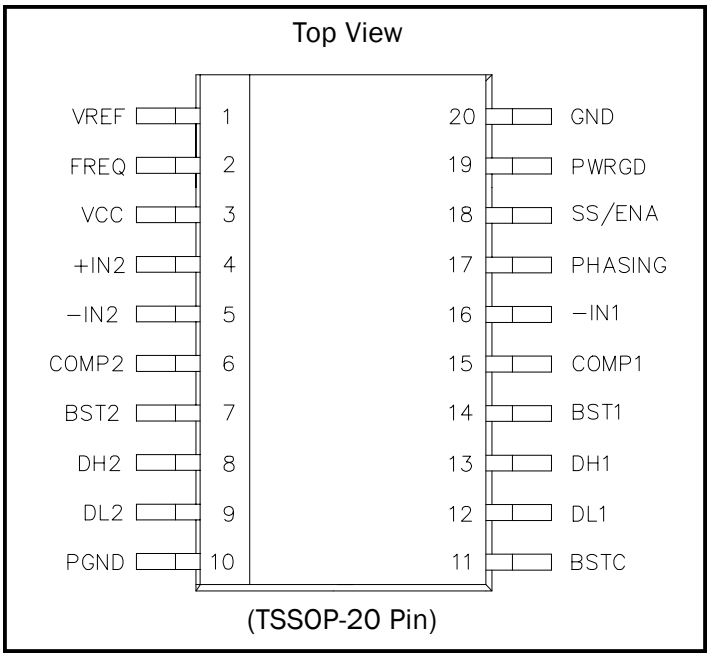


TOP

yyww = Datecode (Example: 9908)

xxxx = Semtech Lot # (Example: 90101)

Pin Configuration



(TSSOP-20 Pin)

Ordering Information

Device[1]	Package
SC2677TSTR	TSSOP-20
SC2677TSTRT[2]	TSSOP-20
SC2677EVB-1	Current Share Evaluation Board
SC2677EVB-2	Dual Channel Evaluation Board

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free package.

Pin Descriptions

EXPANDED PIN DESCRIPTION

Pin 1: (VREF)
Internal 0.5V reference. Connected to the + input of the master channel error amplifier.

Pin 2: (FREQ)
External frequency adjustment. Connect a resistor to AGND to set the switching frequency. Please see more information in Application section.

Pin 3: (VCC)
Bias pin for the controller. Connect a ceramic decoupling capacitor from this pin to AGND with minimum trace length.

Pin 4: (+IN2)
"+" input of the slave error amplifier.

Pin 5, 16: (-IN2, -IN1)
"-" inputs of the error amplifiers.

Pin 6, 15: (COMP2, COMP1)
Compensation pins of the error amplifiers.

Pin 7, 14: (BST2, BST1)
Supply pins for the high side drivers. Usually connected to bootstrap circuit.

Pin 8, 13: (DH2, DH1)
Gate drive pins for the top MOSFETs. Requires a small series resistor.

Pin 9, 12: (DL2, DL1)
Gate drive pins for the bottom MOSFETs. Requires a small series resistor.

Pin 10: (PGND)
Power GND. Return of the high side and low side gate drivers.

Pin 11: (BSTC)
Supply pin for bottom MOSFET gate drivers.

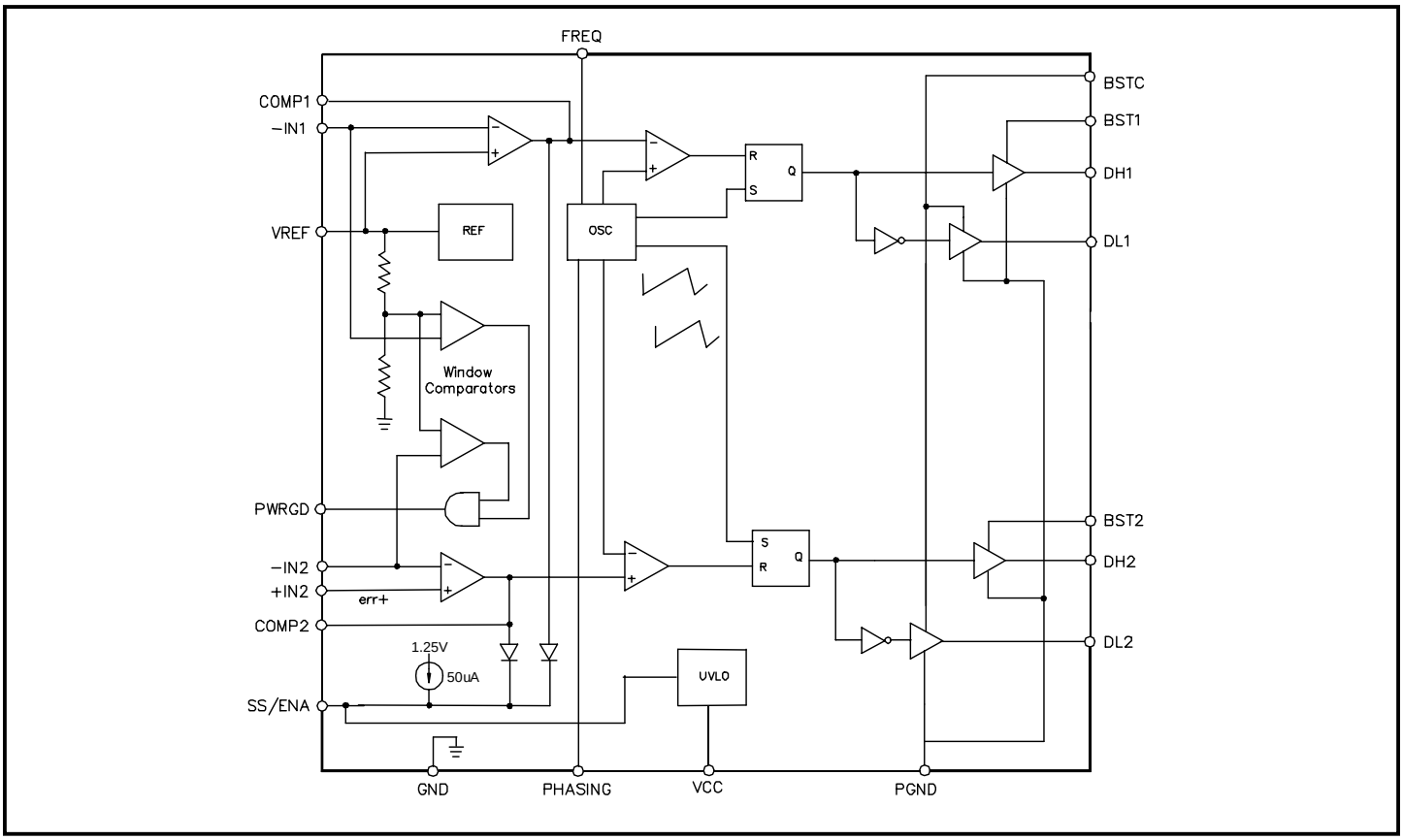
Pin 17: (PHASING)
This pin controls the phase shift between master and slave for optimum noise immunity. Use a resistive divider from the FREQ pin (pin 2) to AGND, and connect the tap of the resistive divider to pin 17. Please see more information in Application section.

Pin 18: (SS/ENA)
Soft start pin. Connect a ceramic capacitor from this pin to AGND, and there is an internal current source charging up this capacitor during soft start. The PWM operation can be disabled if this pin is pulled low.

Pin 19: (PWRGD)
Power good signal. This is an open collector output. It is pulled low internally if output voltage is outside the power good window.

Pin 20: (GND)
Analog GND. Return of the analog signals and bias of the chip.

Block Diagram



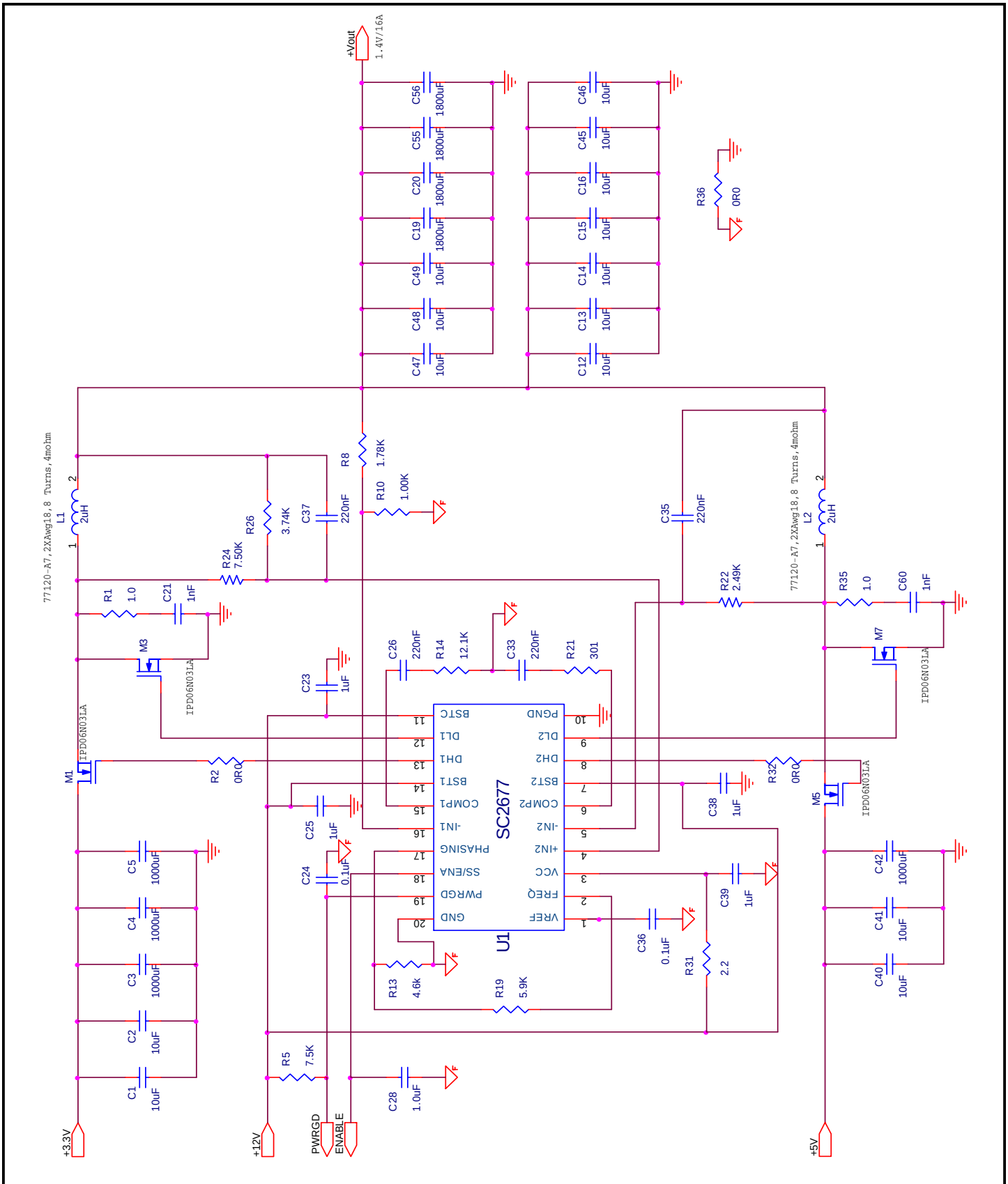
NOTES

(1) Channel 1 is the Master and Channel 2 is the Slave in current sharing configuration.

(2) For dual output operation, tie +IN2 to VREF and the two PWM channels are independent.

Evaluation Schematic

2 Channels with Current Sharing



Main Loop(s)

The SC2677 is a dual, voltage mode synchronous Buck controller. The two separate channels are identical and share only IC supply pins (Vcc and GND), output driver ground (PGND) and pre-driver supply voltage (BSTC). They also share a common oscillator generating a sawtooth waveform for channel 1 and an dephased sawtooth for channel 2. Channel 2 has both inputs of the error amplifier uncommitted and available externally. This allows the SC2677 to operate in two distinct modes.

a) Two independent channels with either common or different input voltages and different output voltages. The two channels each have their own voltage feedback path from their own output. In this mode, positive input of the error amplifier 2 is connected externally to Vref. If the application uses a common input voltage, the sawtooth phase shift between the channels provides some measure of input ripple current cancellation.

It is possible to sequence the start up of the channel with an RC delay between the reference and +IN2. The capacitor will be internally reset during UVLO and soft start.

b) Two channels operating in current sharing mode with common output voltage and either common input voltage or different input voltages. In this mode, channel 1 operates as a voltage mode Buck controller, as before, but error amp 2 monitors and amplifies the difference in voltage across the output current sense resistors of channel 1 and channel 2 (Master and Slave) and adjusts the Slave duty cycle to match output currents. To controller also works well for using the output choke winding resistance as current sensing element (please refer the application schematic for details). The amount of the current of the slave channel vs.. the master channel can be programmed according to the application. This feature is especially useful when two input sources are used and each source has its power budget.

The offset of the current sharing error amplifier is trimmed whthin the range of -2mV to 0. The polarity being such that the slave is OFF if the master has no current.

Power Good

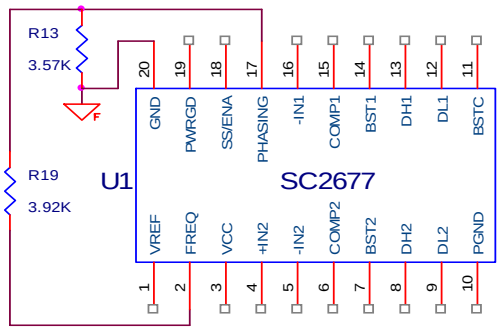
The controller provides a power good signal. This is an open collector output, which is pulled low if the output voltage is outside of the power good window.

Soft Start/Enable

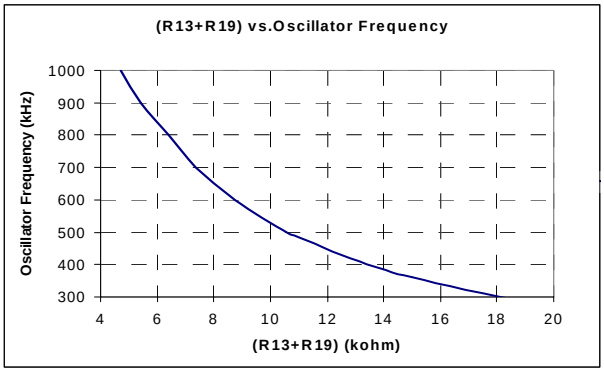
The Soft Start/Enable (SS/ENA) pin serves several functions. If held below the Enable threshold, both channels are inhibited. DH1 and DH2 will be low, turning off the top FETs. Between the Soft Start Enable threshold and the Soft Start End threshold, the duty cycle is allowed to increase. At the Soft Start End threshold, maximum duty cycle is reached. In practical applications the error amplifier will be controlling the duty cycle before the Soft Start End threshold is reached. To avoid boost problems during start-up in current share mode, both channels start up in asynchronous mode, and the bottom FET body diode is used for circulating current during the top FET off time. When the SS/ENA pin reaches the Soft Start Transition threshold, the channels begin operating in synchronous mode for improved efficiency. The soft start pin sources approximately 50uA and soft start timing can be set by selection of an appropriate soft start capacitor value.

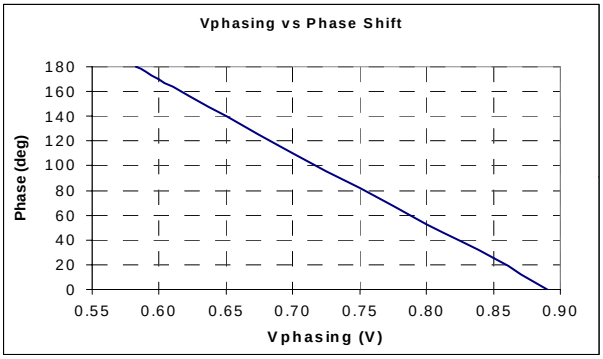
Frequency Set and Phasing

The switching frequency can be programmed by connecting a resistor from the FREQ pin to AGND. The PHASING pin controls the phase shift between the master sawtooth and slave sawtooth which allows the adjustment of the phase shift for maximum noise immunity by controlling the timing between master and slave transition. A resistive divider is used from the FREQ pin to AGND and the divided voltage is fed to the PHASING pin as depicted.



Applications Information





Shutdown

The output short circuit protection is done by output undervoltage detection. Upon output short circuit and when the output voltage drops bellow a certain percentage of the regulation target (see elctrical characteristics table for details, the PWM will be disabled and the output will be dsiabbled and latched off. The latch can be reset by power cycling.

Layout Guidelines

Power and signal traces must be kept separated for noise considerations. Feedback, current sense traces and analog ground should not cross any traces or planes carrying high switching currents, such as in the input loop or the phase node.

The input loop, consisting of the input capacitors and both MOSFETs must be kept as small as possible. Since all of the high switching currents occur in the input loop, the enclosed loop area must be kept small to minimize inductance and radiated and conducted noise emissions. Designing for minimum trace length is not the only factor for best design, often a more optimum layout can be achieved by keeping the wide trace and using proper layer stacking to minimize the stray inductance.

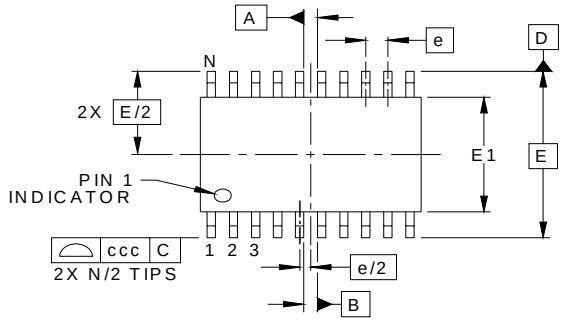
It is important to keep the gate traces short, the IC must be close to the power switches. It is recommended to use at least 25 mil width or wider trace when ever possible. A good placement can help if the controller is placed in the middle of the two PWM channels.

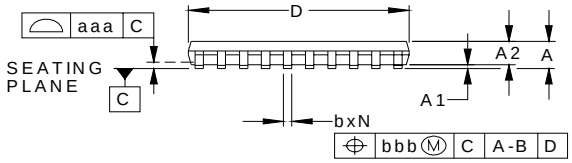
Grounding requirements are always important in a buck converter layout, especially at high power. Power ground (PGND) should be returned to the bottom MOSFET source to provide the best gate current return path. Analog ground (GND) shape should be used for the anaglog returns such as chip decoupling, frequency setiing, reference voltage (or soft starting cap), and the compensation. This groung shap should be single point connected to the PGND shape near the ground side of the output capacitors. This will provide noise free analog ground for operation stablity, and also provide best possible remote sensing for the feedback voltage. In case two output rails need to be regulated, the AGND shape should single point connected to the geometrica center of the PGND for the two point of loads. The single ponit tie is a must to prevent the power current from flowing on the AGND shape, so that the analog circuitry in the controller has an electrically quiet reference and to provide the greatest noise free operation. Keep in mind that the AGND pin is never allowed to have bigger than 1V voltage difference vs the PGND pin. This usually achievable by using a ground plan for PGND in PCB layout. Using ground plane for PGND can reduce the physical separation between the two grounds, such that even the fast current transitions in the PGND plane can not generate voltage spikes exceeding the 1V level, therefore preventing unstable and erratic behavior from happening.

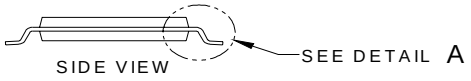
The feedback divider must be close to the IC and be returned to analog ground. Current sense traces must be run parallel and close to each other and to analog ground.

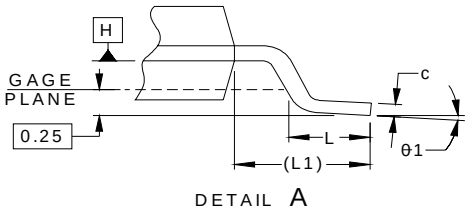
The IC must have a ceramic decoupling capacitor across its supply pins, mounted as close to the device as possible. The small ceramic, noise-filtering capacitors on the current sense lines should also be placed as close to the IC as possible.

Outline Drawing - TSSOP-20







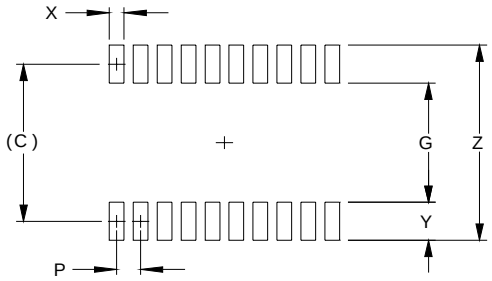


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.251	.255	.259	6.40	6.50	6.60
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	20			20		
θ1	0	-	8	0	-	8
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AC.

Land Pattern - TSSOP-20



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804