## DATA SHEET

# **74LVC00A**Quad 2-input NAND gate

Product specification
Supersedes data of 1997 Aug 11
IC24 Data Handbook

1998 Apr 28





### **Quad 2-input NAND gate**

**74LVC00A** 

#### **FEATURES**

- Wide supply range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5V
- CMOS low power consumption
- Direct interface with TTL levels
- 5-volt tolerant inputs, for interfacing with 5-volt logic

#### **DESCRIPTION**

The 74LVC00A is a high-performance, low power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in a mixed 3.3 V/5 V

Schmitt-trigger action at all inputs makes the circuit tolerant for slower input rise and fall times.

The 74LVC00A provides the 2-input NAND function.

#### **QUICK REFERENCE DATA**

GND = 0 V;  $T_{amb} = 25^{\circ}C$ ;  $t_r = t_f \le 2.5 \text{ ns}$ 

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PHL</sub> t <sub>PLH</sub>	Propagation delay nA, nB to nY	$C_L = 50 \text{ pF};$ $V_{CC} = 3.3 \text{ V}$	3.0	ns
C <sub>I</sub>	Input capacitance		5.0	pF
C <sub>PD</sub>	Power dissipation capacitance per gate	$V_I = GND \text{ to } V_{CC}^1$	28	pF

#### NOTES:

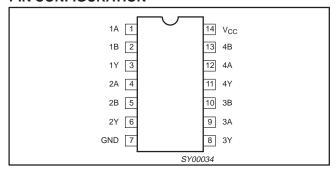
1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W)  $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  $f_0$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of the outputs.}$ 

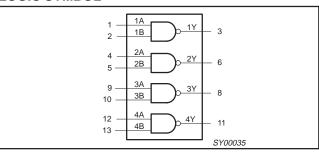
#### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	-40°C to +85°C	74LVC00A D	74LVC00A D	SOT108-1
14-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC00A DB	74LVC00A DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC00A PW	74LVC00APW DH	SOT402-1

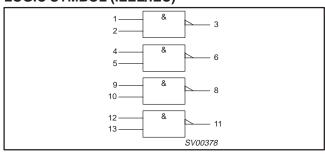
#### **PIN CONFIGURATION**



#### **LOGIC SYMBOL**



#### LOGIC SYMBOL (IEEE/IEC)



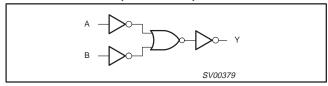
#### PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION				
1, 4, 9, 12	1A – 4A	Data inputs				
2, 5, 10, 13	1B – 4B					
3, 6, 8, 11	1Y – 4Y	Data outputs				
7	GND	Ground (0 V)				
14	V <sub>CC</sub>	Positive supply voltage				

## Quad 2-input NAND gate

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#### **LOGIC DIAGRAM (ONE GATE)**



#### **FUNCTION TABLE**

INP	OUTPUTS	
nA	nY	
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

#### NOTES:

H = HIGH voltage level L = LOW voltage level

#### **RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	CONDITIONS	LIM	IITS	UNIT
STWIBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V <sub>CC</sub>	DC supply voltage (for max. speed performance)		2.7	3.6	V
V <sub>CC</sub>	DC supply voltage (for low-voltage applications)		1.2	3.6	V
VI	DC Input voltage range		0	5.5	V
Vo	DC output voltage range		0	V <sub>CC</sub>	V
T <sub>amb</sub>	Operating ambient temperature range in free-air		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input rise and fall times	$V_{CC} = 1.2 \text{ to } 2.7V$ $V_{CC} = 2.7 \text{ to } 3.6V$	0	20 10	ns/V

#### ABSOLUTE MAXIMUM RATINGS1

Absolute Maximum Rating System (IEC 134) Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage (for max. speed performance)		-0.5 to +6.5	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
VI	DC input voltage	Note 2	-0.5 to +5.5	V
I <sub>OK</sub>	DC output diode current	$V_{O} > V_{CC}$ or $V_{O} < 0$	±50	mA
V <sub>O</sub>	DC output voltage	Note 2	$-0.5$ to $V_{CC} + 0.5$	V
ΙO	DC output source or sink current	$V_O = 0$ to $V_{CC}$	±50	mA
I <sub>GND</sub> , I <sub>CC</sub>	DC V <sub>CC</sub> or GND current		±100	mA
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C
P <sub>TOT</sub>	Power dissipation per package  – plastic mini-pack (SO)  – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	500 500	mW

#### NOTES:

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<sup>1.</sup> Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## Quad 2-input NAND gate

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#### **DC CHARACTERISTICS**

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

			ı	IMITS		
SYMBOL	PARAMETER	TEST CONDITIONS	Temp = -	40°C to	+85°C	UNIT
			MIN	TYP <sup>1</sup>	MAX	
W	LUCI Lloyel Input voltoge	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 2.7 to 3.6V	2.0			ľ
	LOW/ Joyal Japut valtage	V <sub>CC</sub> = 1.2V			GND	
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 2.7 to 3.6V			0.8	
		$V_{CC} = 2.7V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -12mA$	V <sub>CC</sub> - 0.5			
	HICH lovel output voltage	$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -100\mu A$	V <sub>CC</sub> -0.2	V <sub>CC</sub>		
V <sub>OH</sub>	HIGH level output voltage	$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -18$ mA	V <sub>CC</sub> -0.6		]	
		$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = -24$ mA	V <sub>CC</sub> -0.8			
		$V_{CC} = 2.7V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 12$ mA			0.40	
$V_{OL}$	LOW level output voltage	$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$			0.20	V
		$V_{CC} = 3.0V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 24$ mA			0.55	
t <sub>l</sub>	Input leakage current	$V_{CC} = 3.6V; V_I = 5.5V \text{ or GND}$		±0.1	±5	μΑ
I <sub>CC</sub>	Quiescent supply current	$V_{CC} = 3.6V$ ; $V_I = V_{CC}$ or GND; $I_O = 0$		0.1	10	μА
Δl <sub>CC</sub>	Additional quiescent supply current per input pin	$V_{CC} = 2.7V$ to 3.6V; $V_I = V_{CC} - 0.6V$ ; $I_O = 0$		5	500	μА

#### NOTES:

#### **AC CHARACTERISTICS**

 $GND = 0 \text{ V}; t_r = t_f \le 2.5 \text{ ns}; C_L = 50 \text{ pF}$ 

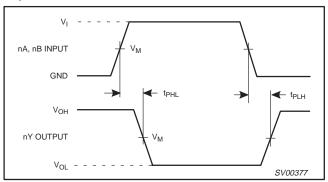
				LIMITS							
SYMBOL PARAMETER		WAVEFORM	$V_{CC} = 3.3V \pm 0.3V$			\	/ <sub>CC</sub> = 2.7\	1	V <sub>CC</sub> = 1.2V	UNIT	
			MIN	TYP <sup>1</sup>	MAX	MIN	TYP	MAX	TYP		
t <sub>PHL</sub> /	Propagation delay nA, nB to nY	1, 2	1.5	3.0	5.0	1.5	3.4	5.8	11	ns	

#### NOTE:

#### **AC WAVEFORMS**

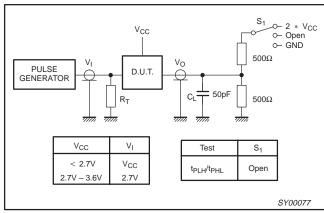
 $V_M = 1.5 \text{ V at } V_{CC} \ge 2.7 \text{ V}$  $V_M = 0.5 \bullet V_{CC} \text{ at } V_{CC} < 2.7 \text{ V}$ 

 $\rm V_{OL}$  and  $\rm V_{OH}$  are the typical output voltage drop that occur with the output load.



Waveform 1. Input (nA) to output (nY) propagation delays.

#### **TEST CIRCUIT**



Waveform 2. Load circuitry for switching times.

<sup>1.</sup> All typical values are at  $V_{CC}$  = 3.3V and  $T_{amb}$  = 25°C.

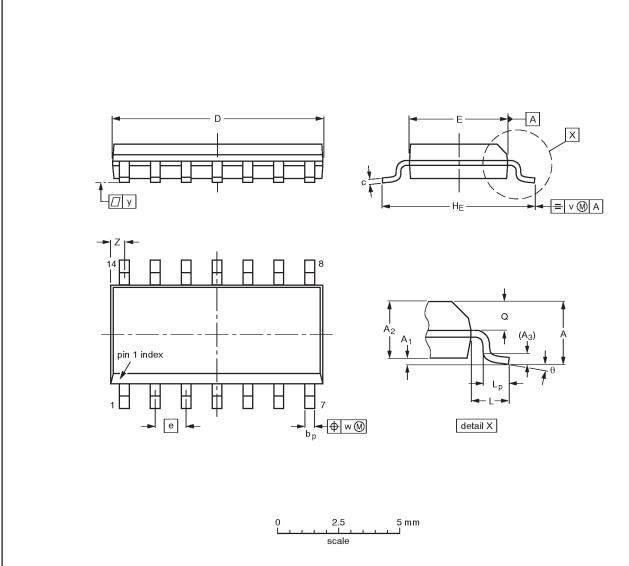
<sup>1.</sup> These typical values are at  $V_{CC}$  = 3.3V and  $T_{amb}$  = 25°C.

## Quad 2-input NAND gate

74LVC00A

#### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



#### DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Ø	v	w	у	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01		0.0098 0.0075		0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016		0.01	0.01	0.004	0.028 0.012	0°

#### Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

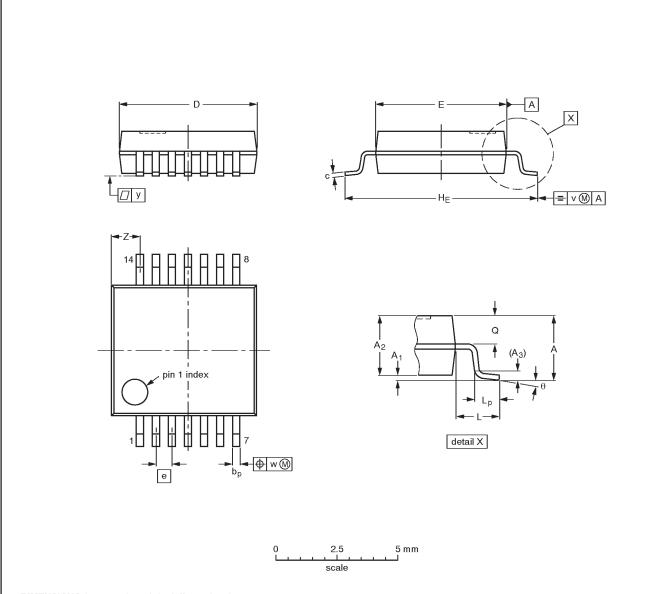
OUTLINE		EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	EIAJ	PROJECTION		
SOT108-1	076E06S	MS-012AB			<del>91-08-13-</del> 95-01-23	

## Quad 2-input NAND gate

74LVC00A

#### SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



#### DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	bp	c	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

#### Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

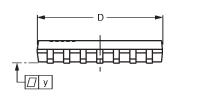
OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE	
SOT337-1		MO-150AB			<del>-95-02-04</del> 96-01-18	

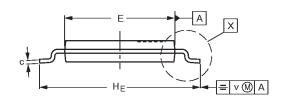
## Quad 2-input NAND gate

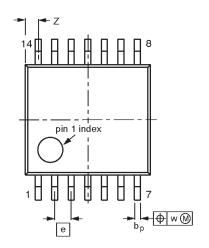
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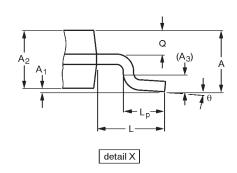
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

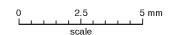
SOT402-1











#### DIMENSIONS (mm are the original dimensions)

UNIT	A max.	Α1	A <sub>2</sub>	A <sub>3</sub>	bр	c	D <sup>(1)</sup>	E <sup>(2)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	IEC JEDEC EIAJ				ISSUE DATE	
SOT402-1		MO-153				<del>94-07-12</del> 95-04-04	

## Quad 2-input NAND gate

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Data Sheet Identification	Product Status	Definition				
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.				
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