INTEGRATED CIRCUITS

DATA SHEET

74LVC1G126
Bus buffer/line driver; 3-state

Product specification
Supersedes data of 2002 Oct 02

2004 Sep 21

Philips
Semiconductors

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FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

DESCRIPTION

The 74LVC1G126 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC1G126 provides one non-inverting buffer/line driver with 3-state output. The 3-state output is controlled by the output enable input (OE). A low level at pin OE causes the output to assume a high-impedance OFF-state.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay input A to output Y	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	3.0	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	2.1	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	2.3	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	2.0	ns
		V_{CC} = 5.0 V; C_L = 50 pF; R_L = 500 Ω	1.7	ns
C_I	input capacitance		5	pF
C_{PD}	power dissipation capacitance	output enabled; notes 1 and 2	25	pF
		output disabled; notes 1 and 2	6	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz;

   f_o = output frequency in MHz;

   C_L = output load capacitance in pF;

   V_{CC} = supply voltage in Volts;

   N = total switching outputs;

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
OE	A	Y
H	L	L
H	H	H
L	X	Z

Note

1. H = HIGH voltage level;
   L = LOW voltage level;
   X = don’t care;
   Z = high-impedance OFF-state.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC1G126GW	–40 °C to +125 °C	5	TSSOP5	plastic	SOT353	VN
74LVC1G126GV	–40 °C to +125 °C	5	SC-74A	plastic	SOT753	V26
74LVC1G126GM	–40 °C to +125 °C	6	XSON6	plastic	SOT886	VN

PINNING

PIN TSSOP5; SC-74A	PIN XSON6	SYMBOL	DESCRIPTION
1	1	OE	output enable input
2	2	A	data input A
3	3	GND	ground (0 V)
4	4	Y	data output Y
-	5	n.c.	not connected
5	6	V_{CC}	supply voltage

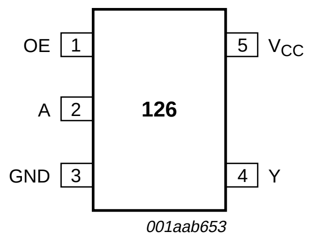


Fig.1 Pin configuration SC-88A; SC-74A.

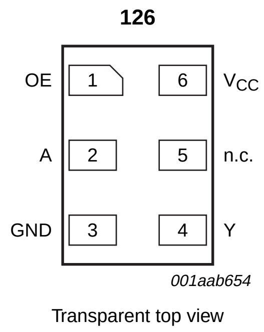


Fig.2 Pin configuration XSON6.

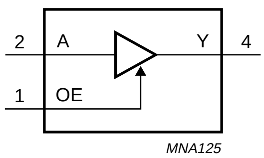


Fig.3 Logic symbol.

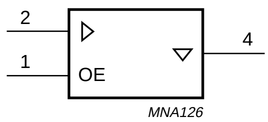


Fig.4 IEE/IEC logic symbol.

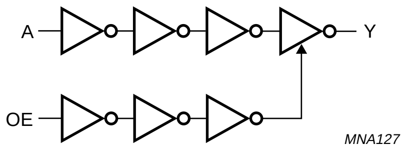


Fig.5 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage	V_{CC} = 1.65 V to 5.5 V; enable mode	0	V_{CC}	V
		V_{CC} = 1.65 V to 5.5 V; disable mode	0	5.5	V
		V_{CC} = 0 V; Power-down mode	0	5.5	V
T_{amb}	operating ambient temperature		–40	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.65 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	0	10	ns/V

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	–	±50	mA
V_O	output voltage	enable mode; notes 1 and 2	–0.5	V_{CC} + 0.5	V
		disable mode; notes 1 and 2	–0.5	+6.5	V
		Power-down mode; notes 1 and 2	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	T_{amb} = –40 °C to +125 °C	–	250	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[1]	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 °C to +85 °C							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	0.65 × V_{CC}	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V_{CC}	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V_{CC}	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA	1.65 to 5.5	–	–	0.1	V
		I_O = 4 mA	1.65	–	–	0.45	V
		I_O = 8 mA	2.3	–	–	0.3	V
		I_O = 12 mA	2.7	–	–	0.4	V
		I_O = 24 mA	3.0	–	–	0.55	V
		I_O = 32 mA	4.5	–	–	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –100 μA	1.65 to 5.5	V_{CC} – 0.1	–	–	V
		I_O = –4 mA	1.65	1.2	–	–	V
		I_O = –8 mA	2.3	1.9	–	–	V
		I_O = –12 mA	2.7	2.2	–	–	V
		I_O = –24 mA	3.0	2.3	–	–	V
		I_O = –32 mA	4.5	3.8	–	–	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	±0.1	±5	μA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; V_O = 5.5 V or GND	5.5	–	±0.1	±10	μA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V	0	–	±0.1	±10	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A	5.5	–	0.1	10	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A	2.3 to 5.5	–	5	500	μA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[1]	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 °C to +125 °C							
V_{IH}	HIGH-level input voltage		1.65 to 1.95	0.65 × V_{CC}	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V_{CC}	–	–	V
V_{IL}	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V_{CC}	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V_{CC}	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 μA	1.65 to 5.5	–	–	0.1	V
		I_O = 4 mA	1.65	–	–	0.70	V
		I_O = 8 mA	2.3	–	–	0.45	V
		I_O = 12 mA	2.7	–	–	0.60	V
		I_O = 24 mA	3.0	–	–	0.80	V
		I_O = 32 mA	4.5	–	–	0.80	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –100 μA	1.65 to 5.5	V_{CC} – 0.1	–	–	V
		I_O = –4 mA	1.65	0.95	–	–	V
		I_O = –8 mA	2.3	1.7	–	–	V
		I_O = –12 mA	2.7	1.9	–	–	V
		I_O = –24 mA	3.0	2.0	–	–	V
		I_O = –32 mA	4.5	3.4	–	–	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	–	±100	μA
I_{OZ}	3-state output OFF-state current	$V_I = V_{IH}$ or V_{IL}; V_O = 5.5 V or GND	5.5	–	–	±200	μA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V	0	–	–	±200	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A	5.5	–	–	200	μA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A	2.3 to 5.5	–	–	5000	μA

Note

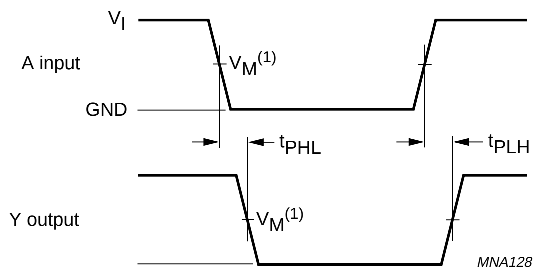
1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.0$ ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = –40 °C to +85 °C							
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 6 and 8	1.65 to 1.95	1.0	3.0	8.0	ns
			2.3 to 2.7	0.5	2.1	5.5	ns
			2.7	0.5	2.3	5.5	ns
			3.0 to 3.6	0.5	2.0	4.5	ns
			4.5 to 5.5	0.5	1.7	4.0	ns
t_{PZH}/t_{PZL}	3-state output enable time input OE to Y	see Figs 7 and 8	1.65 to 1.95	1.0	3.2	9.4	ns
			2.3 to 2.7	0.5	2.2	6.6	ns
			2.7	0.5	2.4	6.6	ns
			3.0 to 3.6	0.5	2.1	5.3	ns
			4.5 to 5.5	0.5	1.6	5.0	ns
t_{PHZ}/t_{PLZ}	3-state output disable time input OE to Y	see Figs 7 and 8	1.65 to 1.95	1.0	4.3	9.2	ns
			2.3 to 2.7	0.5	2.7	5.5	ns
			2.7	0.5	3.4	5.5	ns
			3.0 to 3.6	0.5	3.0	5.5	ns
			4.5 to 5.5	0.5	2.2	4.2	ns
T_{amb} = –40 °C to +125 °C							
t_{PHL}/t_{PLH}	propagation delay A to Y	see Figs 6 and 8	1.65 to 1.95	1.0	–	10.5	ns
			2.3 to 2.7	0.5	–	7	ns
			2.7	0.5	–	7	ns
			3.0 to 3.6	0.5	–	6	ns
			4.5 to 5.5	0.5	–	5.5	ns
t_{PZH}/t_{PZL}	3-state output enable time input OE to Y	see Figs 7 and 8	1.65 to 1.95	1.0	–	12	ns
			2.3 to 2.7	0.5	–	8.5	ns
			2.7	0.5	–	8.5	ns
			3.0 to 3.6	0.5	–	7	ns
			4.5 to 5.5	0.5	–	6.5	ns
t_{PHZ}/t_{PLZ}	3-state output disable time input OE to Y	see Figs 7 and 8	1.65 to 1.95	1.0	–	12	ns
			2.3 to 2.7	0.5	–	7	ns
			2.7	0.5	–	7	ns
			3.0 to 3.6	0.5	–	7	ns
			4.5 to 5.5	0.5	–	5.5	ns

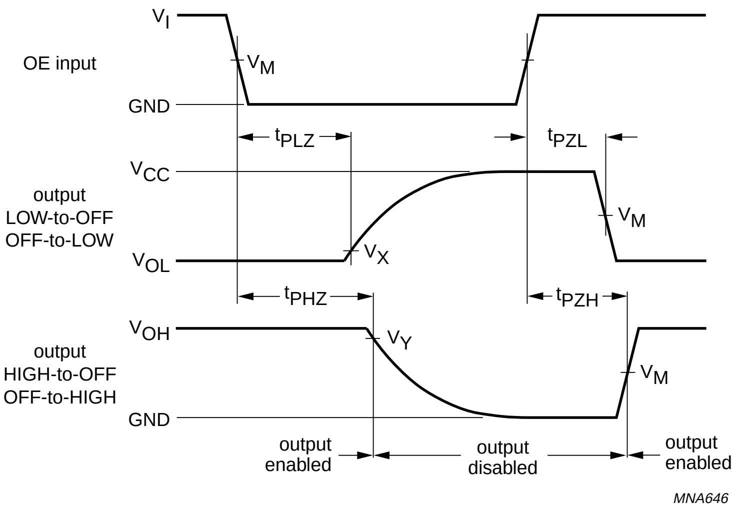
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 V to 1.95 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V_{CC}	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.6 Input A to output Y propagation delay times.

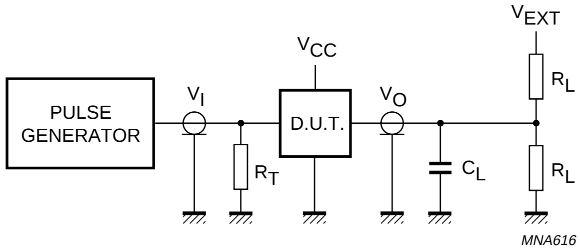


V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 V to 1.95 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V_{CC}	V_{CC}	≤ 2.5 ns

$V_X = V_{OL} + 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_X = V_{OL} + 0.15$ V at $V_{CC} < 2.7$ V;
$V_Y = V_{OH} - 0.3$ V at $V_{CC} \geq 2.7$ V;
$V_Y = V_{OH} - 0.15$ V at $V_{CC} < 2.7$ V.

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.7 3-state enable and disable times.



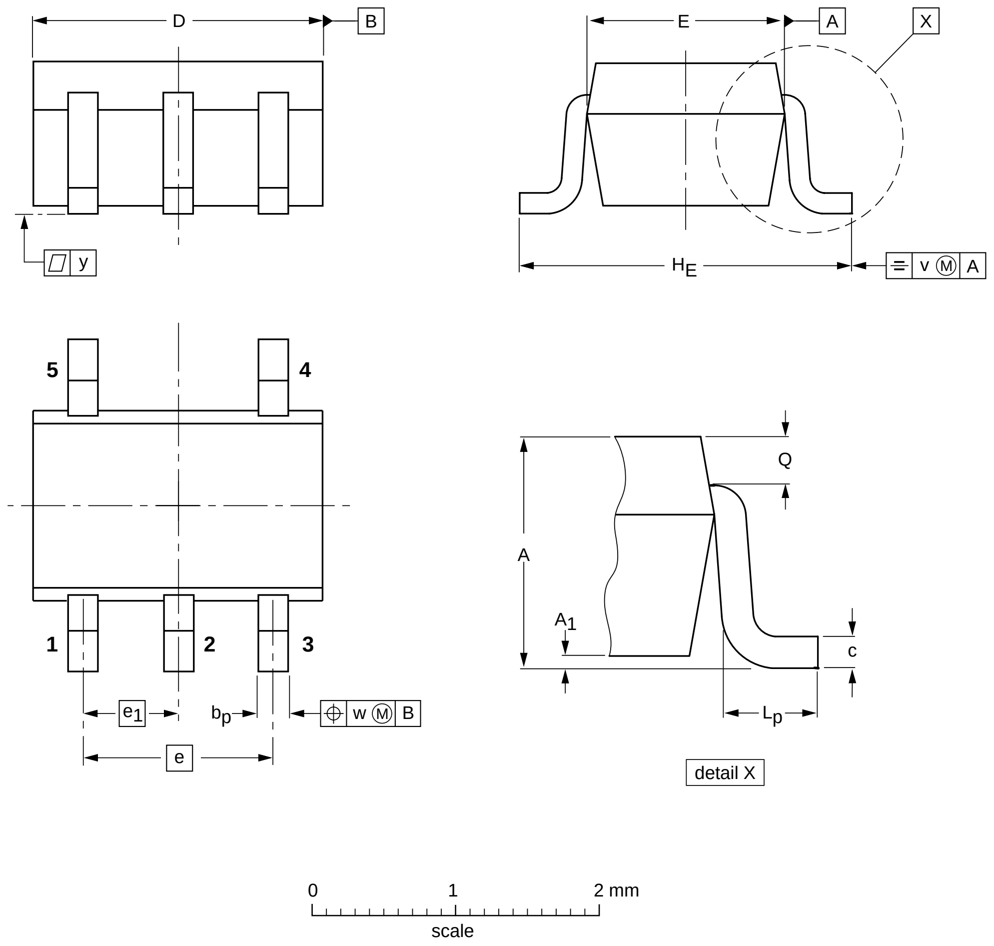
V_{CC}	V_I	C_L	R_L	V_{EXT}		
				t_{PLH}/t_{PHL}	t_{PZH}/t_{PHZ}	t_{PZL}/t_{PLZ}
1.65 V to 1.95 V	V_{CC}	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	30 pF	500 Ω	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	50 pF	500 Ω	open	GND	$2 \times V_{CC}$

Definitions for test circuits:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.8 Load circuitry for switching times.

PACKAGE OUTLINES

Plastic surface mounted package; 5 leads **SOT353**

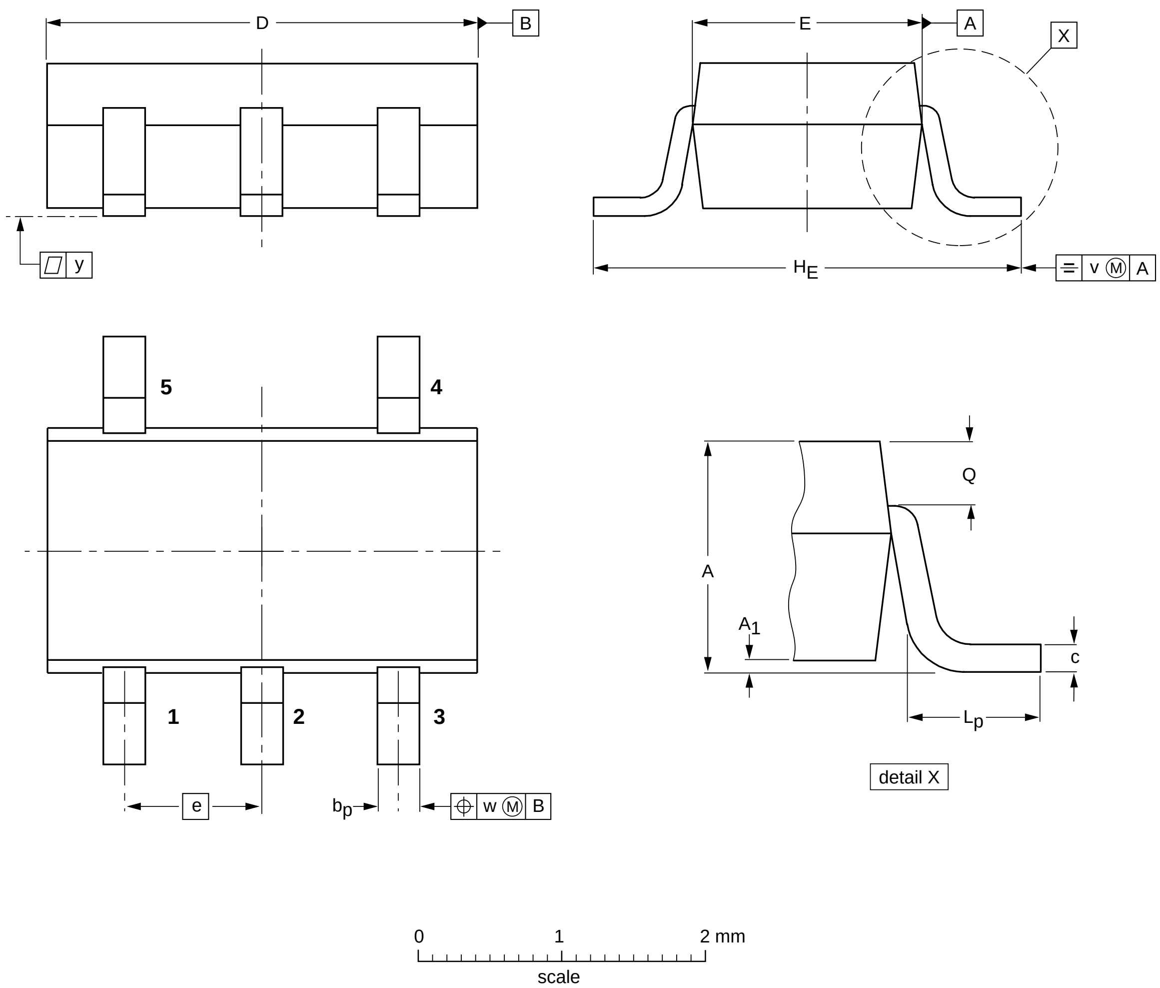


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

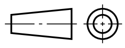
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

Plastic surface mounted package; 5 leads **SOT753**

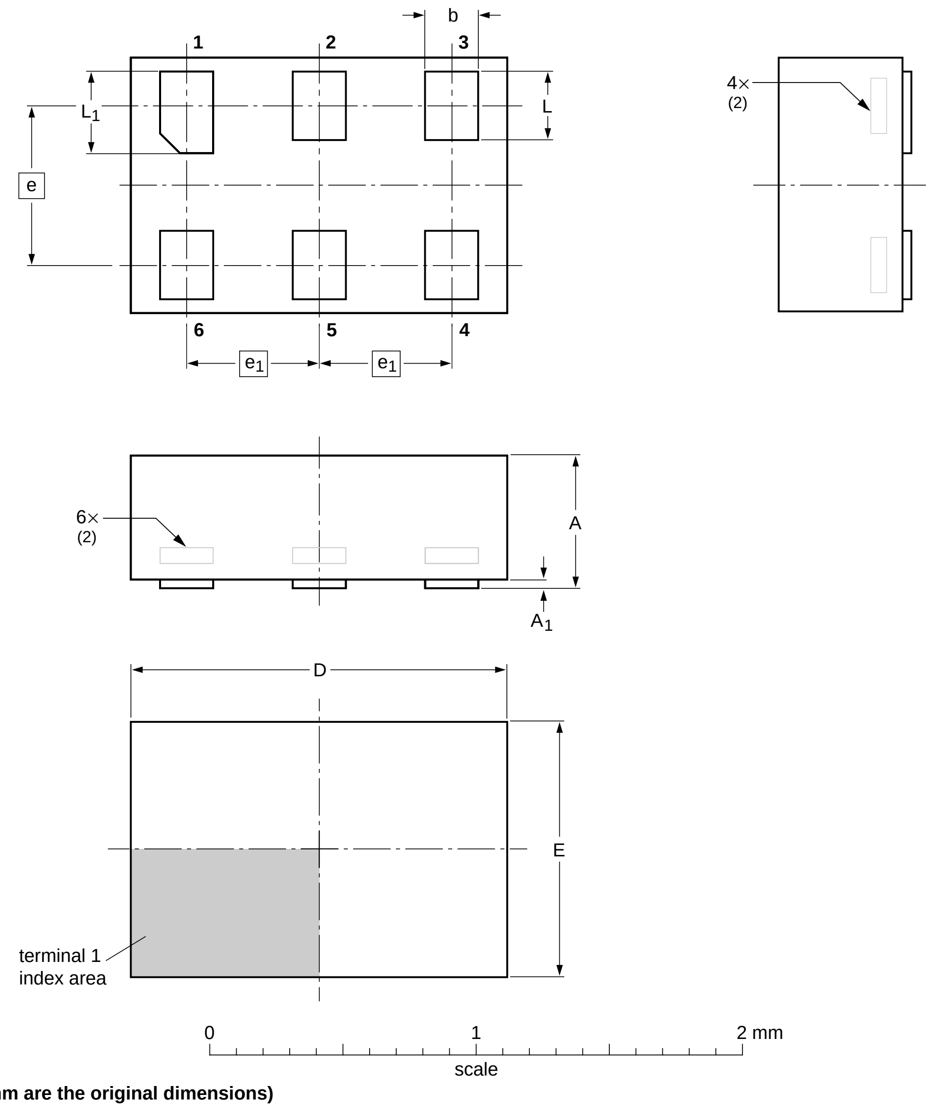


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			02-04-16

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm **SOT886**



DIMENSIONS (mm are the original dimensions)

UNIT	A (1) max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-15~~ 04-07-22

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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