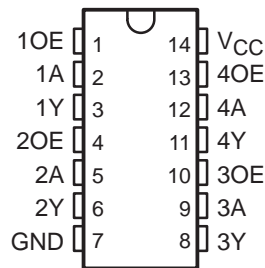


- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages**

**D, DB, DGV, OR PW PACKAGE (TOP VIEW)**



**description**

This quadruple bus buffer gate is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC126A features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC126A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

**FUNCTION TABLE**  
(each buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z



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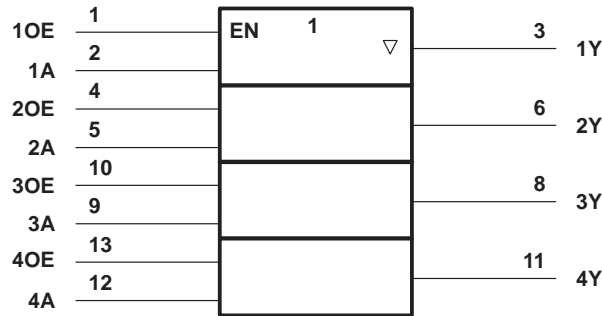
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# SN74LVC126A

## QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

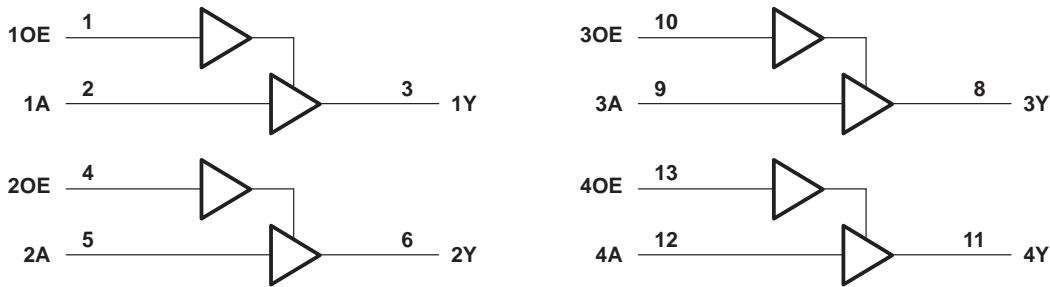
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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 6.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50 mA
Continuous output current, $I_O$ .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 3):	
D package .....	127°C/W
DB package .....	158°C/W
DGV package .....	182°C/W
PW package .....	170°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.
  3. The package thermal impedance is calculated in accordance with JESD 51.

**recommended operating conditions (see Note 4)**

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		
V <sub>I</sub>	Input voltage	0	5.5	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	-4		mA
		V <sub>CC</sub> = 2.3 V	-8		
		V <sub>CC</sub> = 2.7 V	-12		
		V <sub>CC</sub> = 3 V	-24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4		mA
		V <sub>CC</sub> = 2.3 V	8		
		V <sub>CC</sub> = 2.7 V	12		
		V <sub>CC</sub> = 3 V	24		
Δt/Δv	Input transition rise or fall rate	0	10	ns/V	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> -0.2		V	
	I <sub>OH</sub> = -4 mA	1.65 V	1.2			
	I <sub>OH</sub> = -8 mA	2.3 V	1.7			
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			
		3 V	2.4			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V	0.2		V	
	I <sub>OL</sub> = 4 mA	1.65 V	0.45			
	I <sub>OL</sub> = 8 mA	2.3 V	0.7			
	I <sub>OL</sub> = 12 mA	2.7 V	0.4			
	I <sub>OL</sub> = 24 mA	3 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V			±5	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.6 V			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			10	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	4.5			pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	7			pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**SN74LVC126A**  
**QUADRUPLE BUS BUFFER GATE**  
**WITH 3-STATE OUTPUTS**

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**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	13.2	1	7.2	5.2		1	4.7	ns
t <sub>en</sub>	OE	Y	14.3	1	8.3	6.3		1	5.7	ns
t <sub>dis</sub>	OE	Y	14.7	1	8.7	6.7		1.3	6	ns
t <sub>sk(o)</sub> <sup>†</sup>								1		ns

<sup>†</sup> Skew between any two outputs of the same package switching in the same direction

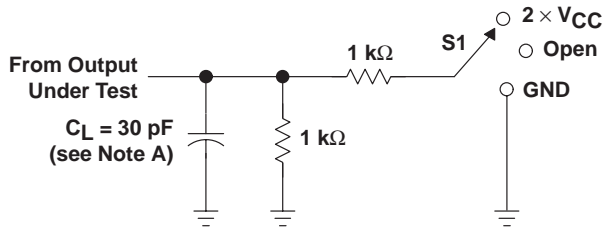
**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT	
			TYP	TYP	TYP		
C <sub>pd</sub>	Power dissipation capacitance per gate	Outputs enabled	f = 10 MHz	20	21	22	pF
		Outputs disabled		2	3	4	



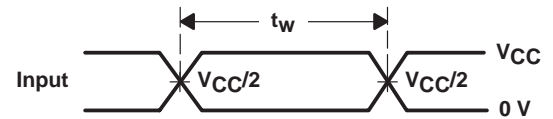
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$

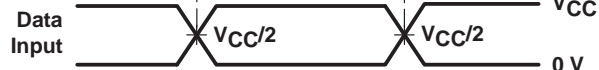


LOAD CIRCUIT

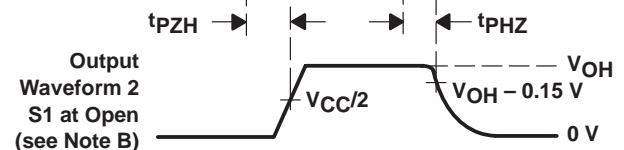
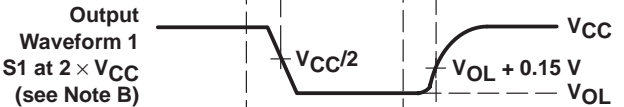
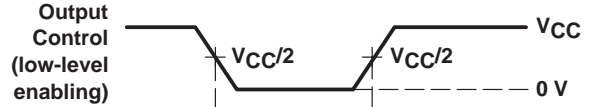
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	Open



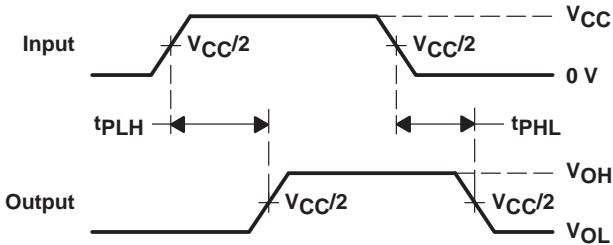
VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

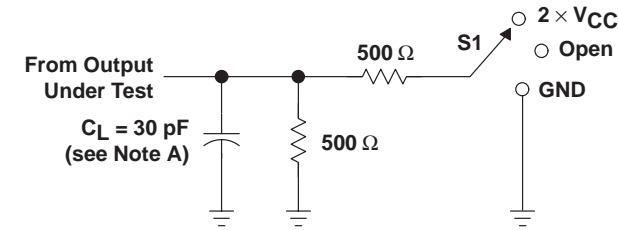
Figure 1. Load Circuit and Voltage Waveforms

# SN74LVC126A QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUTS

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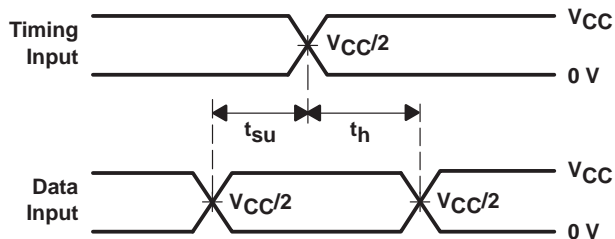
## PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

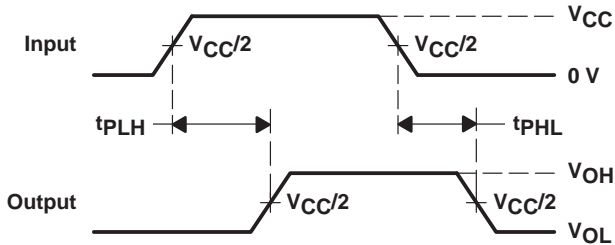


LOAD CIRCUIT

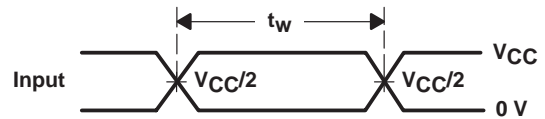
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



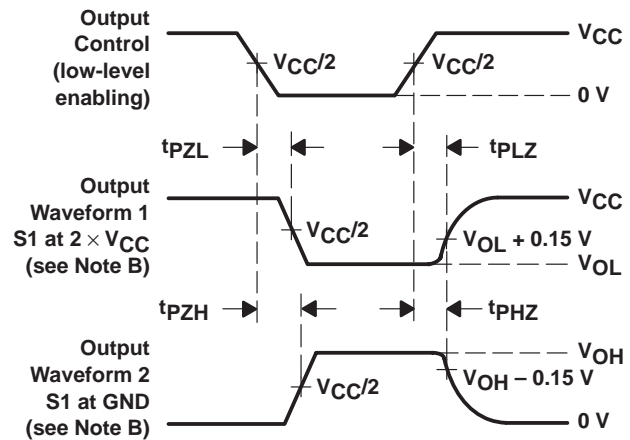
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION

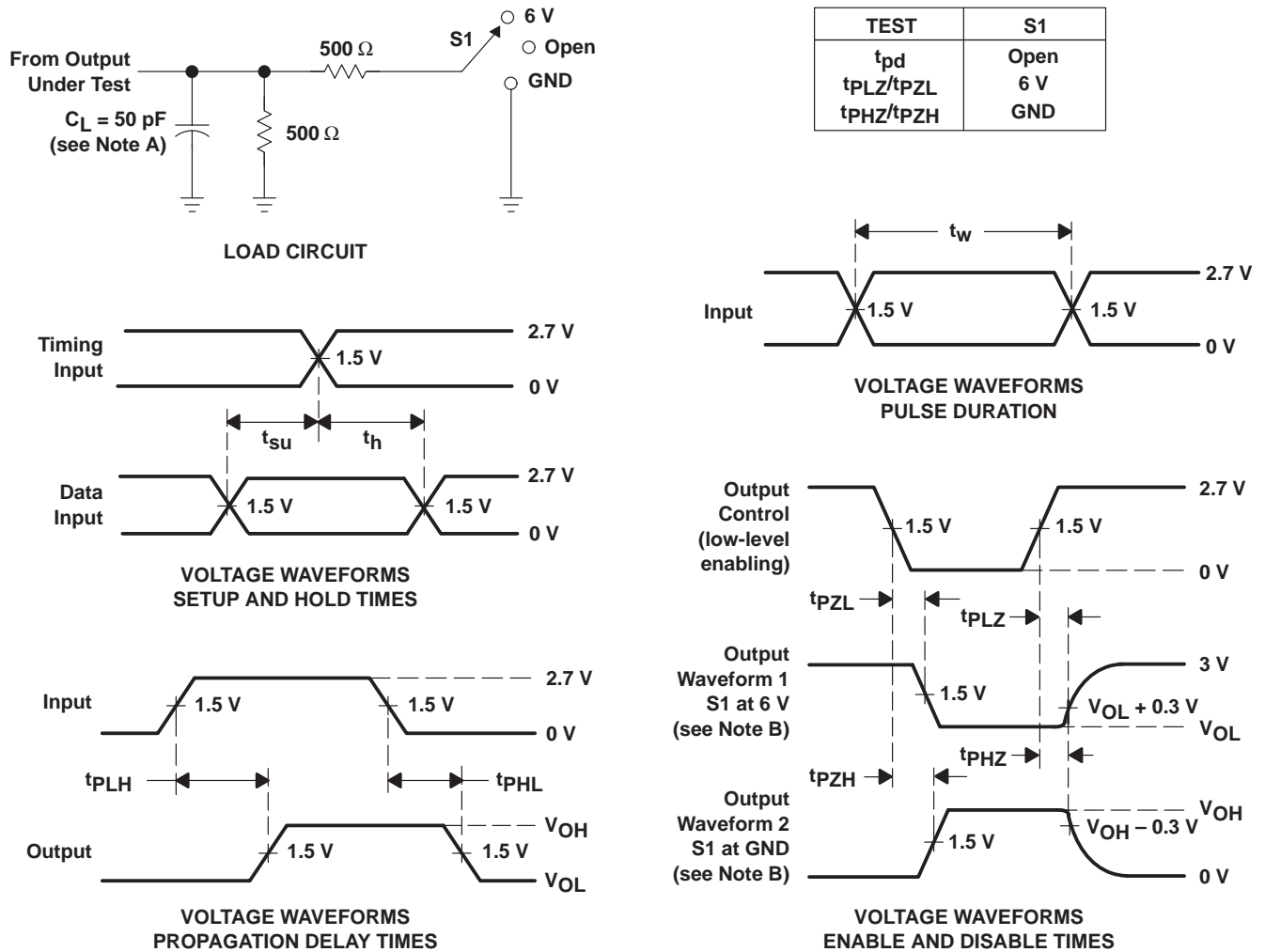


VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION**  
 **$V_{CC} = 2.7\text{ V}$  AND  $3.3\text{ V} \pm 0.3\text{ V}$**



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 3. Load Circuit and Voltage Waveforms**

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