

DATA SHEET

74LVC652

Octal transceiver/register with dual enable (3-State)

Product specification
Supersedes data of 1993 Dec 01
IC24 Data Handbook

1998 Jul 29

Octal transceiver/register with dual enable (3-State)

74LVC652

***FEATURES**

- Wide supply voltage range of 1.2V to 3.6V
- In accordance with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

DESCRIPTION

The 74LVC652 is a high performance, low-power, low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC652 consist of 8 non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' or both buses, will be stored in the internal registers, at the appropriate clock inputs (CPAB or CPBA) regardless of the select inputs (SAB and SBA) or output enable (OEAB and OEBA) control inputs. Depending on the select inputs SAB and SBA data can directly go from input to output (real time mode) or data can be controlled by the clock (storage mode), this is when the OEn inputs this operating mode permits. The output enable inputs OEAB and OEBA determine the operation mode of the transceiver.

When OEAB is LOW, no data transmission from An to Bn is possible and when \overline{OEBA} is HIGH, there is no data transmission from Bn to An possible. When SAB and SBA are in the real time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and \overline{OEBA} . In this configuration each output reinforces its input.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}\text{C}$; $t_r = t_f \leq 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay A _n to B _n ; B _n to A _n	$C_L = 50\text{pF}$ $V_{CC} = 3.3\text{V}$	5.0	ns
f_{max}	Maximum clock frequency		150	MHz
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per latch	Notes 1, 2	45	pF

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacitance in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.
2. The condition is $V_I = \text{GND to } V_{CC}$.

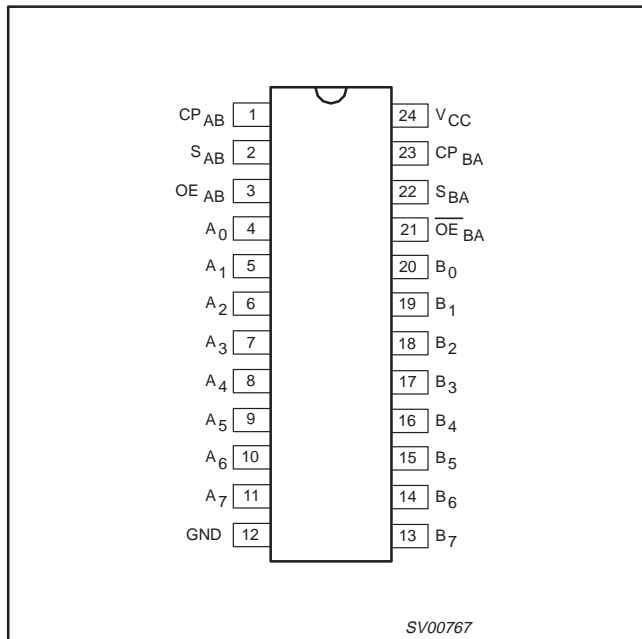
ORDERING AND PACKAGE INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	-40°C to +85°C	74LVC652 D	74LVC652 D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC652 DB	74LVC652 DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC652 PW	4LVC652PW DH	SOT355-1

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PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	CP _{AB}	'A' to 'B' clock input (LOW-to-HIGH, edge-triggered)
2	S _{AB}	Select 'A' to 'B' source input
3	OE _{AB}	Output enable B to A input (active LOW)
4, 5, 6, 7, 8, 9, 10, 11	A ₀ to A ₇	'A' data inputs/outputs
12	GND	Ground (0V)
13, 14, 15, 16, 17, 18, 19, 20	B ₀ to B ₇	'B' data inputs/outputs
21	OE _{BA}	Output enable A to B input
22	S _{BA}	Select 'B' to 'A' source input
23	CP _{BA}	'B' to 'A' clock input (LOW-to-HIGH, edge-triggered)
24	V _{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
OE _{AB}	OE _{BA}	CP _{AB}	CP _{BA}	S _{AB}	S _{BA}	A ₀ to A ₇	B ₀ to B ₇	
L	H	H or L	H or L	X	X	input	input	isolation store A and B data
L	H	↑	↑	X	X	input	input	store A, hold B, store A in both registers
X	H	↑	H or L	X	X	input	un *	output
H	H	↑	↑	L	X	input	output	store A in both registers
L	X	H or L	↑	X	X	un *	input	input
L	L	↑	↑	X	L	output	input	hold A, store B, store B in both registers
L	L	X	X	X	L	output	input	real-time B data to A bus stored B data to A bus
L	L	X	H or L	X	H	output	input	real-time B data to A bus stored B data to A bus
H	H	X	X	L	X	input	output	real-time A data to B bus stored A data to B bus
H	H	H or L	X	H	X	input	output	real-time A data to B bus stored A data to B bus
H	L	H or L	H or L	H	H	output	output	stored A data to B bus and stored B data to A bus

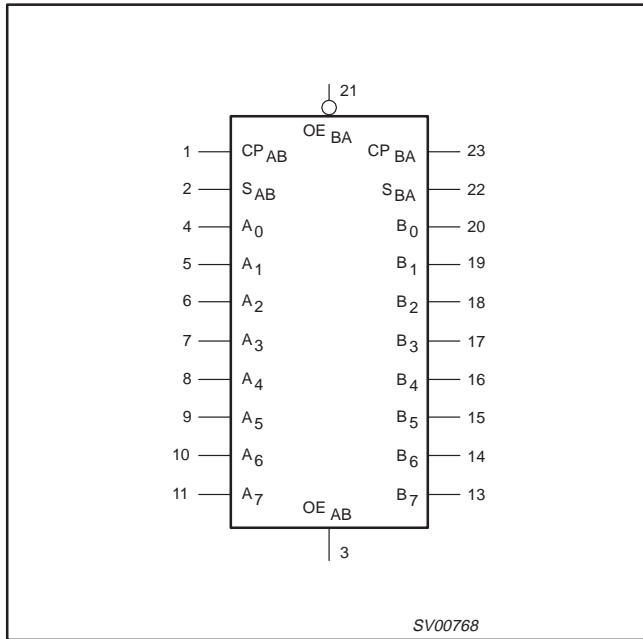
* The data output functions may be enabled or disabled by various signals at the OE_{AB} and OE_{BA} inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

- un = unspecified
- H = HIGH voltage level
- L = LOW voltage level
- X = Don't care
- ↑ = LOW-to-HIGH level transition

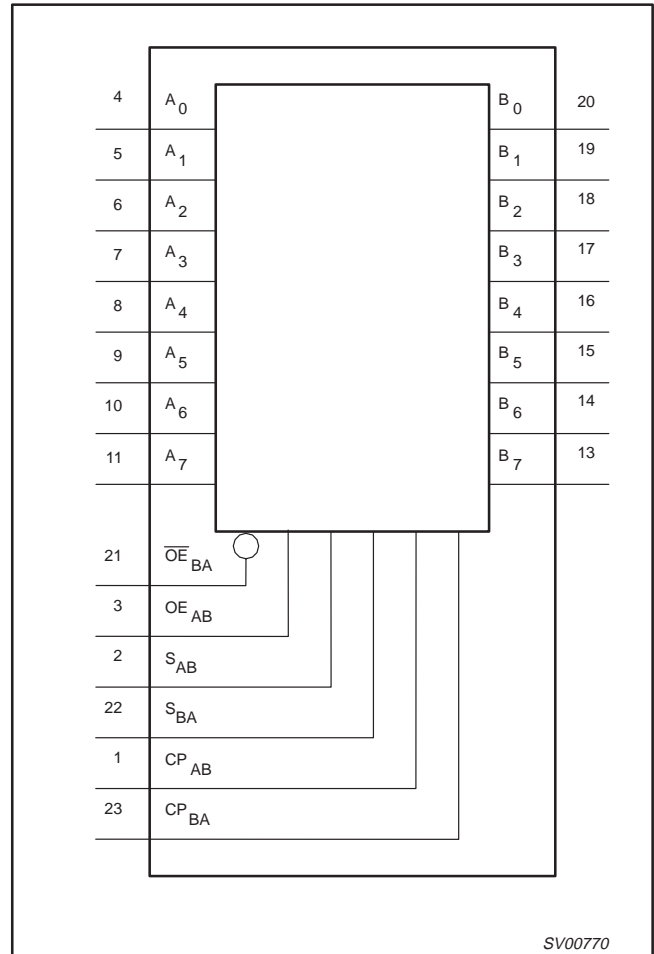
Octal transceiver/register with dual enable (3-State)

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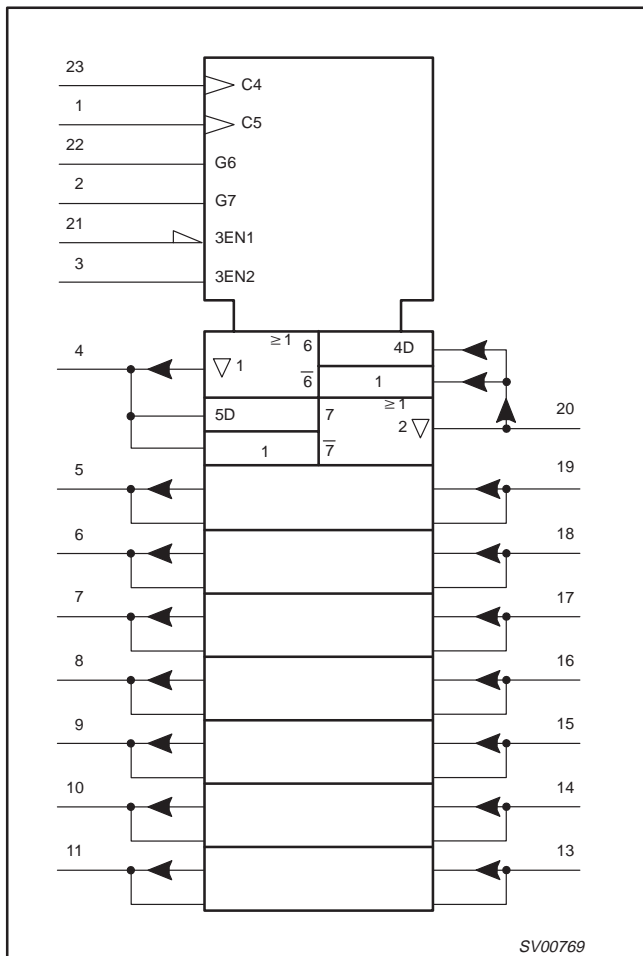
LOGIC SYMBOL



FUNCTIONAL DIAGRAM



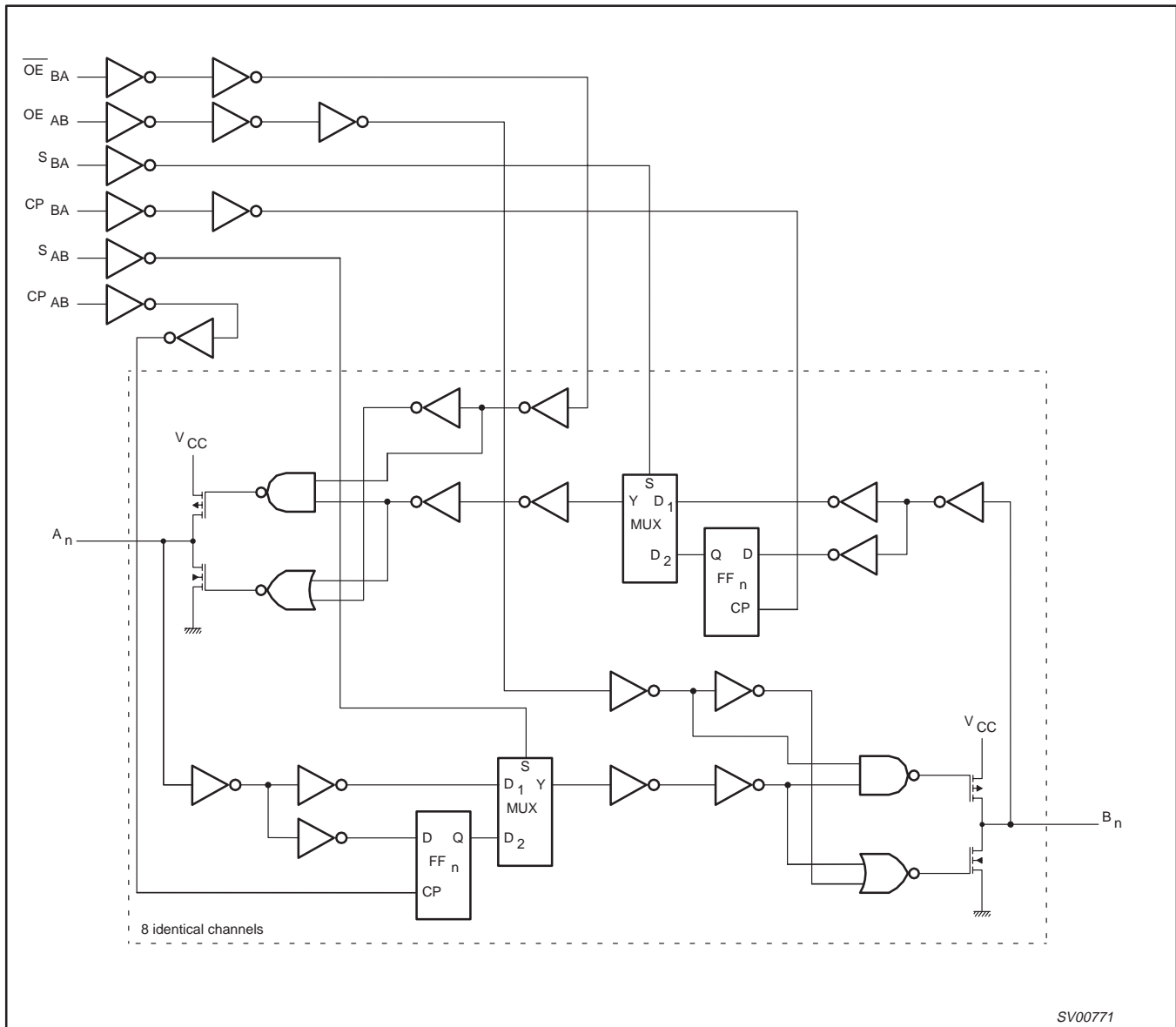
LOGIC SYMBOL (IEEE/IEC)



Octal transceiver/register with dual enable (3-State)

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LOGIC DIAGRAM



Octal transceiver/register with dual enable (3-State)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V _{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
V _I	DC input voltage range		0	5.5	V
V _{I/O}	DC input voltage range for I/Os		0	V _{CC}	V
V _O	DC output voltage range		0	V _{CC}	V
T _{amb}	Operating free-air temperature range		-40	+85	°C
t _p , t _f	Input rise and fall times	V _{CC} = 1.2 to 2.7V V _{CC} = 2.7 to 3.6V	0	20	ns/V
			0	10	

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134)
 Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage	Note 2	-0.5 to +5.5	V
I _{OK}	DC output diode current	V _O > V _{CC} or V _O < 0	± 50	mA
V _{I/O}	DC output voltage; output HIGH or LOW	Note 2	-0.5 to V _{CC} +0.5	V
	DC input voltage; output 3-State	Note 2	-0.5 to V _{CC} +0.5	V
I _O	DC output diode current	V _O = 0 to V _{CC}	± 50	mA
I _{GND} , I _{CC}	DC V _{CC} or GND current		± 100	mA
T _{stg}	Storage temperature range		-65 to +150	°C
P _{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K	500	mW
		above +60°C derate linearly with 5.5 mW/K	500	

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP ¹	MAX	
V _{IH}	HIGH level Input voltage	V _{CC} = 1.2V	V _{CC}			V
		V _{CC} = 2.7 to 3.6V	2.0			
V _{IL}	LOW level Input voltage	V _{CC} = 1.2V			GND	V
		V _{CC} = 2.7 to 3.6V			0.8	
V _{OH}	HIGH level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA	V _{CC} - 0.5			V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100µA	V _{CC} - 0.2	V _{CC}		
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA	V _{CC} - 0.6			
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA	V _{CC} - 0.8			
V _{OL}	LOW level output voltage	V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA			0.40	V
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA		GND	0.20	
		V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA			0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = 5.5V or GND Not for I/O pins		± 0.1	± 5	µA
I _{IHZ} /I _{ILZ}	Input current for common I/O pins	V _{CC} = 3.6V; V _I = 5.5V or GND		± 0.1	± 15	µA
I _{OZ}	3-State output OFF-state current	V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = 5.5V or GND		0.1	± 10	µA
I _{OFF}	Power off leakage current	V _{CC} = 0.0V; V _I = 5.5V; V _O = 5.5V		0.1	± 10	µA
I _{CC}	Quiescent supply current	V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0		0.1	10	µA
ΔI _{CC}	Additional quiescent supply current per input pin	V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0		5	500	µA

NOTES:1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

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AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT	
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		$V_{CC} = 1.2V$		
			MIN	TYP ¹	MAX	MIN	MAX	MIN		TYP
t_{PHL}/t_{PLH}	Propagation delay An to Bn, Bn to An	Figures 1, 5	1.5	4.6	7.9	1.5	9.2	1.5	24	ns
t_{PHL}/t_{PLH}	Propagation delay CP _{AB} , CP _{BA} to B _n , A _n	Figures 2, 5	1.5	5.2	8.9	1.5	11	1.5	26	ns
t_{PHL}/t_{PLH}	Propagation delay S _{AB} , S _{BA} to B _n , A _n	Figures 3, 5	1.5	5.2	8.8	1.5	11	1.5	27	ns
t_{PZH}/t_{PZL}	3-State output enable time OE _{AB} to Bn	Figures 4, 5	1.5	4.8	8.0	1.5	10	1.5	20	ns
t_{PHZ}/t_{PLZ}	3-State output disable time OE _{AB} to Bn	Figures 4, 5	1.5	4.4	8.0	1.5	10	1.5	10	ns
t_{PZH}/t_{PZL}	3-State output enable time OE _{BA} to An	Figures 4, 5	1.5	4.8	8.0	1.5	10	1.5	20	ns
t_{PHZ}/t_{PLZ}	3-State output disable time OE _{BA} to An	Figures 4, 5	1.5	4.4	8.0	1.5	10	1.5	10	ns
t_W	Clock pulse width HIGH or LOW CP _{AB} or CP _{BA}	Figures 4, 5	–	3.0	–	3.0	–	–	–	ns
t_{su}	Set-up time An, Bn to CP _{AB} , CP _{BA}	Figure 2	1.5	0.5	–	1.5	–	–	–	ns
t_h	Hold time An, Bn to CP _{AB} , CP _{BA}	Figure 2	1.0	0	–	1.0	–	–	–	ns
f_{max}	Maximum clock pulse frequency	Figure 2	7.5	150	–	–	–	–	–	MHz

NOTE:

1. These typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.

AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$

$V_M = 0.5V * V_{CC}$ at $V_{CC} < 2.7V$

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

$V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$

$V_X = V_{OL} + 0.1V_{CC}$ at $V_{CC} < 2.7V$

$V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$

$V_Y = V_{OH} - 0.1V_{CC}$ at $V_{CC} < 2.7V$

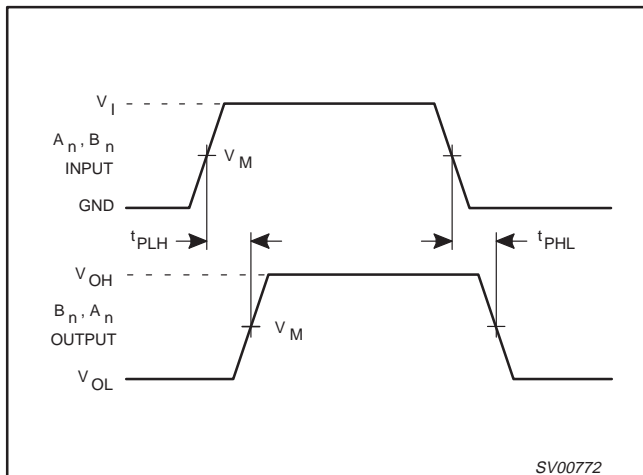


Figure 1. Input An, Bn to output Bn, An propagation delays.

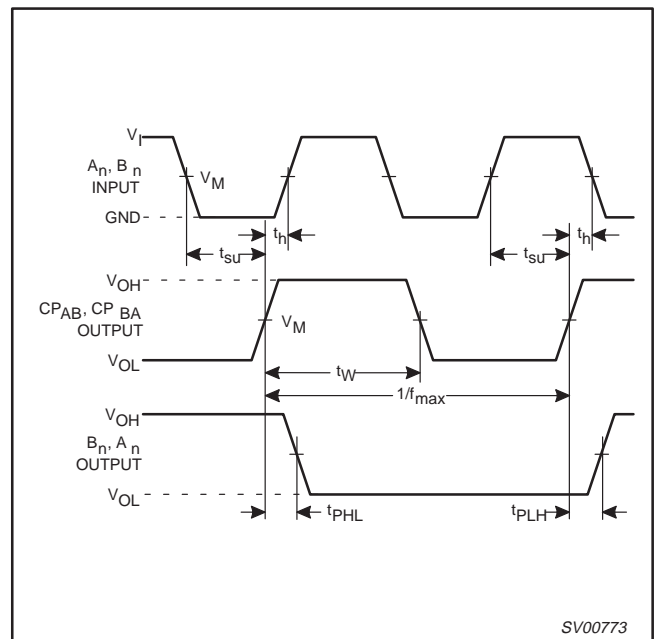


Figure 2. An, Bn to CP_{AB}, CP_{BA} set-up and hold times, clock CP_{AB}, CP_{BA} pulse width, maximum clock pulse frequency and the CP_{AB}, CP_{BA} to output B_n, A_n propagation delays.

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AC WAVEFORMS (Continued)

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$
 $V_M = 0.5V * V_{CC}$ at $V_{CC} < 2.7V$
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$
 $V_X = V_{OL} + 0.1V_{CC}$ at $V_{CC} < 2.7V$
 $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$
 $V_Y = V_{OH} - 0.1V_{CC}$ at $V_{CC} < 2.7V$

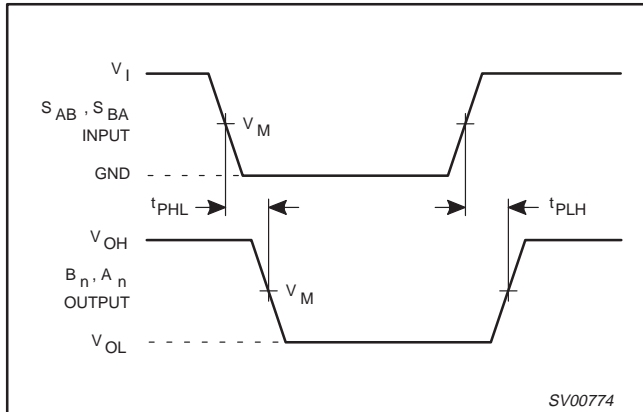


Figure 3. Input S_{AB} , S_{BA} to output B_n , A_n propagation delay times.

TEST CIRCUIT

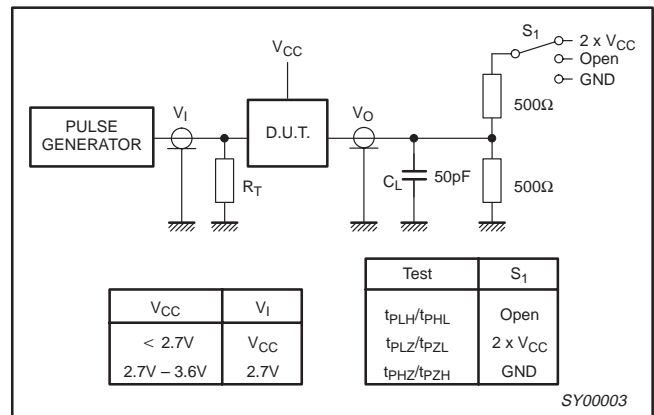


Figure 5. Load circuitry for switching times.

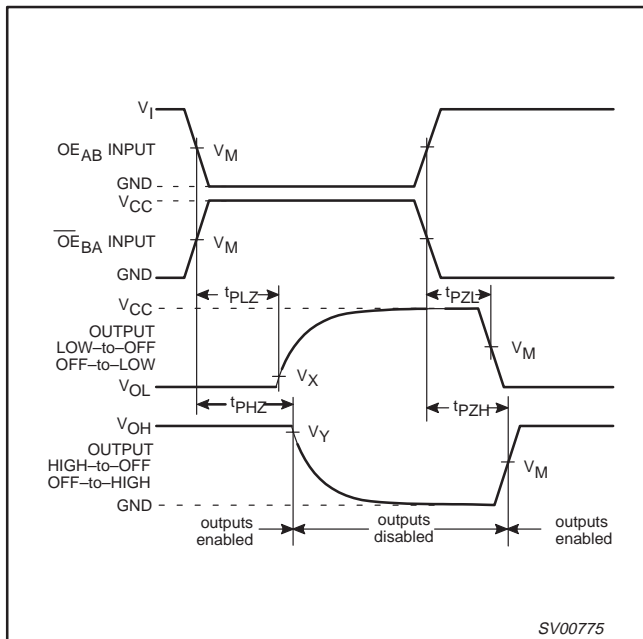


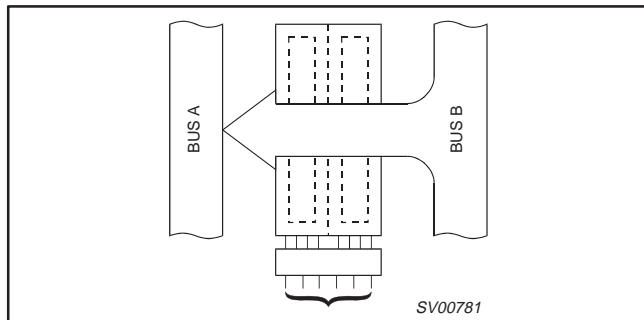
Figure 4. OE inputs (OE_{AB} , \overline{OE}_{BA}) to outputs A_n , B_n enable and disable times.

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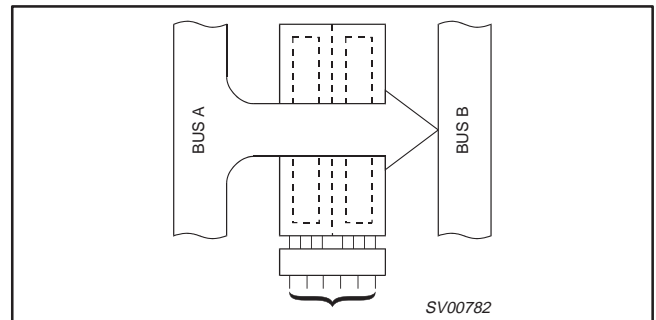
APPLICATION INFORMATION

Real-time transfer; bus B to bus A



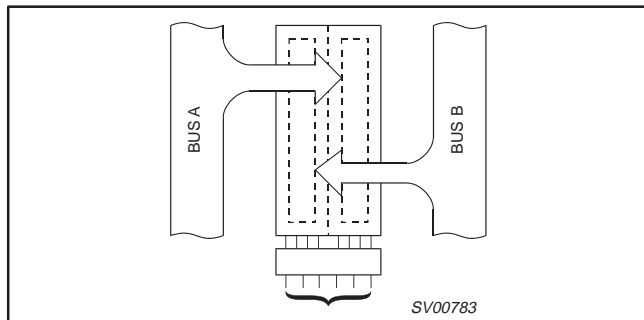
OE _{AB}	$\overline{\text{OE}}_{\text{BA}}$	CP _{AB}	CP _{BA}	S _{AB}	S _{BA}
L	L	X	X	X	L

Real-time transfer; bus A to bus B



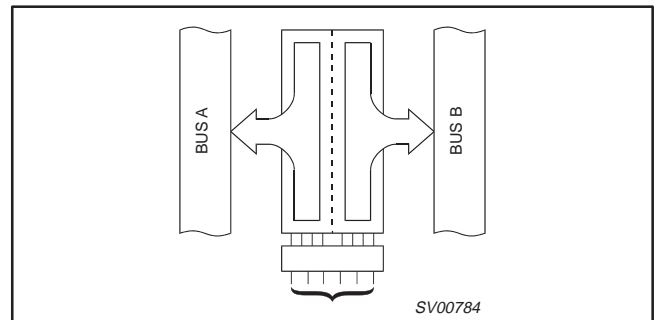
OE _{AB}	$\overline{\text{OE}}_{\text{BA}}$	CP _{AB}	CP _{BA}	S _{AB}	S _{BA}
H	H	X	X	L	X

Store A, B or A and B in one register



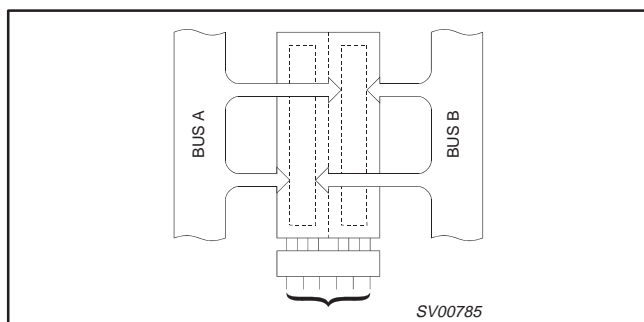
OE _{AB}	$\overline{\text{OE}}_{\text{BA}}$	CP _{AB}	CP _{BA}	S _{AB}	S _{BA}
X	H	↑	↑	L	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

Transfer A stored data to B bus or B stored data to A bus or both at the same time



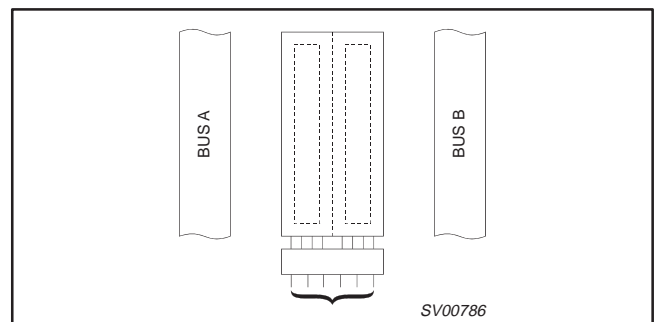
OE _{AB}	$\overline{\text{OE}}_{\text{BA}}$	CP _{AB}	CP _{BA}	S _{AB}	S _{BA}
H	H	H or L	X	H	X
L	L	X	H or L	X	H
H	L	H or L	H or L	H	H

Store bus A in both registers or store bus B in both registers



OE _{AB}	$\overline{\text{OE}}_{\text{BA}}$	CP _{AB}	CP _{BA}	S _{AB}	S _{BA}
H	H	↑	↑	L	X
L	L	↑	↑	X	L

Isolation



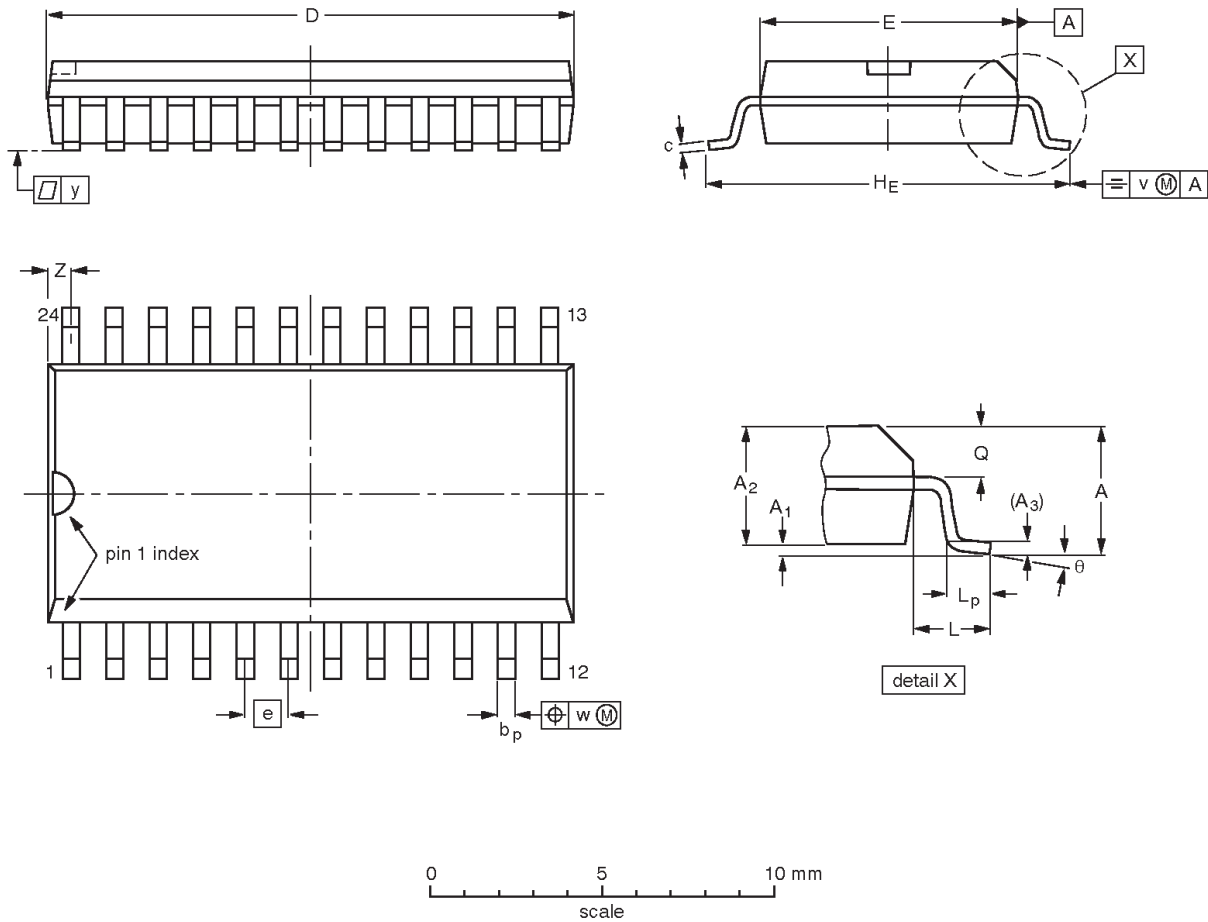
OE _{AB}	$\overline{\text{OE}}_{\text{BA}}$	CP _{AB}	CP _{BA}	S _{AB}	S _{BA}
L	H	H or L	H or L	X	X

Octal transceiver/register with dual enable (3-State)

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

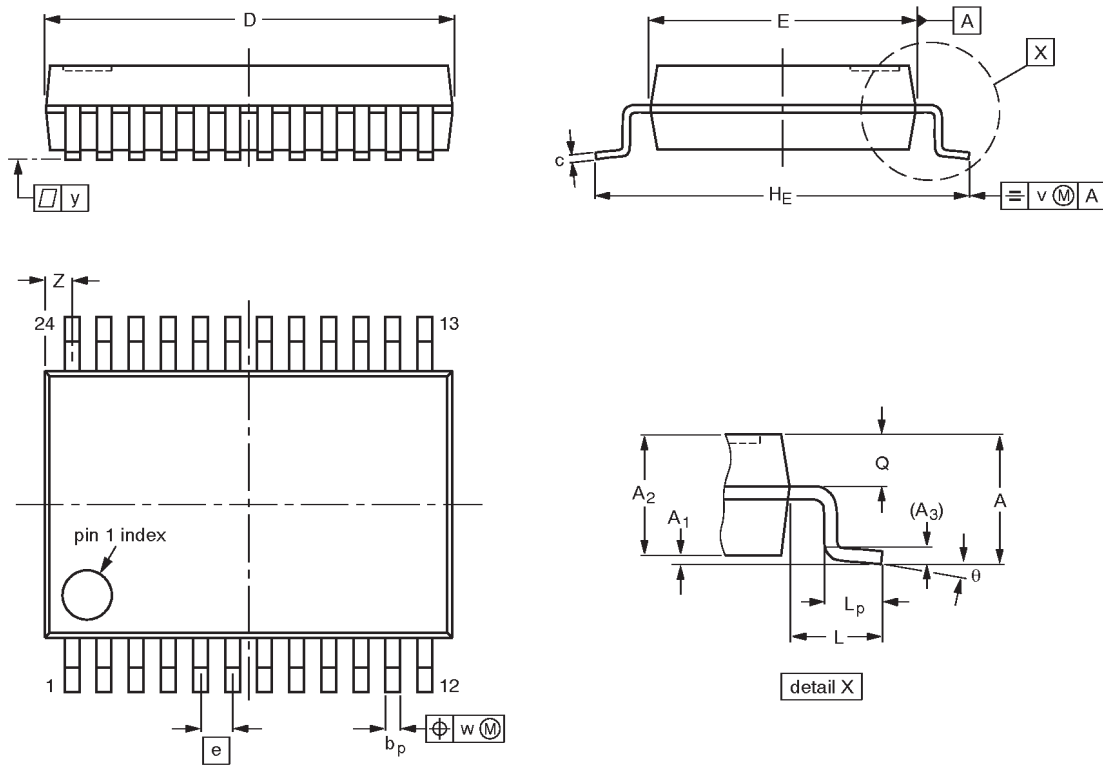
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				95-01-24 97-05-22

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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

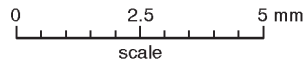
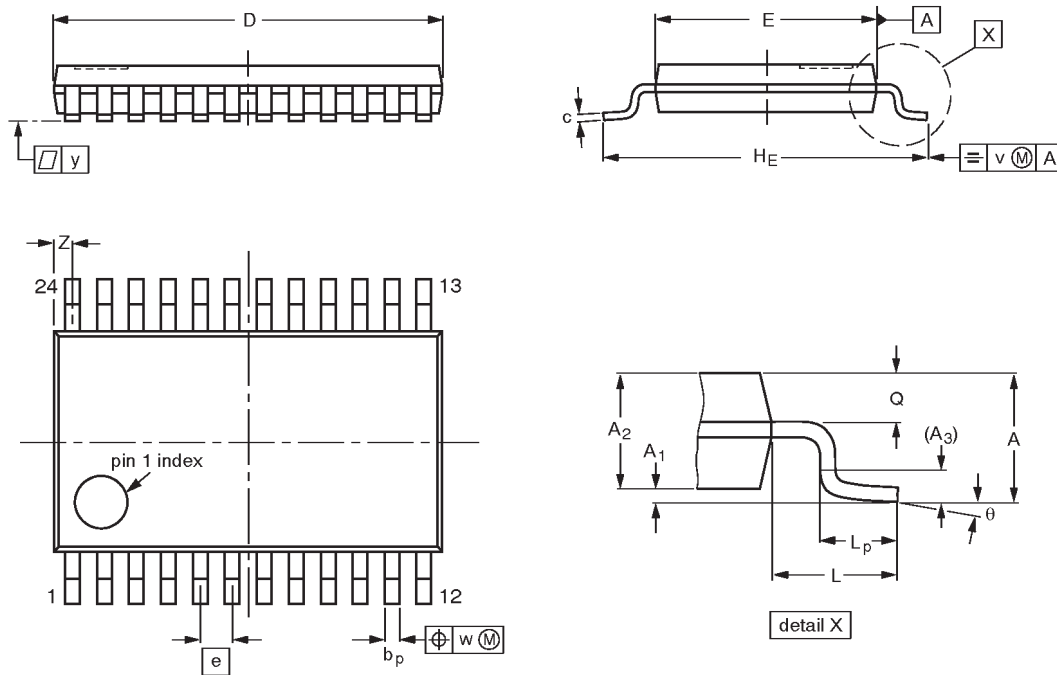
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

Octal transceiver/register with dual enable (3-State)

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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				-93-06-16 95-02-04

Octal transceiver/register with dual enable (3-State)

74LVC652

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 800-234-7381

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