FAIRCHILD SEMICONDUCTOR™

May 2002
Revised May 2002

74ALVCF322835
Low Voltage 36-Bit Universal Bus Driver with 3.6V Tolerant Outputs and 26Ω Series Resistors in Outputs

General Description

The 74ALVCF322835 low voltage 36-bit universal bus driver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes.

Data flow is controlled by output-enable ($\overline{OE}$), latch-enable (LE), and clock (CLK) inputs. The device operates in Transparent Mode when LE is held HIGH. The device operates in clocked mode when LE is LOW and CLK is toggled. Data transfers from the Inputs (I_n) to Outputs (O_n) on a Positive Edge Transition of the Clock. When $\overline{OE}$ is LOW, the output data is enabled. When $\overline{OE}$ is HIGH the output port is in a high impedance state.

The 74ALVCF322835 is designed with 26Ω series resistors in the outputs. This design reduces noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVCF322835 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O capability up to 3.6V.

The 74ALVCF322835 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- Compatible with PC133 DIMM module specifications
- 1.65V to 3.6V V_{CC} specifications provided
- 3.6V tolerant outputs
- 26Ω series resistors in outputs
- t_{PD} (CLK to O_n)
  - 3.7 ns max for 3.0V to 3.6V V_{CC}
  - 4.6 ns max for 2.3V to 2.7V V_{CC}
  - 7.4 ns max for 1.65V to 1.95V V_{CC}
- Power-down high impedance outputs
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model >200V

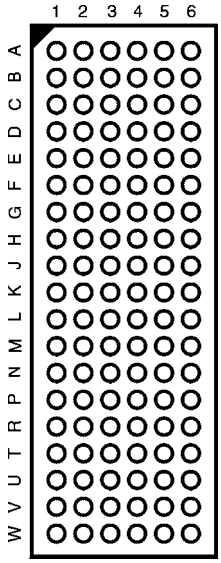
Ordering Code:

Order Number	Package Number	Package Description
74ALVCF322835G (Note 1) (Note 2)	BGA114A	114-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

Note 1: Ordering Code "G" indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



(Top Thru View)

FBGA Pin Assignments

	1	2	3	4	5	6
A	$1O_2$	$1O_1$	NC	NC	$1I_1$	$1I_2$
B	$1O_4$	$1O_3$	NC	GND	$1I_3$	$1I_4$
C	$1O_6$	$1O_5$	GND	GND	$1I_5$	$1I_6$
D	$1O_8$	$1O_7$	V_{CC}	V_{CC}	$1I_7$	$1I_8$
E	$1O_{10}$	$1O_9$	GND	GND	$1I_9$	$1I_{10}$
F	$1I_{12}$	$1O_{11}$	GND	GND	$1I_{11}$	$1I_{12}$
G	$1O_{14}$	$1O_{13}$	V_{CC}	V_{CC}	$1I_{13}$	$1I_{14}$
H	$1O_{15}$	$1O_{16}$	GND	GND	$1I_{16}$	$1I_{15}$
J	$1O_{17}$	$1O_{18}$	$\overline{OE}_1$	CLK_1	$1I_{18}$	$1I_{17}$
K	NC	NC	LE_1	GND	NC	NC
L	$2O_2$	$2O_1$	NC	GND	$2I_1$	$2I_2$
M	$2O_4$	$2O_3$	GND	GND	$2I_3$	$2I_4$
N	$2O_6$	$2O_5$	V_{CC}	V_{CC}	$2I_5$	$2I_6$
P	$2O_8$	$2O_7$	GND	GND	$2O_7$	$2I_8$
R	$2O_{10}$	$2O_9$	GND	GND	$2I_9$	$2I_{10}$
T	$2O_{12}$	$2O_{11}$	V_{CC}	V_{CC}	$2I_{11}$	$2I_{12}$
U	$2O_{14}$	$2O_{13}$	GND	GND	$2I_{13}$	$2I_{14}$
V	$2O_{15}$	$2O_{16}$	$\overline{OE}_2$	CLK_2	$2I_{16}$	$2I_{15}$
W	$2O_{17}$	$2O_{18}$	LE_2	GND	$2I_{18}$	$2I_{17}$

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
LE_n	Latch Enable Input
CLK_n	Clock Input
$1I_1$ - $1I_{18}$	Data Inputs
$2I_1$ - $2I_{18}$	Data Inputs
$1O_1$ - $1O_{18}$	3-STATE Outputs
$2O_1$ - $2O_{18}$	3-STATE Outputs

Truth Table

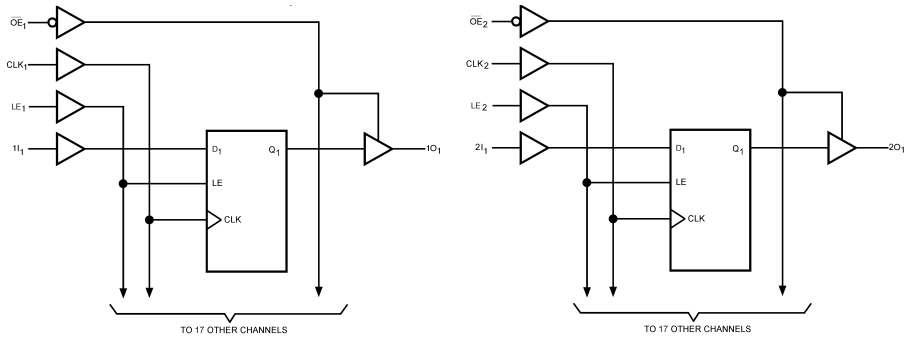
Inputs				Outputs
$\overline{OE}_n$	LE_n	CLK_n	I_n	O_n
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	O_0 (Note 3)
L	L	L	X	O_0 (Note 4)

H = Logic HIGH
L = Logic LOW
X = Don't Care, but not floating
Z = High Impedance
↑ = LOW-to-HIGH Clock Transition

Note 3: Output level before the indicated steady-state input conditions were established provided that CLK was HIGH before LE went LOW.

Note 4: Output level before the indicated steady-state input conditions were established.

Logic Diagram



Absolute Maximum Ratings(Note 5)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to 4.6V
Output Voltage (V_O) (Note 6)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK})	
V_I < 0V	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 7)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

Note 5: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

Note 7: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95	0.65 x V_{CC}		V
			2.3 - 2.7	1.7		
			2.7 - 3.6	2.0		
V_{IL}	LOW Level Input Voltage		1.65 - 1.95		0.35 x V_{CC}	V
			2.3 - 2.7		0.7	
			2.7 - 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	1.65 - 3.6	V_{CC} - 0.2		V
		I_{OH} = −2 mA	1.65	1.2		
		I_{OH} = −4 mA	2.3	1.9		
		I_{OH} = −6 mA	2.3	1.7		
			3.0	2.4		
		I_{OH} = −8 mA	2.7	2		
		I_{OH} = −12 mA	3.0	2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	1.65 - 3.6		0.2	V
		I_{OL} = 2 mA	1.65		0.45	
		I_{OL} = 4 mA	2.3		0.4	
		I_{OL} = 6 mA	2.3		0.55	
			3.0		0.55	
		I_{OL} = 8 mA	2.7		0.6	
		I_{OL} = 12 mA	3.0		0.8	
I_{OH}	High Level Output Current		1.65		−2	mA
			2.3		−6	
			2.7		−8	
			3.0		−12	
I_{OL}	Low Level Output Current		1.65		2	mA
			2.3		6	
			2.7		8	
			3.0		12	
I_I	Input Leakage Current	0 ≤ V_I ≤ 3.6V	1.65 - 3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	0 ≤ V_O ≤ 3.6V, V_I = V_{IH} or V_{IL}	1.65 - 3.6		±10	µA
I_{OFF}	Power Off Leakage Current	0V ≤ (V_I, V_O) ≤ 3.6V	0		10	mA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND, I_O = 0	3.6		40	µA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} − 0.6V	2.7 - 3.6		750	µA

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$								Units
		$C_L = 50$ pF				$C_L = 30$ pF				
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5 \pm 0.2V$		$V_{CC} = 1.8V \pm 0.15V$		
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	250		200		200		100		MHz
t_{PHL}, t_{PLH}	Propagation Delay Bus-to-Bus	1.1	3.6	1.3	4.5	0.8	4.0	1.5	7.2	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Bus	1.5	3.7	2.0	4.6	1.5	4.1	2.0	7.4	ns
t_{PHL}, t_{PLH}	Propagation Delay LE to Bus	1.1	4.2	1.3	5.2	0.8	4.7	1.5	8.5	ns
t_{PZL}, t_{PZH}	Output Enable Time	1.1	4.8	1.3	6.4	0.8	5.9	1.5	9.8	ns
t_{PLZ}, t_{PHZ}	Output Disable Time	1.1	4.7	1.3	5.2	0.8	4.7	1.5	7.9	ns
t_S	Setup Time	1.5		1.5		1.5		2.5		ns
t_H	Hold Time	0.7		0.7		0.7		1.0		ns
t_W	Pulse Width	1.5		1.5		1.5		4.0		ns

Capacitance

Symbol	Parameter		Conditions	$T_A = +25°C$		Units
				V_{CC}	Typical	
C_{IN}	Input Capacitance		$V_I = 0V$ or V_{CC}	3.3	3.5	pF
C_{OUT}	Output Capacitance		$V_I = 0V$ or V_{CC}	3.3	5.5	pF
C_{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, $C_L = 0$ pF	3.3	13	pF
				2.5	13	

I_{OUT} - V_{OUT} Characteristics

I_{OH} versus V_{OH}

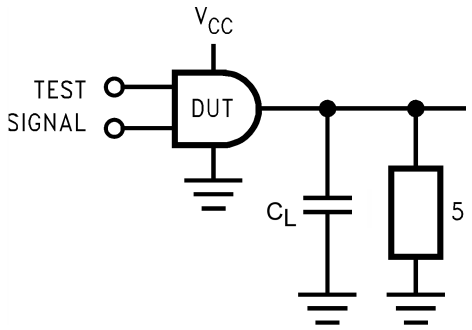


FIGURE 1. Characteristics for Output - Pull Up Drive

I_{OL} versus V_{OL}

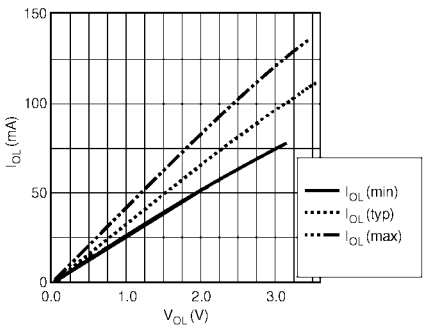


FIGURE 2. Characteristics for Output - Pull Down Driver

AC Loading and Waveforms

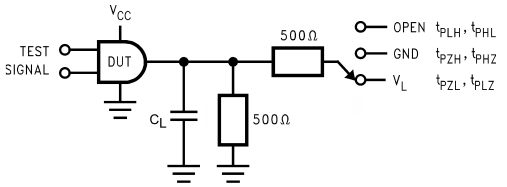


FIGURE 3. AC Test Circuit

Table 1: Values for Figure 1

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_L
t_{PZH}, t_{PHZ}	GND

Table 2: Variable Matrix
(Input Characteristics: f = 1MHz; $t_r = t_f$ = 2ns; $Z_0 = 50\Omega$)

Symbol	V_{CC}			
	3.3V ± 0.3V	**2.7V**	**2.5V ± 0.2V**	**1.8V ± 0.15V**
V_{mi}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3V	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} − 0.3V	V_{OH} − 0.3V	V_{OH} − 0.15V	V_{OH} − 0.15V
V_L	6V	6V	V_{CC}*2	V_{CC}*2

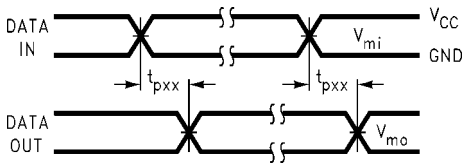


FIGURE 4. Waveform for Inverting and Non-inverting Functions

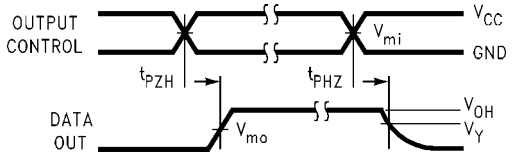


FIGURE 5. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

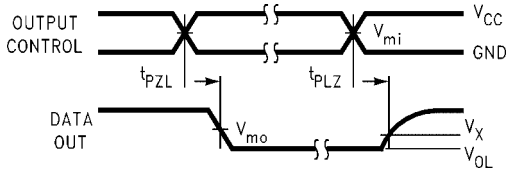
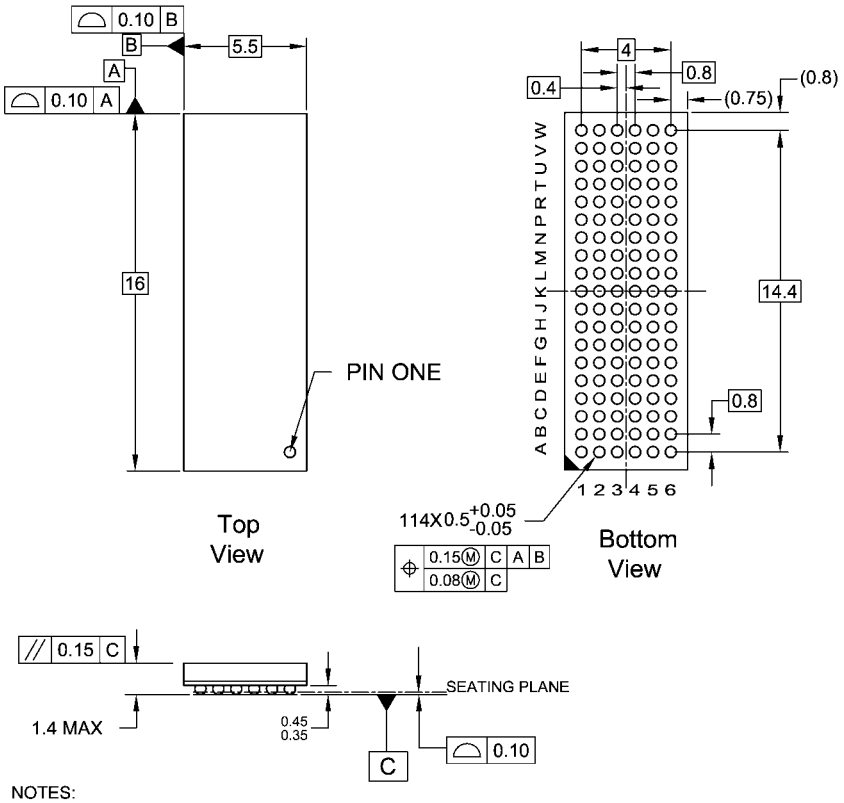


FIGURE 6. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA114ArevE

56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com