

- Member of the Texas Instruments *Widebus*™ Family
- EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Power Off Disables Outputs, Permitting Live Insertion
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Packaged in Plastic Fine-Pitch Ball Grid Array Package

**description**

This 32-bit edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCH32374A is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74LVCH32374A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

**FUNCTION TABLE**  
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



# SN74LVCH32374A

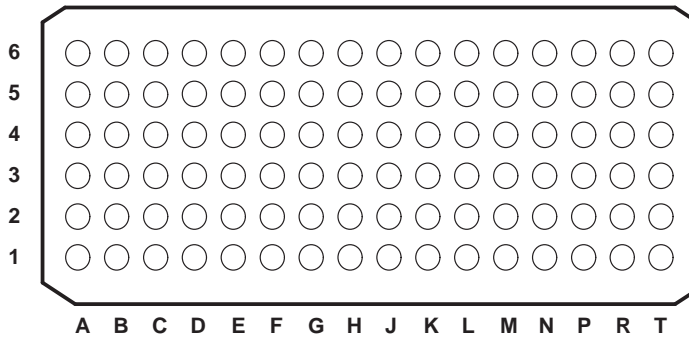
## 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP

### WITH 3-STATE OUTPUTS

SCAS619A – OCTOBER 1998 – REVISED JUNE 1999

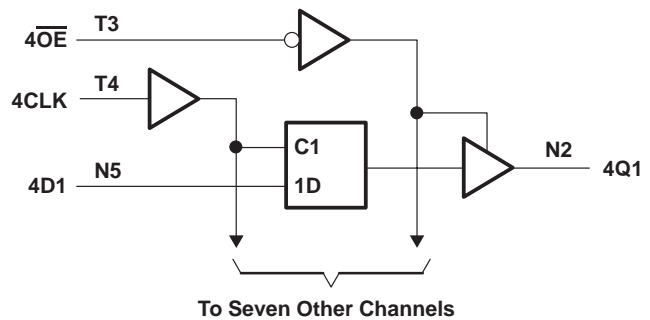
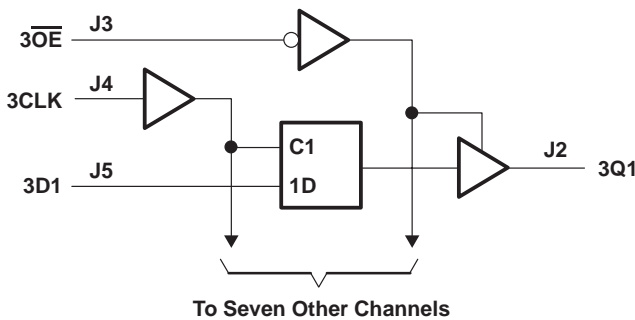
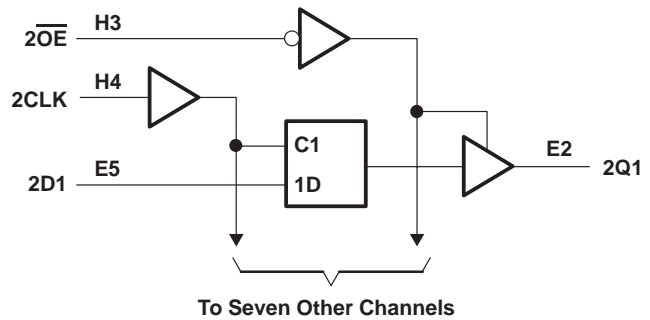
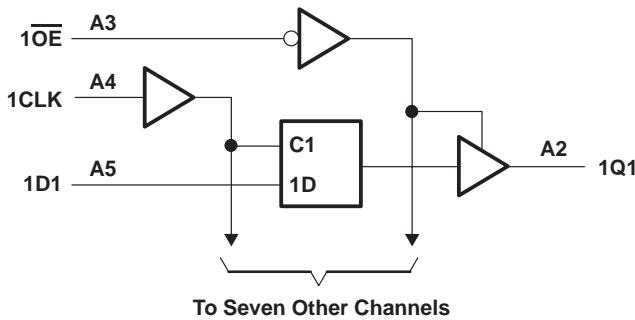
#### terminal assignments

GKE PACKAGE  
(TOP VIEW)



6	1D2	1D4	1D6	1D8	2D2	2D4	2D6	2D7	3D2	3D4	3D6	3D8	4D2	4D4	4D6	4D7
5	1D1	1D3	1D5	1D7	2D1	2D3	2D5	2D8	3D1	3D3	3D5	3D7	4D1	4D3	4D5	4D8
4	1CLK	GND	VCC	GND	GND	VCC	GND	2CLK	3CLK	GND	VCC	GND	GND	VCC	GND	4CLK
3	1OE	GND	VCC	GND	GND	VCC	GND	2OE	3OE	GND	VCC	GND	GND	VCC	GND	4OE
2	1Q1	1Q3	1Q5	1Q7	2Q1	2Q3	2Q5	2Q8	3Q1	3Q3	3Q5	3Q7	4Q1	4Q3	4Q5	4Q8
1	1Q2	1Q4	1Q6	1Q8	2Q2	2Q4	2Q6	2Q7	3Q2	3Q4	3Q6	3Q8	4Q2	4Q4	4Q6	4Q7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

#### logic diagram (positive logic)



# SN74LVCH32374A 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS619A – OCTOBER 1998 – REVISED JUNE 1999

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Continuous output current, $I_O$ .....	±50 mA
Continuous current through each $V_{CC}$ or GND .....	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) .....	40°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.  
 3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3$ V to 2.7 V	1.7		
		$V_{CC} = 2.7$ V to 3.6 V	2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3$ V to 2.7 V	0.7		
		$V_{CC} = 2.7$ V to 3.6 V	0.8		
$V_I$	Input voltage	0	5.5	V	
$V_O$	Output voltage	High or low state	0	$V_{CC}$	V
		3 state	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 1.65$ V	–4		mA
		$V_{CC} = 2.3$ V	–8		
		$V_{CC} = 2.7$ V	–12		
		$V_{CC} = 3$ V	–24		
$I_{OL}$	Low-level output current	$V_{CC} = 1.65$ V	4		mA
		$V_{CC} = 2.3$ V	8		
		$V_{CC} = 2.7$ V	12		
		$V_{CC} = 3$ V	24		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V	
$T_A$	Operating free-air temperature	–40	85	°C	

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# SN74LVCH32374A

## 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS619A – OCTOBER 1998 – REVISED JUNE 1999

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -4 mA	1.65 V	1.2			
	I <sub>OH</sub> = -8 mA	2.3 V	1.7			
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			
	I <sub>OH</sub> = -24 mA	3 V	2.4			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 8 mA	2.3 V			0.7	
	I <sub>OL</sub> = 12 mA	2.7 V			0.4	
	I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5	μA
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V	25			μA
	V <sub>I</sub> = 1.07 V		-25			
	V <sub>I</sub> = 0.7 V	2.3 V	45			
	V <sub>I</sub> = 1.7 V		-45			
	V <sub>I</sub> = 0.8 V	3 V	75			
	V <sub>I</sub> = 2 V		-75			
	V <sub>I</sub> = 0 to 3.6 V‡	3.6 V			±500	
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μA
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V	3.6 V			±10	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	I <sub>O</sub> = 0		20	μA
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V§				20	
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			5	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V			6.5	pF

† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This applies in the disabled state only.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)**

		V <sub>CC</sub> = 1.8 V ±0.15 V		V <sub>CC</sub> = 2.5 V ±0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ±0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		¶		¶	150		150		MHz
t <sub>w</sub>	Pulse duration, CLK high or low		¶		¶	3.3		3.3		ns
t <sub>su</sub>	Setup time, data before CLK↑		¶		¶	1.9		1.9		ns
t <sub>h</sub>	Hold time, data after CLK↑		¶		¶	1.1		1.1		ns

¶ This information was not available at the time of publication.



**SN74LVCH32374A**  
**32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP**  
**WITH 3-STATE OUTPUTS**

SCAS619A – OCTOBER 1998 – REVISED JUNE 1999

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			†		†		150		150		MHz
t <sub>pd</sub>	CLK	Q	†	†	†	†	4.9		1.5	4.5	ns
t <sub>en</sub>	$\overline{OE}$	Q	†	†	†	†	5.3		1.5	4.6	ns
t <sub>dis</sub>	$\overline{OE}$	Q	†	†	†	†	6.1		1.5	5.5	ns
t <sub>sk(o)</sub> †									1.5		ns

† This information was not available at the time of publication.

‡ Skew between any two outputs of the same package switching in the same direction

**operating characteristics, T<sub>A</sub> = 25°C**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance per flip-flop	f = 10 MHz	†	†	58	pF
	Outputs enabled		†	†	24	
	Outputs disabled					

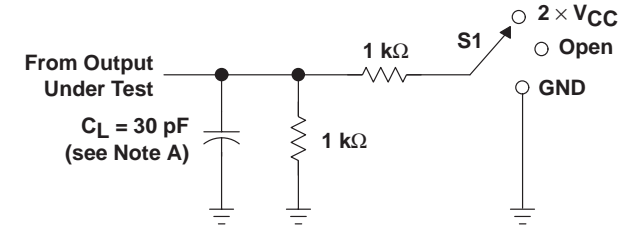
† This information was not available at the time of publication.

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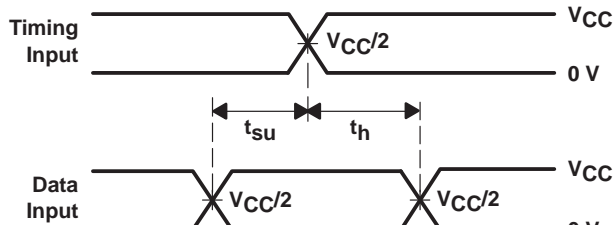
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$

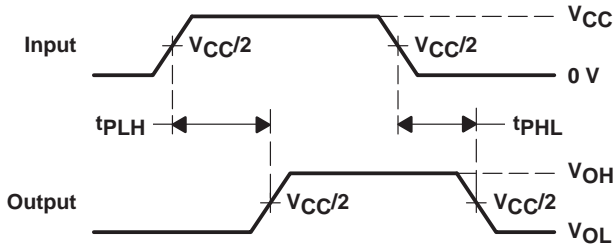


**LOAD CIRCUIT**

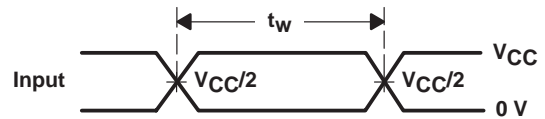
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



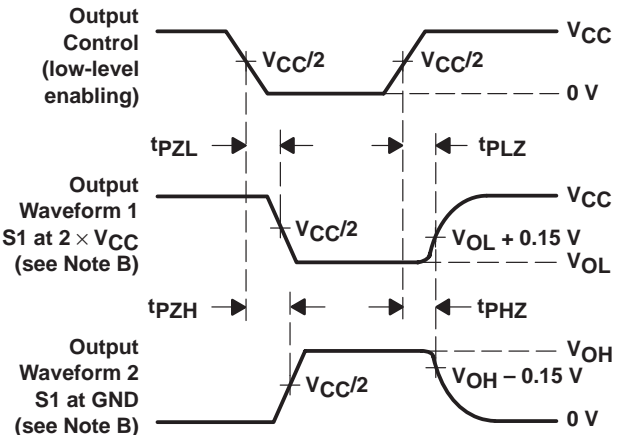
**VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
 PULSE DURATION**



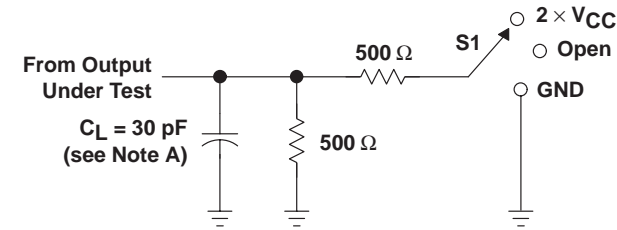
**VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES**

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

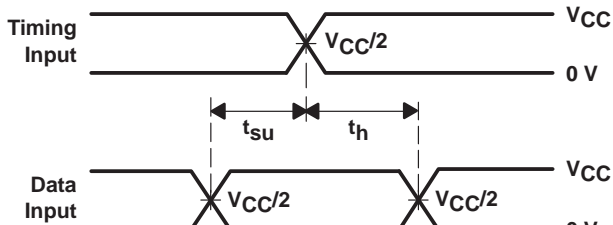
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

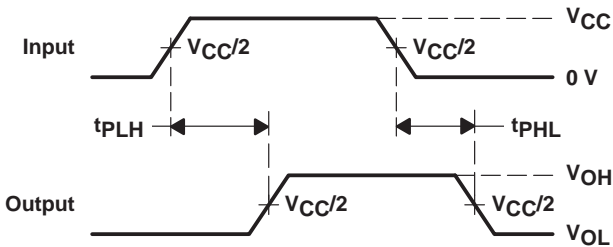


LOAD CIRCUIT

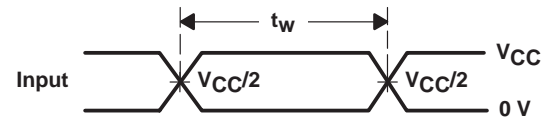
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	2 $\times$ $V_{CC}$
$t_{PHZ}/t_{PZH}$	GND



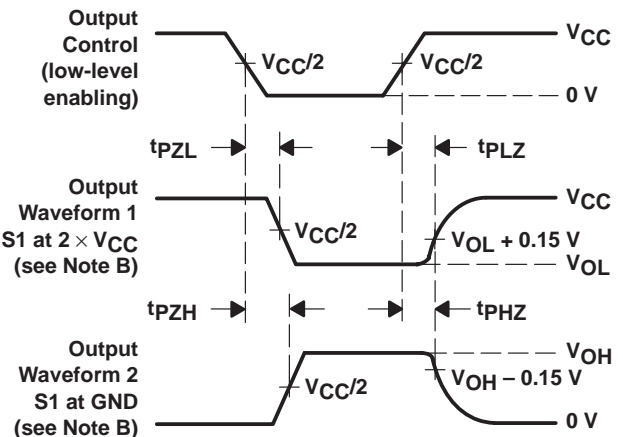
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

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C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

# SN74LVCH32374A

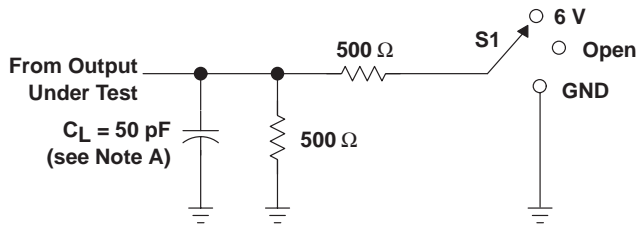
## 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP

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SCAS619A – OCTOBER 1998 – REVISED JUNE 1999

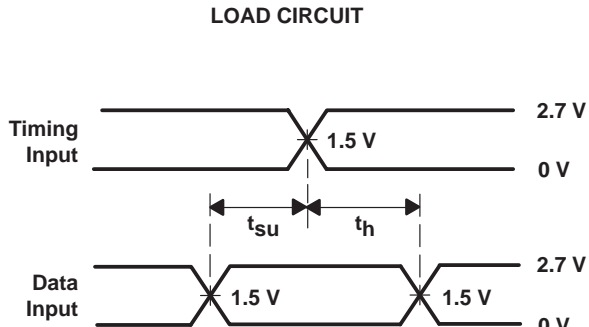
#### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

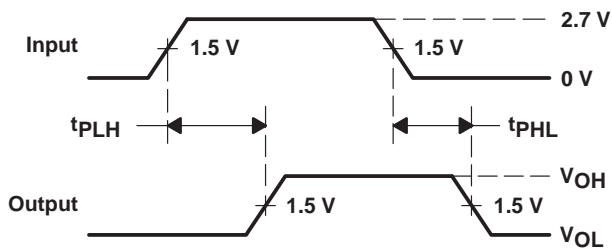


LOAD CIRCUIT

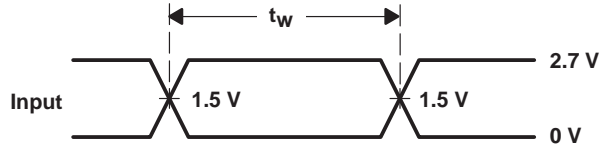
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



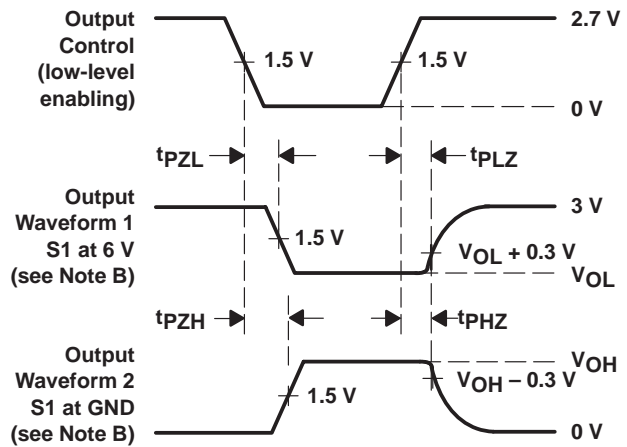
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
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VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
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  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Load Circuit and Voltage Waveforms



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