

SN65LVCP22

SLLS553 – NOVEMBER 2002

2x2 1000 Mbps LVDS CROSSPOINT SWITCH

FEATURES

- High Speed (>1000 Mbps) Upgrade for DS90CP22 2x2 LVDS Crosspoint Switch
- LVPECL Crosspoint Switch Available in SN65LVCP23
- Low-Jitter 1000-Mbps Fully Differential Data Path
- 20 ps (Typ), 50 ps (Max), of Peak-to-Peak Jitter With PRBS = 2²³–1 Pattern at 1000 Mbps
- Less Than 200 mW (Typ), 280 mW (Max) Total Power Dissipation
- Balanced Output Impedance
- Output (Channel-to-Channel) Skew Is 10 ps (Typ), 20 ps (Max)
- Configurable as 2:1 Mux, 1:2 Demux, Repeater or 1:2 Signal Splitter
- Inputs Accept LVDS, LVPECL, and CML Signals
- Fast Switch Time of 1.2 ns (Typ), 1.5 ns (Max)
- Fast Propagation Delay of 0.65 ns (Typ), 0.8 ns (Max)
- Receiver Input Threshold < ±50 mV
- 16 Lead SOIC and TSSOP Packages
- Inter-Operates With TIA/EIA–644–A LVDS Standard
- Operating Temperature: –40°C to 85°C

APPLICATIONS

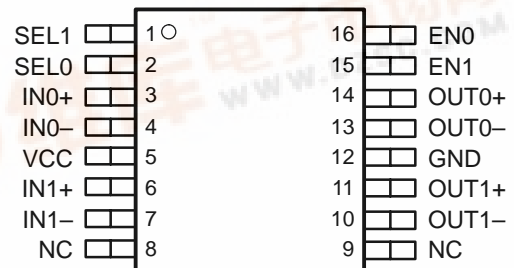
- Base stations
- Add/Drop Muxes
- Protection Switching for Serial Backplanes
- Network Switches/Routers
- Optical Networking Line Cards/Switches
- Clock Distribution

DESCRIPTION

The SN65LVCP22 is a 2x2 crosspoint switch providing greater than 1000 Mbps operation for each path. The dual channels incorporate wide common-mode (0 V to 4 V) receivers, allowing for the receipt of LVDS, LVPECL, and CML signals. The dual outputs are LVDS drivers to provide low-power, low-EMI, high-speed operation. The SN65LVCP22 provides a single device supporting 2:2 buffering (repeating), 1:2 splitting, 2:1 multiplexing, 2x2 switching, and LVPECL/CML to LVDS level translation on each channel. The flexible operation of the SN65LVCP22 provides a single device to support the redundant serial bus transmission needs (working and protection switching cards) of fault-tolerant switch systems found in optical networking, wireless infrastructure, and data communications systems. TI offers additional gigabit repeater/translator and crosspoint products in the SN65LVDS100 and SN65LVDS122.

The SN65LVCP22 uses a fully differential data path to ensure low-noise generation, fast switching times, low pulse width distortion, and low jitter. Output jitter is less than 20 ps (typ), and 50 ps (max), to provide an eye that is at least 95 % open at 1000 Mbps. Output channel-to-channel skew is less than 10 ps (typ) and 20 ps (max) to ensure accurate alignment of outputs in all applications. Both SOIC and TSSOP package options are available to allow easy upgrade for existing solutions, and board area savings where space is critical.

**D or PW PACKAGE
(TOP VIEW)**



NC – No internal connection

PRODUCT PREVIEW



SN65LVCP22

SLLS553 – NOVEMBER 2002



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PACKAGE DESIGNATOR	PART NUMBER(1)	SYMBOLIZATION
SOIC	SN65LVCP22D	TBD
TSSOP	SN65LVCP22PW	TBD

(1) Add the syffix R for taped and reeled carrier

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
SOIC (D)	950 mW	7.5 mW/ $^\circ\text{C}$	494 mW
TSSOP (PW)	774 mW	6.2 mW/ $^\circ\text{C}$	402 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

FUNCTION TABLE

SEL0	SEL1	OUT0	OUT1	FUNCTION
0	0	IN0	IN0	1:2 Splitter
0	1	IN0	IN1	Repeater
1	0	IN1	IN0	Switch
1	1	IN1	IN1	1:2 Splitter

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

INPUT AND OUTPUT SCHEMATICS TO BE INCLUDED AFTER DESIGN IS FINALIZED

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

			UNITS
Supply voltage ⁽²⁾ range, V_{CC}			–0.5 V to 4 V
CMOS/TTL input voltage (ENO, EN1, SEL0, SEL1)			–0.5 V to 4 V
LVDS receiver input voltage (IN+, IN–)			–0.7 V to 4.3 V
LVDS driver output voltage (OUT+, OUT–)			–0.5 V to 4 V
LVDS output short circuit current			Continuous
Junction temperature			150°C
Storage temperature range			–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C
Continuous power dissipation			See Dissipation Rating Table
Electrostatic discharge	Human body model ⁽³⁾	IN+, IN–, OUT+, OUT–, and GND	±8 kV
		All pins	±2 kV
	Charged-device mode ⁽⁴⁾	All pins	±500 V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminals.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Receiver input voltage	0		4	V
Operating free-air temperature, T_A	–40		85	°C
Magnitude of differential input voltage $ V_{ID} $	0.05		3	V

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
CMOS/TTL DC SPECIFICATIONS (EN0, EN1, SEL0, SEL1)					
V_{IH} High-level input voltage		2		V_{CC}	V
V_{IL} Low-level input voltage		GND		0.8	V
I_{IH} High-level input current	$V_{IN} = 3.6\text{ V or }2.0\text{ V}, V_{CC} = 3.6\text{ V}$		± 7	± 20	μA
I_{IL} Low-level input current	$V_{IN} = 0.0\text{ V or }0.8\text{ V}, V_{CC} = 3.6\text{ V}$		± 1	± 10	μA
V_{CL} Input clamp voltage	$I_{CL} = -18\text{ mA}$		-0.8	-1.5	V
LVDS OUTPUT SPECIFICATIONS (OUT0, OUT1)					
$ V_{OD} $ Differential output voltage	$R_L = 75\ \Omega$, See Figure 2	270	365	475	mV
	$R_L = 75\ \Omega, V_{CC} = 3.3\text{ V}, T_A = 25^\circ\text{C}$, See Figure 2	285	365	440	
$ \Delta V_{OD} $ Change in differential output voltage magnitude between logic states	$V_{ID} = \pm 100\text{ mV}$, See Figure 2	-25		25	mV
V_{OS} Steady-state offset voltage	Figure 3	1	1.2	1.45	V
ΔV_{OS} Change in steady-state offset voltage between logic states	Figure 3	-25		25	mV
$V_{OC(PP)}$ Peak-to-peak common-mode output voltage	Figure 3		50	150	mV
I_{OZ} High-impedance output current	$V_{OUT} = \text{GND or } V_{CC}$			± 1	μA
I_{OFF} Power-off leakage current	$V_{CC} = 0\text{ V}, 1.5\text{ V}; V_{OUT} = 3.6\text{ V or GND}$			± 1	μA
I_{OS} Output short-circuit current	V_{OUT+} or $V_{OUT-} = 0\text{ V}$			-24	mA
I_{OSB} Both outputs short-circuit current	V_{OUT+} and $V_{OUT-} = 0\text{ V}$	-12		12	mA
C_O Differential output capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5\text{ V}$				pF
LVDS RECEIVER DC SPECIFICATIONS (IN0, IN1)					
V_{TH} Positive-going differential input voltage threshold	See Figure 1 and Table 1			50	mV
V_{TL} Negative-going differential input voltage threshold	See Figure 1 and Table 1	-50			mV
$V_{ID(HYS)}$ Differential input voltage hysteresis					mV
V_{CMR} Common-mode voltage range	$V_{ID} = 100\text{ mV}, V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0.05		3.95	V
I_{IN} Input current	$V_{IN} = 4\text{ V}, V_{CC} = 3.6\text{ V or }0.0$		± 1	± 10	mA
	$V_{IN} = 0\text{ V}, V_{CC} = 3.6\text{ V or }0.0$		± 1	± 10	
C_{IN} Differential input capacitance	$V_I = 0.4 \sin(4E6\pi t) + 0.5\text{ V}$		3		pF
SUPPLY CURRENT					
I_{CCD} Total supply current	$R_L = 75\ \Omega, C_L = 5\text{ pF}, 500\text{ MHz}$ (1000 Mbps), EN0=EN1=High		60	85	mA
I_{CCZ} 3-state supply current	EN0 = EN1 = Low		25	40	mA

(1) All typical values are at 25°C and with a 3.3 V supply.

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T _{SET}	Input to Sel setup time	Figure 7	0.7	0.5		ns
T _{HOLD}	Input to Sel hold time	Figure 7	1.0	0.5		ns
T _{SWITCH}	SEL to switched output	Figure 7		1.2	1.5	ns
t _{PHZ}	Disable time, high-level-to-high-impedance	Figure 6		2	4.0	ns
t _{PLZ}	Disable time, low-level-to-high-impedance	Figure 6		2	4.0	ns
t _{PZH}	Enable time, high-impedance -to-high-level output	Figure 6		2	6.0	ns
t _{PZL}	Enable time, high-impedance-to-low-level output	Figure 6		2	6.0	ns
t _{LHT}	Differential output signal rise time (20%–80%)	C _L = 5 pF, Figure 5	200		450	ps
t _{HLT}	Differential output signal fall time (20%–80%)	C _L = 5 pF, Figure 5	200		450	ps
t _{JIT}	LVDS data path peak-to-peak jitter	V _{ID} = 300 mV, 50% duty cycle, V _{CM} = 1.2 V at 1000 Mbps (500 MHz), C _L = 5 pF		10	30	ps
		V _{ID} = 300 mV, PRBS = 2 ²³ –1 data pattern, V _{CM} = 1.2 V at 1000 Mbps, C _L = 5 pF		20	50	ps
T _{Jrms}	Added random jitter (rms)	V _{ID} = 300 mV, 50% duty cycle, V _{CM} = 1.2 V at 1000 Mbps, C _L = 5 pF		0.5	1	ps _{RMS}
t _{PLHD}	Propagation delay time, low-to-high-level output	V _{CC} = 3.3 V, T _A = 25°C, C _L = 5 pF, See Figure 5		650	800	ps
		C _L = 5 pF, Figure 5	550	650	800	
t _{PHLD}	Propagation delay time, high-to-low-level output	V _{CC} = 3.3 V, T _A = 25°C, C _L = 5 pF, See Figure 5	550	650	800	ps
		C _L = 5 pF, Figure 5	550	650	800	ps
t _{skew}	Pulse skew (t _{PLHD} – t _{PHLD}) ⁽¹⁾	C _L = 5 pF, Figure 5	550	0	20	ps
t _{CCS}	Output channel-to-channel skew {want this to cover splitter mode, repeater, and switch modes.}	C _L = 5 pF, Figure 5		10	20	ps
t _{sk(pp)}	Part-to-part skew ⁽²⁾	V _{CMR} : 0.05 to 3.95 V			250	ps
		V _{CMR} : 0.50 to 3.95 V			100	

(1) t_{skew} is the magnitude of the time difference between the t_{PLHD} and t_{PHLD} of any output of a single device.

(2) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

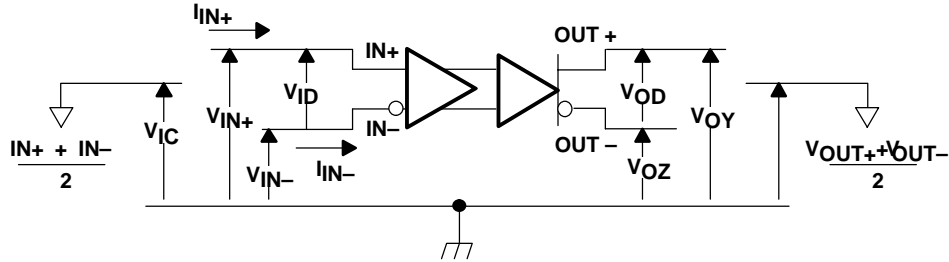


Figure 1. Voltage and Current Definitions

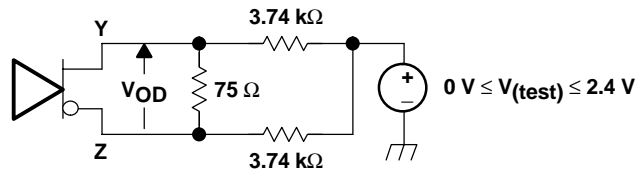
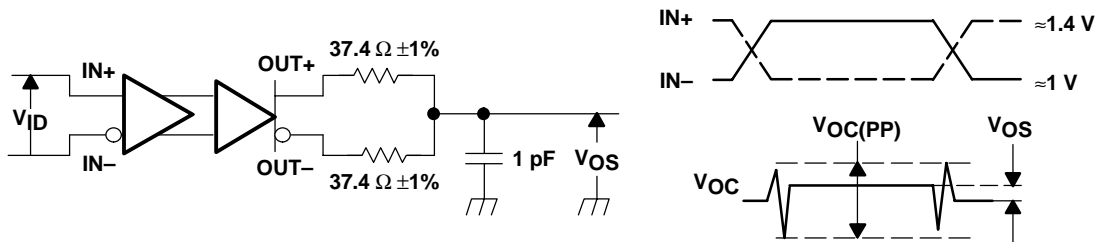
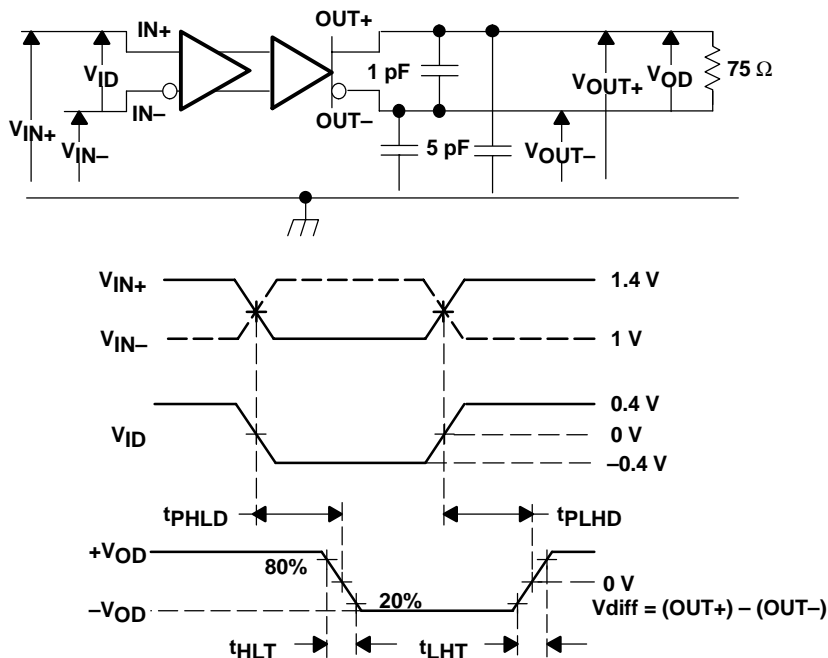


Figure 2. Differential Output Voltage (V_{OD}) Test Circuit



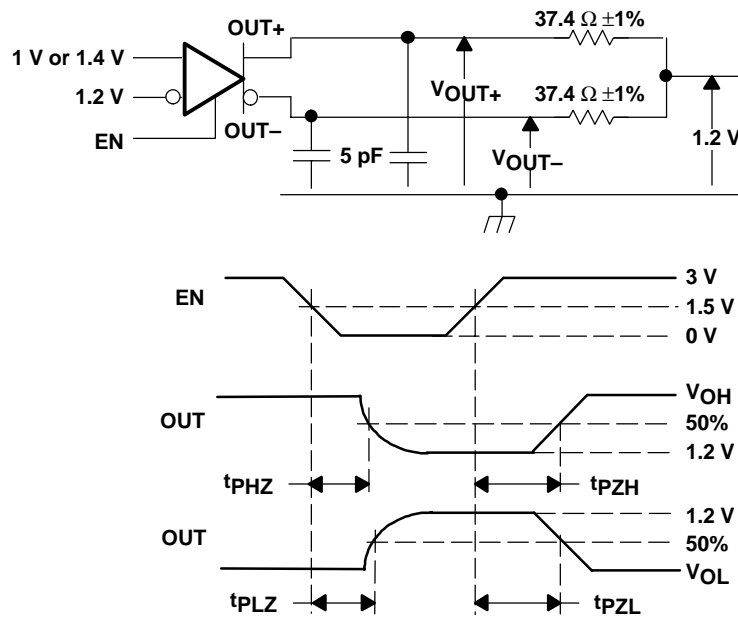
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns; $R_L = 100 \Omega$; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



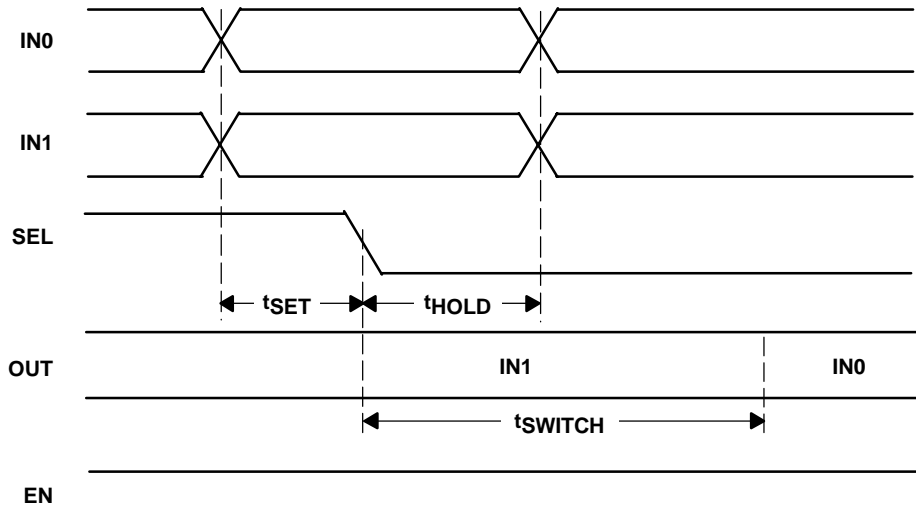
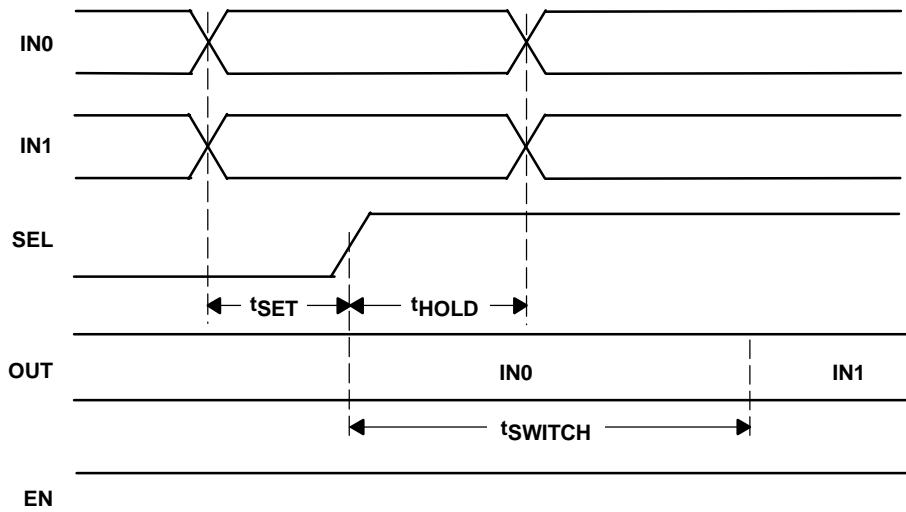
NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq .25$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Timing Test Circuit and Waveforms



NOTE: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse-repetition rate (PRR) = 0.5 Mpps, Pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions



NOTE: t_{SET} and t_{HOLD} times specify that data must be in a stable state before and after mux control switches.

Figure 6. Input to Select for Both Rising and Falling Edge Setup and Hold Times

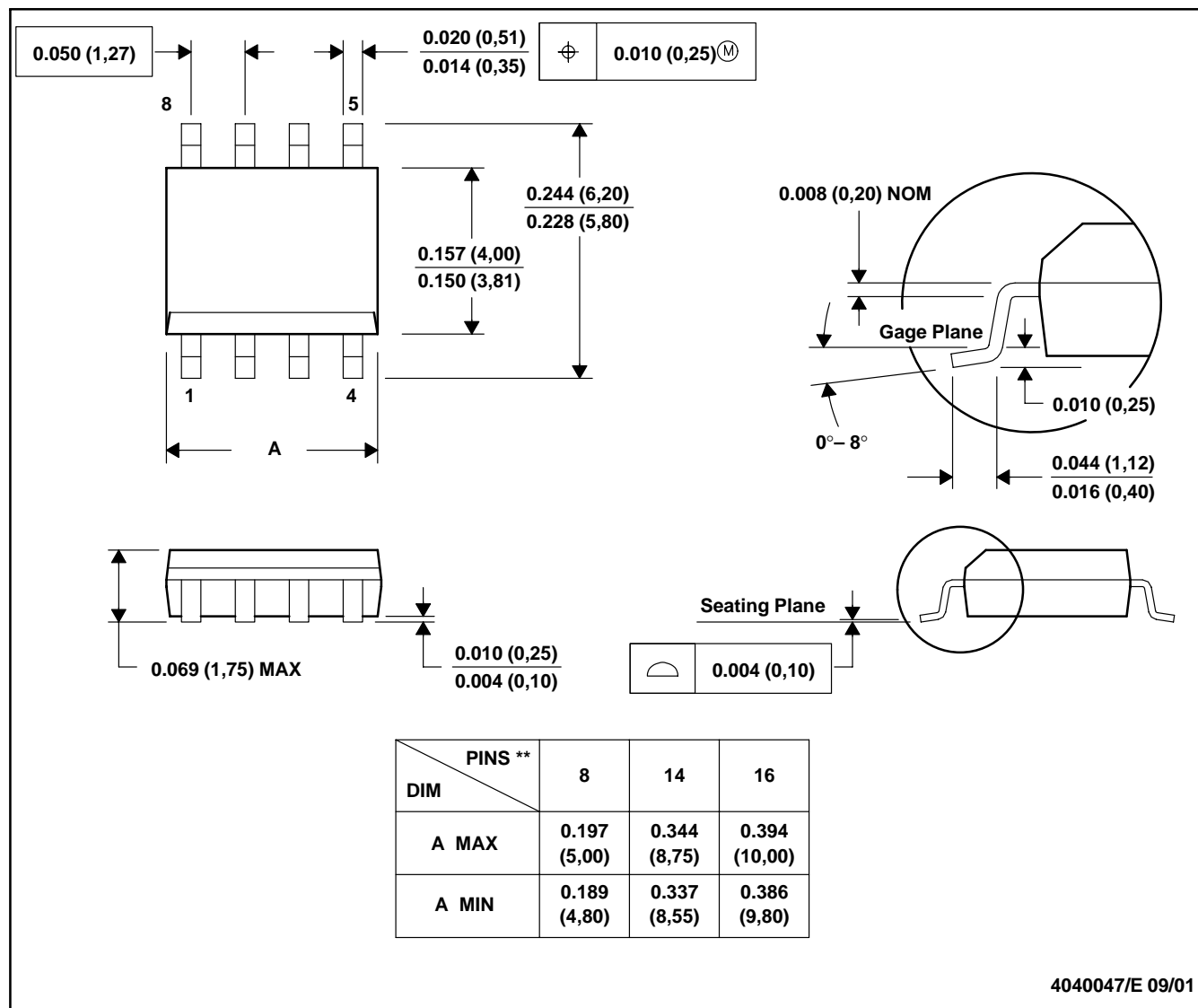
MECHANICAL DATA

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012

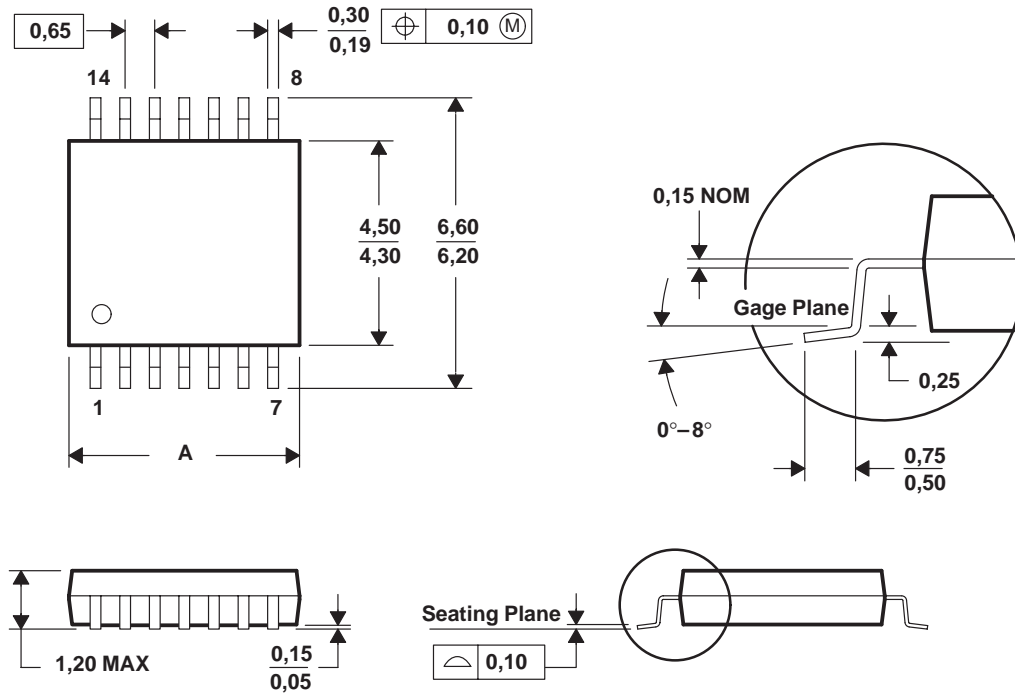
MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265