

February 1999 Revised July 2000

74VCX16722 Low Voltage 22-Bit Register with 3.6V Tolerant Inputs and Outputs

General Description

The VCX16722 low voltage 22-bit register contains twenty-two non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The design has been optimized for use with JEDEC compliant 200 pin DIMM modules.

The 74VCX16722 is designed for low voltage (1.65V to 3.6V) $\rm V_{CC}$ applications with I/O capability up to 3.6V.

The 74VCX16722 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V-3.6V V_{CC} specifications provided
- 3.6V tolerant inputs and outputs
- t_{PD} (CLK to O_n)
 3.6ns max for 3.0V to 3.6V V_{CC}
 4.6ns max for 2.3V to 2.7V V_{CC}
 9.2ns max for 1.65V to 1.95V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Meets JEDEC registered module specifications
- Static Drive (I_{OH}/I_{OL}) ±24mA @ 3.0V ±18mA @ 2.3V ±6mA @ 1.65V
- Latchup performance exceeds 300 mA
- ESD performance:

Human body model > 2000V

Machine model >200V

Note 1: To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74VCX16722MTD	MTD64	64-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code

Connection Diagram

ÖĒ - 1 64 - CLK Oo - 2 63 - D₀ O₁ - 3 62 - D₁ GND- 4 61 - GND O₂ - 5 60 - D₂ O₃ - 6 59 - D₃ Vcc - 7 58 - Vcc O₄ - 8 57 - D₄ O₅ - 9 56 - D₅ O₅ - 10 55 - D₆ GND- 11 54 - GND Oγ - 12 53 - Dγ O₀ - 15 50 - D₁ O₀ - 15 50 - D₁ O₁ - 16 49 - D₁ O₁ - 17 48 - D₁ GND - 18 47 - GND O₁ - 21 17 - 48 - D₁ GND - 18 47 - GND O₁ - 21 21 - 44 - D₁ Vcc - 22 43 - Vcc O₁ - 24 41 - D₁ O₁ - 25 40 - GND O₁ - 25 40 - GND O₁ - 26 20 - 39 - D₁ O₁ - 27 24 - D₁ O₁ - 26 39 - D₁ O₁ - 27 24 - D₁ O₁ - 27 24 - D₁ O₁				
O₁ - 3	ŌĒ -	1	64	-CLK
GND- 4 61 - GND O2- 5 60 - D2 O3- 6 59 - D3 VCC- 7 58 - VCC O4- 8 57 - D4 O5- 9 56 - D5 GND- 11 54 - GND O7- 12 53 - D7 O6- 13 52 - D8 O8- 14 51 - D9 O10- 15 50 - D10 O1- 16 49 - D11 GND- 18 47 - GND O13- 19 46 - D13 O13- 19 46 - D13 O13- 19 46 - D13 O14- 20 45 - D14 O15- 21 44 - D15 VCC- 22 43 - VCC O16- 23 42 - D16 O17- 24 41 - D17 GND- 25 40 - GND O18- 26 39 - D18 O19- 27 38 - D18 O19- 27 38 - D18 O19- 31 34 - GND GND- 31 34 - GND	O ₀ –	2	63	$-D_0$
O₂ - 5	0, -	3	62	D₁
O3 = 6			61	
O₃ = 6	O ₂ –	5	60	- D ₂
VCC - 7 58 - VCC O4 - 8 57 - D4 O5 - 9 56 - D5 O6 - 10 55 - D6 GND - 11 54 - GND O ₅ - 12 53 - D ₇ O ₈ - 13 52 - D ₈ O ₉ - 14 51 - D ₉ O ₁₀ - 15 50 - D ₁₀ O ₁ - 16 49 - D ₁₁ O ₁ - 16 49 - D ₁₁ O ₁ - 17 48 - D ₁₂ GND - 18 47 - GND O ₁ - 20 45 - D ₁₄ O ₁₅ - 21 44 - D ₁₅ O ₁₅ - 21 44 - D ₁₅ O ₁₅ - 21 44 - D ₁₅ O ₁₅ - 21 44 - D ₁₇ GND - 25 40 - GND O ₁₅ - 24 41 - D ₁₇ GND - 25 40 - GND O ₁₈ - 26 39 - D ₁₈ O ₁₉ - 27 38	O ₃ –	6	59	
O4− 8 57 − D4 O5− 9 56 D5 O8− 10 55 − D6 GND− 11 54 − GND O7− 12 53 − D7 O8− 13 52 − D8 O8− 14 51 − D9 O10− 15 50 − D10 O1− 16 49 − D11 CND− 18 47 − GND O1− 20 45 − D14 O1− 21 44 − D15 VCC − 22 43 − VCC O1− 23 42 − D16 O1− 25 40 − GND O1− 26 39 − D18 O1− 27 38 − D18 VCC − 28 37 − VCC O2− 29 36 − D20 O2− 29 36 − D20 O2− 29 36 − D20 O2− 30 − D20 O3− D10 OND − 31 34 − GND	V _{CC} -	7	58	
O ₆ - 10 55 - D ₆ GND- 11 54 - GND O ₇ - 12 53 - D ₇ O ₈ - 13 52 - D ₈ O ₉ - 14 51 - D ₉ O ₁₀ - 15 50 - D ₁₁ O ₁₂ - 17 48 - D ₁₂ GND- 18 47 - GND O ₁₃ - 19 46 - D ₁₃ O ₁₄ - 20 45 - D ₁₄ O ₁₅ - 21 44 - D ₁₅ VCC- 22 43 - VCC O ₁₆ - 23 42 - D ₁₆ O ₁₇ - 24 41 - D ₁₇ GND- 25 40 - GND O ₁₈ - 26 39 - D ₁₈ O ₁₉ - 27 38 - D ₁₉ VCC- 28 37 - VCC O ₂₀ - 29 36 - D ₂₀ O ₂₁ - 30 35 - D ₂₁ GND- 31 34 - GND		8	57	
O ₆ - 10 55 - D ₆ GND- 11 54 - GND O ₇ - 12 53 - D ₇ O ₈ - 13 52 - D ₈ O ₉ - 14 51 - D ₉ O ₁₀ - 15 50 - D ₁₀ O ₁₁ - 16 49 - D ₁₁ O ₁₂ - 17 48 - D ₁₂ GND- 18 47 - GND O ₁₃ - 19 46 - D ₁₃ O ₁₄ - 20 45 - D ₁₄ O ₁₅ - 21 44 - D ₁₅ VCC- 22 43 - VCC O ₁₇ - 24 41 - D ₁₇ GND- 25 40 - GND O ₁₇ - 24 41 - D ₁₇ GND- 25 40 - GND O ₁₈ - 26 39 - D ₁₈ O ₁₇ - 27 38 - D ₁₉ VCC- 28 37 - VCC O ₂₀ - 29 36 - D ₂₀ O ₂₁ - 30 35 - D ₂₁ GND- 31 34 - GND		9	56	D₅
GND— 11 54 — GND O7— 12 53 — D7 O8— 13 52 — D8 O8— 14 51 — D9 O10— 15 50 — D10 O11— 16 49 — D11 O13— 17 48 — D12 GND— 18 47 — GND O13— 19 46 — D13 O13— 21 44 — D15 VCC — 22 43 — VCC O14— 23 42 — D16 O17— 24 41 — D17 GND— 25 40 — GND O18— 26 39 — D18 O19— 27 38 — D18 VCC — 28 37 — VCC O20— 29 36 — D20 O21— 30 35 — D21 GND— 31 34 — GND	O ₆ -	10	55	
O ₈ - 13 52 − D ₈ O ₉ - 14 51 − D ₉ O ₁₀ - 15 50 − D ₁₀ O ₁₁ - 16 49 − D ₁₁ O ₁₂ - 17 48 − D ₁₂ GND− 18 47 − GND O ₁₃ - 19 46 − D ₁₃ O ₁₄ - 20 45 − D ₁₄ O ₁₅ - 21 44 − D ₁₅ VCC− 22 43 − VCC O ₁₆ - 23 42 − D ₁₆ O ₁₇ - 24 41 − D ₁₇ GND− 25 40 − GND O ₁₈ - 26 39 − D ₁₈ O ₁₉ - 27 38 − D ₁₉ VCC− 28 37 − VCC O ₂₀ - 29 36 − D ₂₀ O ₂₁ - 30 35 − D ₂₁ GND− 31 34 − GND	GND-	11	54	
0		12	53	- D ₇
0	O ₈ -	13	52	− D ₈
O ₁₀ 15 50 - D ₁₀ O ₁₁ 16 49 - D ₁₁ O ₁₂ 17 48 - D ₁₂ GND - 18 47 - GND O ₁₃ - 19 46 - D ₁₃ O ₁₄ - 20 45 - D ₁₄ O ₁₅ - 21 44 - D ₁₅ VCC - 22 43 - VCC O ₁₆ - 23 42 - D ₁₆ O ₁₇ - 24 41 - D ₁₇ GND - 25 40 - GND O ₁₈ - 26 39 - D ₁₈ O ₁₉ - 27 38 - D ₁₉ VCC - 28 37 - VCC O ₂₀ - 29 36 - D ₂₀ O ₂₁ 30 35 - D ₂₁ GND - 31 34 - GND	O ₉	14	51	- D ₉
O ₁₁ 16 49 - D ₁₁ O ₁₂ 17 48 - D ₁₂ GND- 18 47 - GND O ₁₃ 19 46 - D ₁₃ O ₁₄ 20 45 - D ₁₄ O ₁₅ 21 44 - D ₁₅ VCC- 22 43 - VCC O ₁₆ 23 42 - D ₁₆ O ₁₇ 24 41 - D ₁₇ GND- 25 40 - GND O ₁₈ 26 39 - D ₁₈ O ₁₉ 27 38 - D ₁₉ VCC- 28 37 - VCC O ₂₀ 29 36 - D ₂₀ O ₂₁ 30 35 - D ₂₁ GND 31 34 - GND	O ₁₀ -	15	50	- D ₁₀
O₁₂ 17 48 − D₁₂ GND− 18 47 − GND O₁₃ 19 46 − D₁₃ O₁₃ − 20 45 − D₁₃ Vcc − 22 43 − Vcc O₁₅ − 23 42 − D₁₅ O₁¬ 24 41 − D₁¬ CN¬ 24 41 − D₁¬ CN¬ 26 39 − D₁¬ CN¬ 27 38 − D₁¬ Vcc − 28 37 − Vcc O₂₀ 29 36 − D₂₀ C₁¬ 31 34 − GND	0,,-	16	49	- D ₁
GND - 18	O ₁₂ -	17	48	- D ₁₂
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	GND-	18	47	-GND
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	O ₁₃ -	19	46	- D ₁₃
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	O ₁₄ -	20	45	- D ₁₄
VCC	O ₁₅ -	21	44	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Vcc-	22	43	⊸∨cc
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	O ₁₆ -	23	42	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	0,,,-			
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	GND-			-GND
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	O ₁₈ -	26		
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	O ₁₉ -	27		- D ₁₉
O_{21} 30 35 - D_{21} GND 31 34 - GND	Vcc-			−Vcc
O_{21} 30 35 - D_{21} GND 31 34 - GND	O ₂₀ -			- D ₂₀
GND - 31 34 - GND	O ₂₁ -			- D ₂₁
NC - 32 33 - CE	GND-			-GND
	NC-	32	33	-CĒ
				•

Pin Descriptions

Pin Names	Description
ŌĒ	Output Enable Input (Active LOW)
CE	Clock Enable Input (Active Low)
CLK	Clock Input
D ₁ - D ₂₁	Data Inputs
O ₁ - O ₂₁	3-STATE Outputs

Truth Table

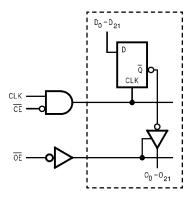
CLK	CE	ŌĒ	D ₀ -D ₂₁	O ₀ -O ₂₁
Χ	Χ	Н	Χ	Z
Χ	Н	L	Х	O ₀
	L	L	L	L
_	L	L	Н	Н
L or H	L	L	Χ	O ₀

- H = HIGH Voltage Level
- L = LOW Level Voltage X = Immaterial (HIGH or LOW, Inputs may not float)
- Z = High Impedance $O_0 = \text{Previous } O_0 \text{ before LOW-to-HIGH transition of Clock}$
- ∠ = LOW-to-HIGH transition

Functional Description

The VCX16722 contains twenty-two D-type flip-flops with 3-STATE standard outputs. The twenty-two flip-flops will store the state of their individual D-type inputs that meet the setup and hold time requirements on the LOW-HIGH Clock (CLK) transition, when the Clock-Enable (CE) is LOW. The 3-STATE standard outputs are controlled by the Output-Enable (OE). When OE is HIGH, the standard outputs are in high impedance mode but this does not interfere with entering new data into the flip-flops.

Logic Diagram



Absolute Maximum Ratings(Note 2)

 $\label{eq:supply Voltage VCC} \begin{tabular}{lll} Supply Voltage (V_{CC}) & -0.5V to +4.6V \\ DC Input Voltage (V_I) & -0.5V to +4.6V \\ \end{tabular}$

Output Voltage (V_O)

Outputs 3-STATE -0.5V to +4.6V Outputs Active (Note 3) -0.5 to $V_{CC} + 0.5$ V DC Input Diode Current (I_{IK}) $V_I < 0$ V -50 mA

DC Input Diode Current (I_{IK}) $V_I < 0V$ DC Output Diode Current (I_{OK})

 $V_{O} < 0V$ —50 mA $V_{O} > V_{CC}$

DC Output Source/Sink Current

 (I_{OH}/I_{OL}) ±50 mA

DC V_{CC} or Ground Current per

Supply Pin (I $_{CC}$ or Ground) $\pm 100 \text{ mA}$

Storage Temperature Range (T_{STG}) $-65^{\circ}C$ to $+150^{\circ}C$

Recommended Operating Conditions (Note 4)

Power Supply

 Operating
 1.65V to 3.6V

 Data Retention Only
 1.2V to 3.6V

 Input Voltage
 -0.3V to 3.6V

Output Voltage (VO)

Output in Active States OV to V_{CC} Output in 3-STATE 0.0V to 3.6V

Output Current in I_{OH}/I_{OL}

 $\begin{array}{ll} \text{V}_{\text{CC}} = 3.0 \text{V to } 3.6 \text{V} & \pm 24 \text{ mA} \\ \text{V}_{\text{CC}} = 2.3 \text{V to } 2.7 \text{V} & \pm 18 \text{ mA} \end{array}$

 $V_{CC} = 1.65V \text{ to } 2.3V$ ±6 mA

-40°C to +85°C

Free Air Operating Temperature (T_A) Minimum Input Edge Rate $(\Delta t/\Delta V)$

 $V_{IN} = 0.8V \text{ to } 2.0V, V_{CC} = 3.0V$ 10 ns/V

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The Recommended Operating Conditions tables will define the conditions for actual device operation.

Note 3: IO Absolute Maximum Rating must be observed.

Note 4: Floating or unused pin (inputs or I/O's) must be held HIGH or LOW.

DC Electrical Characteristics (2.7V < $V_{\mbox{\footnotesize CC}} \leq$ 3.6V)

Symbol	Parameter	Conditions	V _{CC}	Min	Max	Units
Syllibol	i didiffetei	Conditions	(V)	Willi	IVIAX	Units
V _{IH}	HIGH Level Input Voltage		2.7-3.6	2.0		V
V _{IL}	LOW Level Input Voltage		2.7-3.6		0.8	V
V _{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7-3.6	V _{CC} - 0.2		
		$I_{OH} = -12 \text{ mA}$	2.7	2.2		V
		$I_{OH} = -18 \text{ mA}$	3.0	2.4		v
		$I_{OH} = -24 \text{ mA}$	3.0	2.2		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.7-3.6		0.2	
		I _{OL} = 12 mA	2.7		0.4	V
		I _{OL} = 18 mA	3.0		0.4	v
		I _{OL} = 24 mA	3.0		0.55	
I	Input Leakage Current	$0V \le V_I \le 3.6V$	2.7-3.6		±5.0	μΑ
I _{OZ}	3-STATE Output Leakage	0V ≤ V _O ≤ 3.6V	2.7-3.6		±10	μА
		$V_I = V_{IH}$ or V_{IL}	2.7-3.0		±10	μΛ
I _{OFF}	Power Off Leakage Current	$0V \le (V_I, V_O) \le 3.6V$	0		10	μΑ
I _{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7-3.6		20	μА
		$V_{CC} \le (V_I, V_O) \le 3.6V \text{ (Note 5)}$	2.7-3.6		±20	μΑ
ΔI_{CC}	Increase in I _{CC} per Input	$V_{IH} = V_{CC} - 0.6V$	2.7–3.6		750	μΑ

Note 5: Outputs disabled or 3-STATE only.

DC Electrical Characteristics (2.3V \leq V_CC \leq 2.7V)

Symbol	Parameter	Conditions	V _{CC}	Min	Max	Units
Syllibol	Talameter Conditions	(V)	WIIII	IVIAX	Units	
V _{IH}	HIGH Level Input Voltage		2.3-2.7	1.6		V
V _{IL}	LOW Level Input Voltage		2.3–2.7		0.7	V
V _{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.3–2.7	V _{CC} - 0.2		
		$I_{OH} = -6 \text{ mA}$	2.3	2.0		V
		$I_{OH} = -12 \text{ mA}$	2.3	1.8		v
		$I_{OH} = -18 \text{ mA}$	2.3	1.7		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3-2.7		0.2	
		I _{OL} = 12mA	2.3		0.4	V
		I _{OL} = 18 mA	2.3		0.6	
I	Input Leakage Current	0 ≤ V _I ≤ 3.6V	2.3-2.7		±5.0	μΑ
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 3.6V	2.3–2.7		±10	
		$V_I = V_{IH}$ or V_{IL}	2.3–2.1		±10	μΑ
I _{OFF}	Power Off Leakage Current	$0 \le (V_I, V_O) \le 3.6V$	0		10	μΑ
Icc	Quiescent Supply Current	V _I = V _{CC} or GND	2.3-2.7		20	
		$V_{CC} \le (V_I, V_O) \le 3.6V$ (Note 6)	2.3–2.7		±20	μΑ

Note 6: Outputs disabled or 3-STATE only.

DC Electrical Characteristics (1.65V \leq $V_{\mbox{\footnotesize CC}} < 2.3\mbox{\footnotesize V})$

Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units
V _{IH}	HIGH Level Input Voltage		1.65 - 2.3	0.65 × V _{CC}		V
V _{IL}	LOW Level Input Voltage		1.65 - 2.3		$0.35 \times V_{CC}$	V
V _{OH}	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 2.3	V _{CC} - 0.2		V
		$I_{OH} = -6 \text{ mA}$	1.65	1.25		v
V _{OL}	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	1.65 - 2.3		0.2	V
		$I_{OL} = 6mA$	1.65		0.3	v
II	Input Leakage Current	$0 \le V_I \le 3.6V$	1.65 - 2.3		±5.0	μΑ
l _{OZ}	3-STATE Output Leakage	$0 \le V_O \le 3.6V$	1.65 - 2.3		±10	μА
		$V_I = V_{IH}$ or V_{IL}				μΑ
I _{OFF}	Power Off Leakage Current	$0 \le (V_I, V_O) \le 3.6V$	0		10	μΑ
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	1.65 - 2.3		20	μА
		$V_{CC} \le (V_I, V_O) \le 3.6V \text{ (Note 7)}$	1.65 - 2.3		±20	μΑ

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 8)

		$T_A = -40^{\circ}$ C to $+85^{\circ}$ C, $C_L = 30$ pF, $R_L = 500\Omega$						
Symbol	Parameter	$V_{CC} = 3.3V \pm 0.3V$		$\rm V_{CC}=2.5\pm0.2V$		$V_{CC}=1.8\pm0.15V$		Units
		Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	250		200		100		MHz
t _{PHL} , t _{PLH}	Propagation Delay Clock to Bus	1.3	3.6	1.5	4.6	2.0	9.2	ns
t _{PZL} , t _{PZH}	Output Enable Time	0.6	3.5	0.8	4.5	1.5	9.0	ns
t _{PLZ} , t _{PHZ}	Output Disable Time	0.6	3.2	0.8	4.2	1.5	7.6	ns
t _S	Setup Time	2.0		2.0		3.0		ns
t _H	Hold Time	0.0		0.0		0.5		ns
t _W	Pulse Width	1.5		1.5		4.0		ns
toshl	Output to Output Skew		0.5		0.5		0.75	ns
toslh	(Note 9)		0.5		0.5		0.75	113

Note 8: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

AC Electrical Characteristics Over Load (Note 10)

		$T_A = -0$	T _A = -0° C to $+70^{\circ}$ C, R _L = 500Ω V _{CC} = 3.3 V \pm 0.3 V				
Symbol	Parameter	C _L =	C _L = 0 pF		C _L = 50 pF		
		Min	Max	Min	Max		
t _{PHL} , t _{PLH}	Prop Delay Clock to Bus	1.1	2.5	1.9	3.9	ns	
t _{PZL} , t _{PZH}	Output Enable Time	0.7	2.4	1.0	3.8	ns	
t _{PLZ} , t _{PHZ}	Output Disable Time	0.7	2.1	1.0	3.5	ns	
t _S	Setup Time	2.0		2.0		ns	
t _H	Hold Time	0.0		0.0		ns	
t _W	Pulse Width	1.5		1.5		ns	

Note 10: This parameter is guaranteed by characterization but not tested.

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V _{CC}	T _A = +25°C Typical	Units
V _{OLP}	Quiet Output Dynamic Peak VOI	$C_{L} = 30 \text{ pF}, V_{IH} = V_{CC}, V_{II} = 0V$	1.8	0.25	
02.	, , ,		2.5	0.6	V
			3.3	0.8	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	-0.25	
			2.5	-0.6	V
			3.3	-0.8	
V _{OHV}	Quiet Output Dynamic Valley VOH	$C_L = 30 \text{ pF}, V_{IH} = V_{CC}, V_{IL} = 0V$	1.8	1.5	
			2.5	1.9	V
			3.3	2.2	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25^{\circ}C$	Units
Syllibol	Farameter	Conditions	Typical	Onits
C _{IN}	Input Capacitance	$V_{I} = 0V \text{ or } V_{CC}, V_{CC} = 1.8V, 2.5V, \text{ or } 3.3V,$	3.5	pF
C _{I/O}	Input/Output Capacitance	$V_{I} = 0V$, or V_{CC} , $V_{CC} = 1.8V$, 2.5V or 3.3V	5.5	pF
C _{PD}	Power Dissipation Capacitance	$V_I = 0V \text{ or } V_{CC}, f = 10 \text{ MHz}, V_{CC} = 1.8V, 2.5V \text{ or } 3.3V$	13	pF

I_{OUT} - V_{OUT} Characteristics



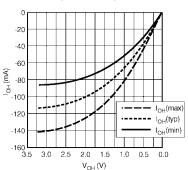


FIGURE 1. Characteristics for Output - Pull Up Driver

${\rm I_{OL}}$ versus ${\rm V_{OL}}$

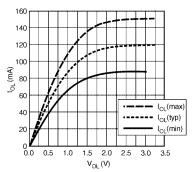


FIGURE 2. Characteristics for Output - Pull Down Driver

AC Loading and Waveforms

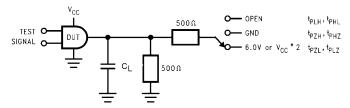


FIGURE 3. AC Test Circuit

TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$; 1.8V to $\pm 0.15V$
t _{PZH} , t _{PHZ}	GND

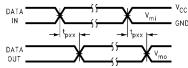


FIGURE 4. Waveform for Inverting and Non-inverting Functions $t_r = t_f \leq 2.0 ns, \, 10\% \ to \ 90\%$

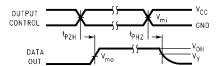


FIGURE 5. 3-STATE Output High Enable and Disable Times for Low Voltage Logic $t_r=t_f \leq 2.0ns,\,10\%\ to\ 90\%$

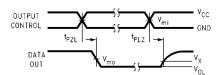


FIGURE 6. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic $t_r=t_f\!\le\!2.0 ns,\,10\%$ to 90%

Symbol	V _{CC}		
	$\textbf{3.3V} \pm \textbf{0.3V}$	$\textbf{2.5V} \pm \textbf{0.2V}$	1.8 ± 0.15V
V _{mi}	1.5V	V _{CC} /2	V _{CC} /2
V _{mo}	1.5V	V _{CC} /2	V _{CC} /2
V _x	V _{OL} + 0.3V	V _{OL} + 0.15V	V _{OL} + 0.15V
V _y	V _{OH} – 0.3V	V _{OH} – 0.15V	V _{OH} – 0.15V

Physical Dimensions inches (millimeters) unless otherwise noted 0.65 TYP AAAAAAIAAAAA 9.20 8.10 6.10±0.10 -B-4.05 0.2 C B A ALL LEAD TIPS PIN #1 IDENT. LAND PATTERN RECOMMENDATION ALL LEAD TIPS 0.1 C +0.15 -0.10 SEE DETAIL A 0.09-0.20 0.10±0.05 0.50 ♦ 0.13 M A BS CS ____ 0.25**M**) A 12.00° TOP & BOTTOM DIMENSIONS ARE IN MILLIMETERS R0.16 CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION EF, REF NOTE 6, DATE 7/93. DIMENSIONS ARE IN MILLIMETERS. SEATING PLANE 0.60±0.10 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. - 100 D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982 DETAIL A MTD64REVB 64-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Package Number MTD64

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