

TC74VCX162827FT

LOW-VOLTAGE 20-BIT BUS BUFFER WITH 3.6 V TOLERANT INPUTS AND OUTPUTS

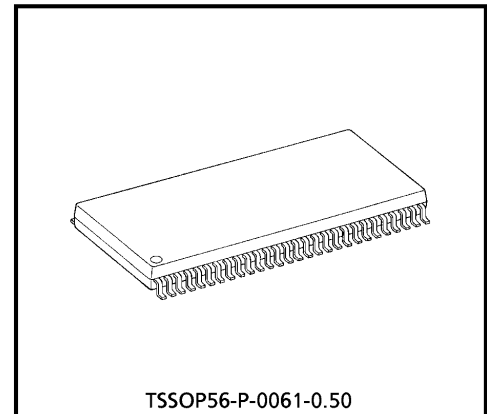
The TC74VCX162827FT is a high performance CMOS 20-bit BUS BUFFER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

The TC74VCX162827FT is composed of two 10-bit sections with separate output-enable signals. For either 10-bit buffer section, the two output-enable ($\overline{1OE1}$ and $\overline{1OE2}$ or $\overline{2OE1}$ and $\overline{2OE2}$) inputs must both be low for the corresponding Y outputs to be active.

When the $\overline{OE}$ input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.

The 26- Ω series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge.



Weight : 0.25 g (Typ.)

FEATURES

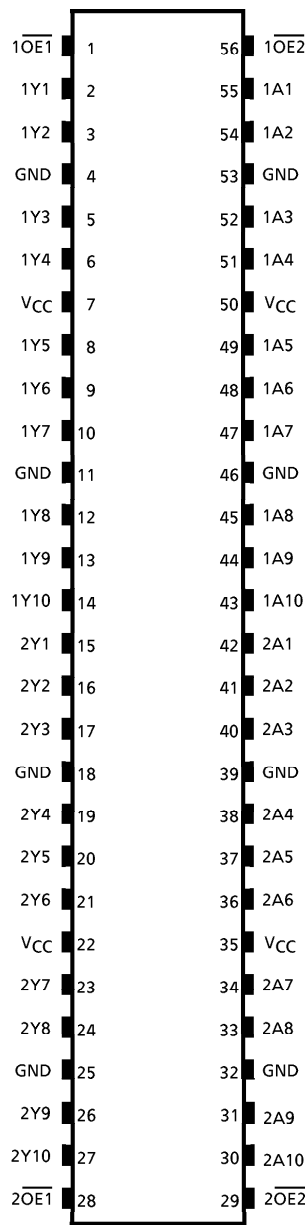
- 26- Ω Series Resistors on Outputs.
- Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6$ V
- High Speed Operation : $t_{pd} = 3.4$ ns (max) at $V_{CC} = 3.0 \sim 3.6$ V
 $t_{pd} = 4.1$ ns (max) at $V_{CC} = 2.3 \sim 2.7$ V
 $t_{pd} = 8.2$ ns (max) at $V_{CC} = 1.8$ V
- 3.6 V Tolerant inputs and outputs.
- Output Current : $I_{OH}/I_{OL} = \pm 12$ mA (min) at $V_{CC} = 3.0$ V
 $I_{OH}/I_{OL} = \pm 8$ mA (min) at $V_{CC} = 2.3$ V
 $I_{OH}/I_{OL} = \pm 4$ mA (min) at $V_{CC} = 1.8$ V
- Latch-up Performance : ± 300 mA
- ESD Performance : Human Body Model $> \pm 2000$ V
Machine Model $> \pm 200$ V
- Package : TSSOP
(Thin Shrink Small Outline Package)
- Power Down Protection is provided on all inputs and outputs.
- Supports live insertion / withdrawal (Note 1)

(Note 1) : To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

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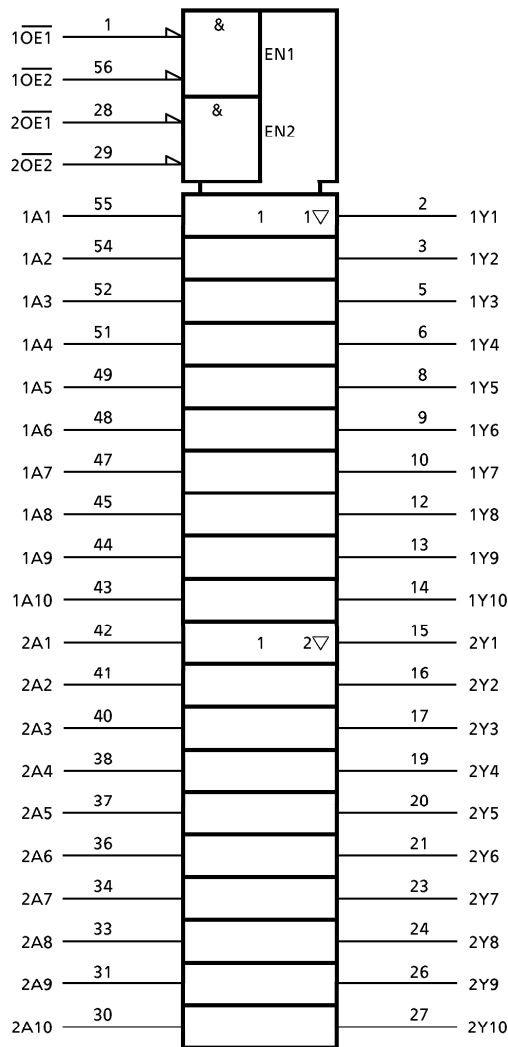
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PIN ASSIGNMENT



(TOP VIEW)

SYMBOL



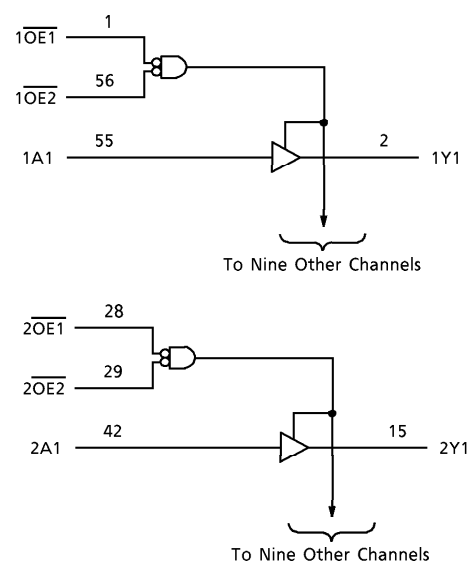
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FUNCTION TABLE (each 10-bit latch)

INPUT			OUTPUT Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	$-0.5 \sim 4.6$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 4.6$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim 4.6$ (Note 1)	V
		$-0.5 \sim V_{CC} + 0.5$ (Note 2)	
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	± 50 (Note 3)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} / Ground Current Per Supply Pin	I_{CC} / I_{GND}	± 100	mA
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

(Note 1) : Off-State

(Note 2) : High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 3) : $V_{OUT} < \text{GND}$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note 4)	
Input Voltage	V_{IN}	$-0.3 \sim 3.6$	V
Output Voltage	V_{OUT}	0~3.6 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH} / I_{OL}	± 12 (Note 7)	mA
		± 8 (Note 8)	
		± 4 (Note 9)	
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise And Fall Time	dt / dv	0~10 (Note 10)	ns / V

(Note 4) : Data Retention Only

(Note 5) : Off-State

(Note 6) : High or Low State

(Note 7) : $V_{CC} = 3.0 \sim 3.6 \text{ V}$ (Note 8) : $V_{CC} = 2.3 \sim 2.7 \text{ V}$ (Note 9) : $V_{CC} = 1.8 \text{ V}$ (Note 10) : $V_{IN} = 0.8 \sim 2.0 \text{ V}$, $V_{CC} = 3.0 \text{ V}$

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = -40~85°C, 2.7 V < V_{CC} ≤ 3.6 V Range)

PARAMETER		SYMBOL	TEST CONDITION		V _{CC} (V)	MIN	MAX	UNIT
Input Voltage	“H” Level	V _{IH}			2.7~3.6	2.0	—	V
	“L” Level	V _{IL}			2.7~3.6	—	0.8	
Output Voltage	“H” Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 100 μA	2.7~3.6	V _{CC} - 0.2	—	V
				I _{OH} = - 6 mA	2.7	2.2	—	
				I _{OH} = - 8 mA	3.0	2.4	—	
				I _{OH} = - 12 mA	3.0	2.2	—	
	“L” Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.7~3.6	—	0.2	
				I _{OL} = 6 mA	2.7	—	0.4	
				I _{OL} = 8 mA	3.0	—	0.55	
				I _{OL} = 12 mA	3.0	—	0.8	
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6 V	2.7~3.6	—	± 5.0	μA	
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6 V	2.7~3.6	—	± 10.0	μA	
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6 V	0	—	10.0	μA	
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		2.7~3.6	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V		2.7~3.6	—	± 20.0	
Increase In I _{CC} Per Input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6 V		2.7~3.6	—	750	μA

DC characteristics (Ta = -40~85°C, 2.3 V ≤ V_{CC} ≤ 2.7 V Range)

PARAMETER		SYMBOL	TEST CONDITION			MIN	MAX	UNIT	
					V _{CC} (V)				
Input Voltage	“H” Level	V _{IH}				2.3~2.7	1.6	—	V
	“L” Level	V _{IL}				2.3~2.7	—	0.7	
Output Voltage	“H” Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.3~2.7	V _{CC} - 0.2	—	V	
				I _{OH} = -4 mA	2.3	2.0	—		
				I _{OH} = -6 mA	2.3	1.8	—		
				I _{OH} = -8 mA	2.3	1.7	—		
	“L” Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.3~2.7	—	0.2		
				I _{OL} = 6 mA	2.3	—	0.4		
				I _{OL} = 8 mA	2.3	—	0.6		
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6 V		2.3~2.7	—	± 5.0	μA	
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6 V		2.3~2.7	—	± 10.0	μA	
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6 V		0	—	10.0	μA	
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		2.3~2.7	—	20.0	μA	
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V		2.3~2.7	—	± 20.0		

ELECTRICAL CHARACTERISTICSDC characteristics (Ta = -40~85°C, 1.8 V ≤ V_{CC} < 2.3 V Range)

PARAMETER		SYMBOL	TEST CONDITION			MIN	MAX	UNIT	
			V _{CC} (V)						
Input Voltage	“H” Level	V _{IH}	1.8~2.3			0.7 × V _{CC}	—	V	
	“L” Level	V _{IL}	1.8~2.3			—	0.2 × V _{CC}		
Output Voltage	“H” Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = − 100 μA	1.8	V _{CC} − 0.2	—	V	
				I _{OH} = − 4 mA	1.8	1.4	—		
	“L” Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.8	—	0.2		
				I _{OL} = 4 mA	1.8	—	0.3		
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6 V			1.8	—	± 5.0	μA
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6 V			1.8	—	± 10.0	μA
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6 V			0	—	10.0	μA
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND			1.8	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V			1.8	—	± 20.0	

AC characteristics (Ta = -40~85°C, Input $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500 \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	MIN	MAX	UNIT
Propagation Delay Time	t_{pLH} t_{pHL}	(Fig.1, 2)	1.8	1.5	8.2	ns
			2.5 ± 0.2	1.0	4.1	
			3.3 ± 0.3	0.8	3.4	
3-State Output Enable Time	t_{pZL} t_{pZH}	(Fig.1, 3)	1.8	1.5	9.8	ns
			2.5 ± 0.2	1.0	5.9	
			3.3 ± 0.3	0.8	4.3	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	(Fig.1, 3)	1.8	1.5	8.8	ns
			2.5 ± 0.2	1.0	4.9	
			3.3 ± 0.3	0.8	4.3	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 11)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.

(Note 11) : Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic switching characteristics (Ta = 25°C, Input $t_r = t_f = 2.0$ ns, $C_L = 30$ pF)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	$V_{IH} = 1.8$ V, $V_{IL} = 0$ V (Note 12)	1.8	0.15	V
		$V_{IH} = 2.5$ V, $V_{IL} = 0$ V (Note 12)	2.5	0.25	
		$V_{IH} = 3.3$ V, $V_{IL} = 0$ V (Note 12)	3.3	0.35	
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	$V_{IH} = 1.8$ V, $V_{IL} = 0$ V (Note 12)	1.8	-0.15	V
		$V_{IH} = 2.5$ V, $V_{IL} = 0$ V (Note 12)	2.5	-0.25	
		$V_{IH} = 3.3$ V, $V_{IL} = 0$ V (Note 12)	3.3	-0.35	
Quiet Output Minimum Dynamic V_{OH}	V_{OHV}	$V_{IH} = 1.8$ V, $V_{IL} = 0$ V (Note 12)	1.8	1.55	V
		$V_{IH} = 2.5$ V, $V_{IL} = 0$ V (Note 12)	2.5	2.05	
		$V_{IH} = 3.3$ V, $V_{IL} = 0$ V (Note 12)	3.3	2.65	

(Note 12) : Parameter guaranteed by design.

Capacitive characteristics (Ta = 25°C)

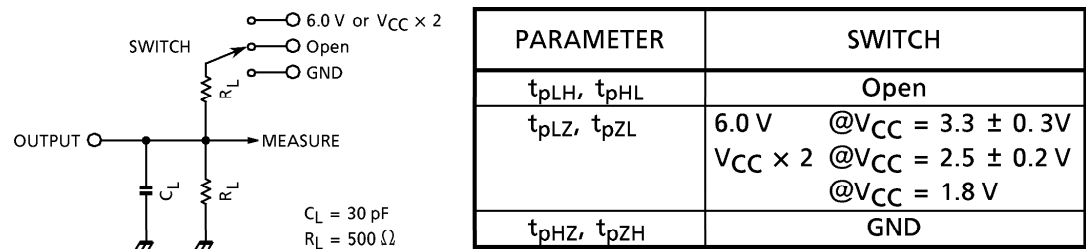
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	UNIT
Input Capacitance	C_{IN}		1.8, 2.5, 3.3	6	pF
Output Capacitance	C_{OUT}		1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C_{PD}	$f_{IN} = 10$ MHz (Note 13)	1.8, 2.5, 3.3	20	pF

(Note 13) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/20 \text{ (Per bit)}$$

TEST CIRCUIT
Fig.1



AC WAVEFORM

Fig.2 t_{pLH} , t_{pHL}

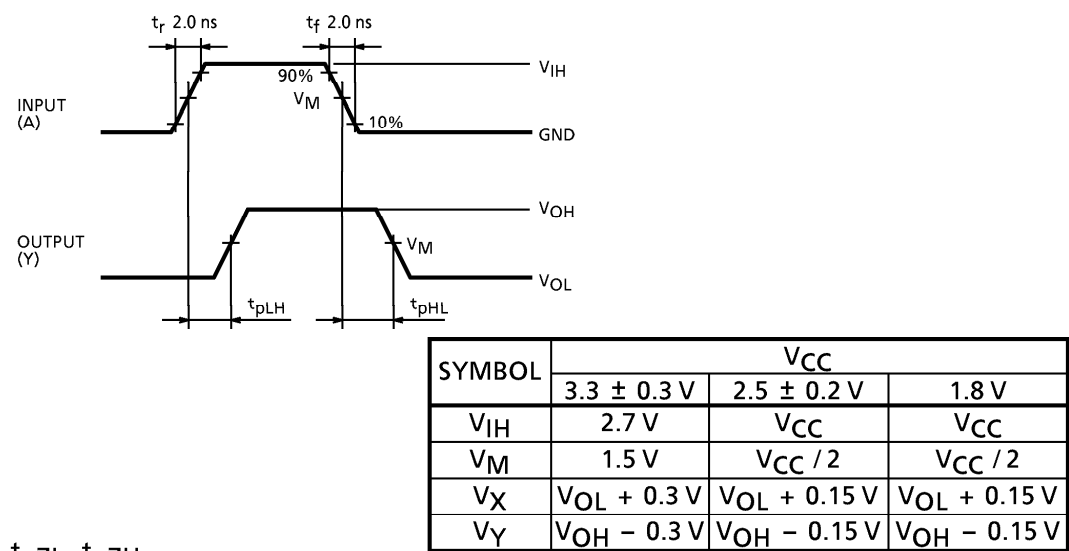
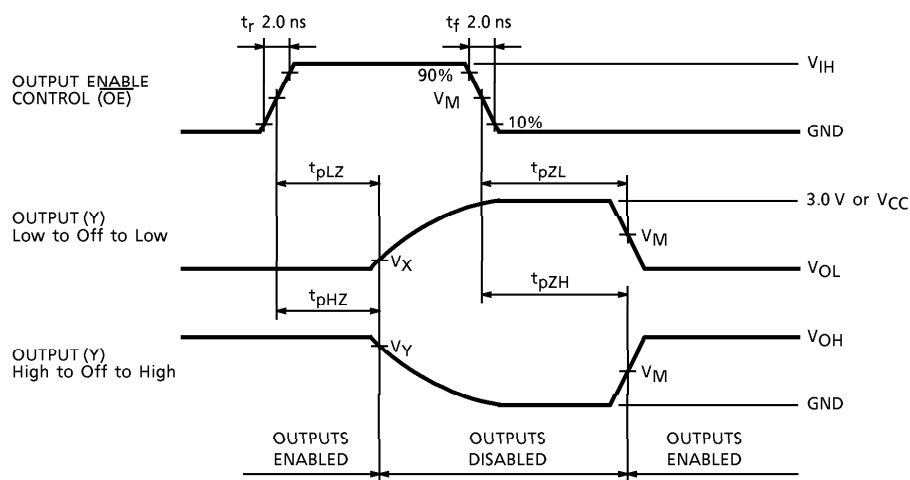


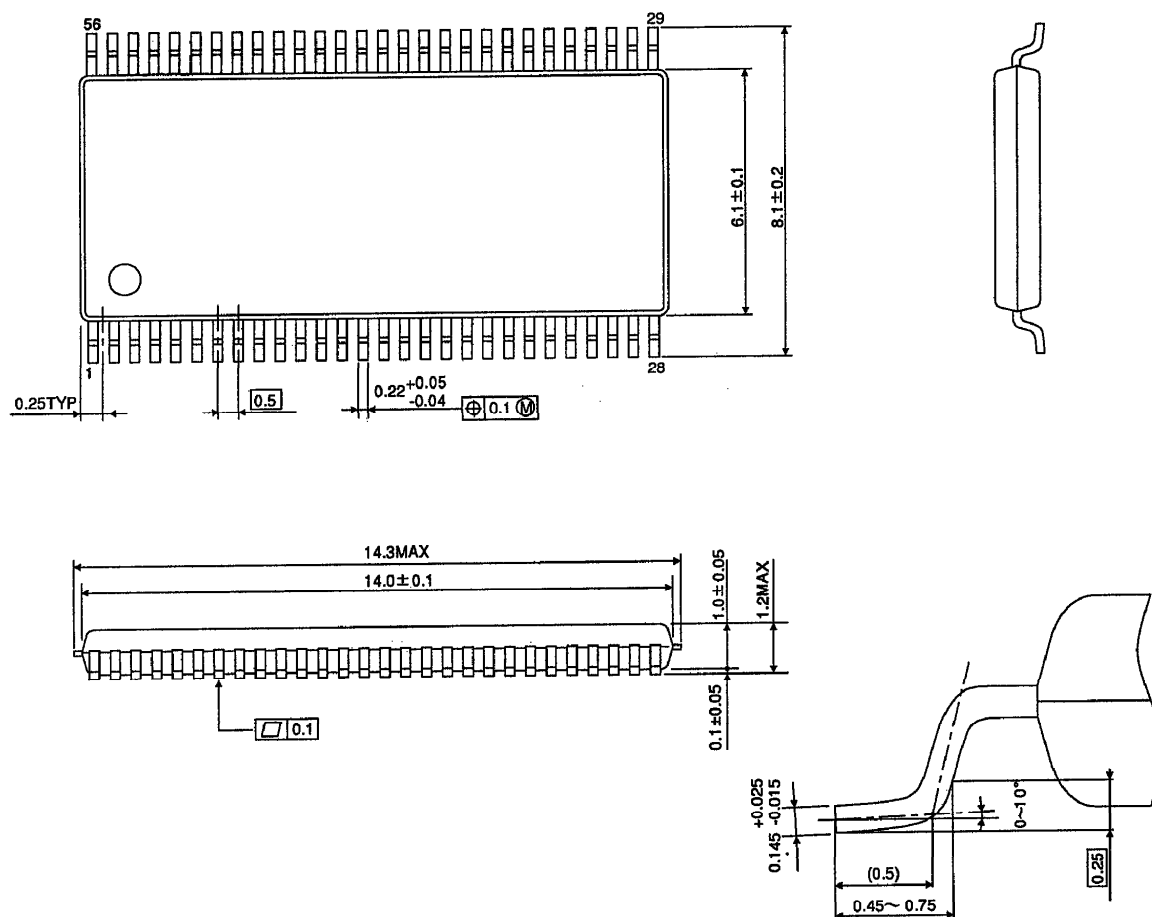
Fig.3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}



OUTLINE DRAWING

TSSOP56-P-0061-0.50

Unit : mm



Weight : 0.25 g (Typ.)

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