TOSHIBA TC74VCX16646FT

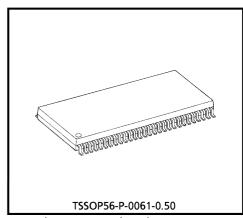
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCX16646FT

LOW VOLTAGE 16-BIT BUS TRANSCEIVER / REGISTER WITH 3.6 V TOLERANT INPUTS AND OUTPUTS

The TC74VCX16646FT is a high parformance CMOS 16-bit BUS TRANSCEIVER/REGISTER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. All inputs are equipped with protection circuits against static discharge.



Weight: 0.25 g (Typ.)

FEATURES

Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6 \text{ V}$

High Speed Operation : t_{pd} = 2.9 ns (max) at V_{CC} = 3.0~3.6 V

: t_{pd} = 3.5 ns (max) at V_{CC} = 2.3~2.7 V : tpd = 7.0 ns (max) at V_{CC} = 1.8 V

3.6 V Tolerant inputs and outputs.

Output Current : $I_{OH}/I_{OL} = \pm 24 \,\text{mA}$ (min) at $V_{CC} = 3.0 \,\text{V}$

: $I_{OH}/I_{OL} = \pm 18 \text{ mA (min)}$ at $V_{CC} = 2.3 \text{ V}$: $I_{OH}/I_{OL} = \pm 6 \text{ mA (min)}$ at $V_{CC} = 1.8 \text{ V}$

: ±300 mA Latch-up Performance

ESD Performance : Human Body Model > ±2000 V

: Machine Model > ±200 V

: TSSOP (Thin Shrink Small Outline Package) Package

Bidirectional interface between 2.5 V and 3.3 V signals.

Power Down Protection is provided on all inputs and outputs

Supports live insertion/withdrawal (Note 3)

(Note 1): Do not apply a signal to any bus terminal when it is in the output mode. Damage may

(Note 2): All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.

(Note 3): To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

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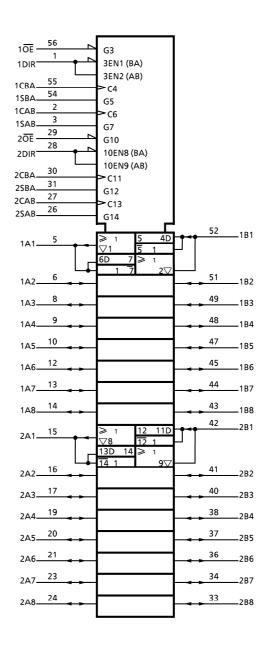
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PIN ASSIGNMENT

56 1OE 1DIR 55 1CBA 1CAB 1SAB 3 54 1SBA GND 4 53 GND 52 1B1 1A1 5 51 1B2 1A2 6 V_{CC} 7 50 V_{CC} 1A3 8 49 1B3 1A4 9 48 1B4 1A5 10 47 1B5 GND 11 46 GND 45 1B6 1A6 12 1A7 13 44 1B7 1A8 14 43 1B8 42 2B1 2A1 15 41 2B2 2A2 16 2A3 17 40 2B3 **GND** 18 39 GND 38 2B4 2A4 19 2A5 20 37 2B5 2A6 21 36 2B6 V_{CC} 22 35 V_{CC} 2A7 23 34 2B7 2A8 24 33 2B8 32 GND GND 25 2SAB 26 31 2SBA 2CAB 27 30 2CBA 2DIR 28 29 2OE

(TOP VIEW)

SYMBOL



TRUTH TABLE

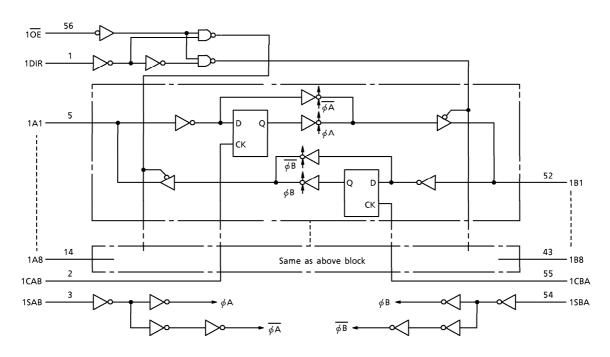
	C	ONTRO	L INPU	ΓS		ВІ	JS	FUNCTION
ŌĒ	DIR	CAB	СВА	SAB	SBA	Α	В	FUNCTION
		X*	X*	х	Х	INPUT Z	INPUT Z	The output functions of A and B Busses are disabled.
Н	X			х	x	х	х	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
		X*	X*	L	x	INPUT L H	OUTPUT L H	The data on the A bus are displayed on the B bus.
	н		X*	L	х	L H	L H	The data on the A bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	Н	×	х	Qn	The data in the A storage flop-flops are displayed on the B Bus.
		F	X*	Н	X	L	L	The data on the A Bus are stored into the A storage flip-flops on the rising edge of
		7		''		н	Н	CAB, and the stored data propagate directly onto the B Bus.
		X*	X*	x	L	OUTPUT L	INPUT L	The data on the B Bus are displayed on the A bus.
						Н	Н	
		V.4	<u>+</u> -	.,		L	L	The data on the B Bus are displayed on the
		X*		Х	L	Н	Н	A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
L	L	X*	X*	х	Н	Qn	×	The data in the B storage flip-flops are displayed on the A Bus.
		V*	f	V	1.1	L	L	The data on the B Bus are stored into the B storage flip-flops on the rising edge of
		X*		X	Н	Н	Н	CBA, and the stored data propagate directly onto the A Bus.

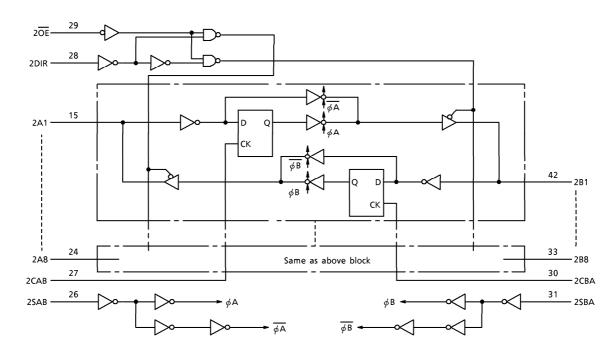
X : Don't careZ : High Impedance

Qn: The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

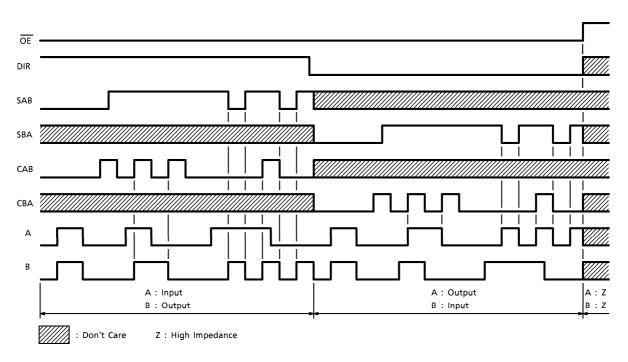
* The clocks are not internally with either $\overline{\text{OE}}$ or DIR. Thefore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

SYSTEM DIAGRAM





TIMING CHART



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V _C C	-0.5~4.6	V
DC Input Voltage (DIR, $\overline{\text{OE}}$, CAB, CBA, SAB, SBA)	V _{IN}	- 0.5~4.6	٧
DC Bus I/O Voltage	V	-0.5~4.6 (Note 1)	V
DC Bus I/O Voltage	V _I /O	-0.5~V _{CC} + 0.5 (Note 2)]
Input Diode Current	ΙΚ	– 50	mA
Output Diode Current	^I ОК	±50 (Note 3)	mA
DC Output Current	IOUT	± 50	mA
Power Dissipation	PD	400	mW
DC V _{CC} / Ground Current Per Supply Pin	Icc/IGND	± 100	mA
Storage Temperature	T _{stg}	-65∼150	°C

(Note 1) : Off-State

(Note 2) : High or Low State. IOUT absolute maximum rating must be observed.

(Note 3) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	\/	1.8~3.6	V
Supply Voltage	VCC	1.2~3.6 (Note 4)	'
Input Voltage (DIR, $\overline{\text{OE}}$, CAB, CBA, SAB, SBA)	VIN	-0.3~3.6	٧
Bus I/O Voltage	\/ .	0~3.6 (Note 5)	V
Bus 170 Voltage	V _I /O	0∼ V _{CC} (Note 6)	\ \ \
		± 24 (Note 7)	
Output Current	IOH/IOL	± 18 (Note 8)	mA
		±6 (Note 9)	
Operating Temperature	T _{opr}	- 40∼85	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 10)	ns / V

(Note 4) : Data Retention Only

(Note 5) : Off-State

(Note 5) : On-state (Note 6) : High or Low State (Note 7) : $V_{CC} = 3.0 \sim 3.6 \text{ V}$ (Note 8) : $V_{CC} = 2.3 \sim 2.7 \text{ V}$ (Note 9) : $V_{CC} = 1.8 \text{ V}$ (Note 10) : $V_{IN} = 0.8 \sim 2.0 \text{ V}$, $V_{CC} = 3.0 \text{ V}$

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = $-40\sim85^{\circ}$ C, 2.7 V < V_{CC} \leq 3.6 V)

PARA	METER	SYMBOL	TEST	CONDITION	V _{CC} (V)	MIN	MAX	UNIT
Input	"H" Level	VIH			2.7~3.6	2.0	_	V
Voltage	"L" Level	V _{IL}			2.7~3.6	_	0.8	V
			.,	I _{OH} = -100 μA	2.7~3.6	V _{CC} - 0.2	1	
	"H" Level	Voн	V _{IN} =	I _{OH} = -12 mA	2.7	2.2		V
			V _{IH} or V _{IL}	I _{OH} = -18 mA	3.0	2.4	_	
Output				I _{OH} = -24 mA	3.0	2.2	_	
Voltage				I _{OL} = 100 μA	2.7~3.6	_	0.2	
	"L" Level	\/ a .	V _{IN} =	I _{OL} = 12 mA	2.7	_	0.4	v
	L Levei	VOL	VIH or VIL	I _{OL} = 18 mA	3.0	_	0.4	·
				I _{OL} = 24 mA	3.0	_	0.55	
Input Leaka	age Current	IN	$V_{IN} = 0 \sim 3$.	6 V	2.7~3.6	_	± 5.0	μ A
	3-State Output Off-State Current		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = 0 \sim 3.6 \text{ V}$		2.7~3.6		± 10.0	μΑ
Power Off Current	Power Off Leakage I_{OFF} V_{IN} , $V_{OUT} = 0 \sim 3.6 \text{ V}$		= 0~3.6 V	0		10.0	μ A	
Quiescent Supply		laa	$V_{IN} = V_{CC}$	or GND	2.7~3.6		20.0	
Current		lcc	$V_{CC} \leq (V_{IN})$	$V_{OUT} \leq 3.6 V$	2.7~3.6		± 20.0	μ A
Increase In Input	I _{CC} Per	∆ارح	V _{IH} = V _{CC}	- 0.6 V	2.7~3.6	_	750	μΑ

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = $-40\sim85^{\circ}$ C, 2.3 V \leq V_{CC} \leq 2.7 V)

PARA	PARAMETER SYMBOL		TEST	TEST CONDITION		MIN	MAX	UNIT
Input	"H" Level	V_{IH}			2.3~2.7	1.6	_	V
Voltage	"L" Level	V _{IL}			2.3~2.7	_	0.7	V
			.,	I _{OH} = -100 μA	2.3~2.7	V _C C - 0.2	_	
	utput "H" Level VOH VIN = VIH or VIL		$I_{OH} = -6 \text{mA}$	2.3	2.0		V	
Output			VIH or VIL	I _{OH} = -12 mA	2.3	1.8	_	.
Voltage				I _{OH} = -18 mA	2.3	1.7		
			\/	I _{OL} = 100 μA	2.3~2.7	_	0.2	
	"L" Level	v_{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12 mA	2.3	_	0.4	V
			VIH OI VIL	I _{OL} = 18 mA	2.3	_	0.6	
Input Leak	age Current	IN	V _{IN} = 0~3.6 V		2.3~2.7	_	± 5.0	μΑ
3-State Output Off-State Current		loz	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6 V		2.3~2.7		± 10.0	μ A
Power Off Leakage Current IOFF VIN, VOUT		= 0~3.6 V	0	_	10.0	μ A		
Quiescent S	Supply	laa	$V_{IN} = V_{CC}$	or GND	2.3~2.7	_	20.0	
Current		lcc	V _{CC} ≤ (V _{IN}	, V _{OUT}) ≤ 3.6 V	2.3~2.7	_	± 20.0	μ A

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = $-40\sim85^{\circ}$ C, $1.8 \text{ V} \leq \text{V}_{CC} < 2.3 \text{ V})$

PARA	METER	SYMBOL	TEST	TEST CONDITION		MIN	MAX	UNIT
Input	"H" Level	V _{IH}				0.7 × V _{CC}	1	٧
Voltage	"L" Level	V_{IL}			1.8~2.3	_	0.2 x V _C C	V
Outnut	"H" Level	V _{ОН}	V _{IN} =	I _{OH} = -100 μA	1.8	V _{CC} - 0.2	_	V
Output Voltage			V _{IH} or V _{IL}	I _{OH} = -6 mA	1.8	1.4	_	
voitage	"L" Level	V	V _{IN} =	I _{OL} = 100 μA	1.8	_	0.2	V
	L Levei	V_{OL}	V _{IH} or V _{IL}	I _{OL} = 6 mA	1.8	_	0.3	·
Input Leak	age Current	lи	$V_{IN} = 0 \sim 3$.	6 V	1.8	_	± 5.0	μ A
3-State Out Off-State C		loz	V _{IN} = V _{IH} (V _{OUT} = 0~	or V _{IL} -3.6 V	1.8	1	± 10.0	μΑ
Power Off Leakage Current		V _{IN} , V _{OUT} = 0~3.6 V		0		10.0	μΑ	
Quiescent S	Supply	loc	$V_{IN} = V_{CC}$	or GND	1.8	_	20.0	μ A
Current		lcc	$V_{CC} \le V_{IN}$, V_{OUT}) $\leq 3.6 V$	1.8		± 20.0	μ A

716 characteristics (14 - 40 05 c, hipat tr - tr - 2.0115, cr - 50 pr, 14 - 500 22)	AC characteristics (Ta =	$-40\sim85^{\circ}$ C, Input t _r =	$t_f = 2.0 \text{ ns}, C_L = 30 \text{ pF}, R_L$	$=$ 500 Ω)
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PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	MIN	MAX	UNIT
Manimum Clark			1.8	100	_	
Maximum Clock Frequency	fMAX	(Fig.1, 2)	2.5 ± 0.2	200	_	MHz
rrequency			3.3 ± 0.3	250	_	
Dranagation Dalay Time	4		1.8	1.5	7.0	
Propagation Delay Time (An, Bn-Bn, An)	t _{pLH}	(Fig.1, 2)	2.5 ± 0.2	0.8	3.5	ns
(All, Bil-Bil, All)	^t pHL		3.3 ± 0.3	0.6	2.9	
Propagation Delay Time	+		1.8	1.5	8.8	
(CAB, CBA-Bn, An)	t _{pLH}	(Fig.1, 3)	2.5 ± 0.2	0.8	4.4	ns
(CAB, CBA-BII, AII)	^t pHL		3.3 ± 0.3	0.6	3.2	
Dranagation Dalay Time	4		1.8	1.5	8.8	
Propagation Delay Time (SAB, SBA-Bn, An)	t _{pLH}	(Fig.1, 2)	2.5 ± 0.2	0.8	4.4	ns
(SAB, SBA-BII, AII)	^t pHL		3.3 ± 0.3	0.6	3.5	
Output Enable Time	+		1.8	1.5	9.8	
(OE, DIR-An, Bn)	t _{pZL}	(Fig.1, 4, 5)	2.5 ± 0.2	0.8	4.9	ns
(OE, DIR-AII, BII)	^t pZH		3.3 ± 0.3	0.6	3.8	
Output Disable Time			1.8	1.5	7.6	
Output Disable Time (OE, DIR-An, Bn)	t _{pLZ}	(Fig.1, 4, 5)	2.5 ± 0.2	0.8	4.2	ns
(OE, DIR-AII, BII)	^t pHZ		3.3 ± 0.3	0.6	3.7	
	4		1.8	4.0	_	
Minimum Pulse Width	tw (H)	(Fig.1, 3)	2.5 ± 0.2	1.5	_	ns
	^t w (L)		3.3 ± 0.3	1.5	_	
			1.8	2.5	_	
Minimum Set-up Time	t _s	(Fig.1, 3)	2.5 ± 0.2	1.5	_	ns
			3.3 ± 0.3	1.5	_	
			1.8	1.0	_	
Minimum Hold Time	t _h	(Fig.1, 3)	2.5 ± 0.2	1.0	_	ns
			3.3 ± 0.3	1.0	_	
	4		1.8	_	0.5	
Output to Output Skew	tosLH	(Note 11)	2.5 ± 0.2	_	0.5	ns
	^t osHL		3.3 ± 0.3		0.5	

For $C_L = 50 \, pF$, add approximately 300 ps to the AC maximum specification.

(Note 11) : Parameter guaranteed by design.
$$(t_{OSLH} = |t_{pLHm} - t_{pLHn}|, \ t_{OSHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic switching characteri	tics ($Ta = 25^{\circ}C$,	Input $t_r = t_f$	$f = 2.0 \text{ ns}, C_1$	= 30 pF)
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PARAMETER	SYMBOL	TEST CONDITIO	DN	V _{CC} (V)	TYP.	UNIT
Quiet Output Maximum		$V_{IH} = 1.8 V, V_{IL} = 0 V$	(Note 12)	1.8	0.25	
Dynamic VOL	V _{OLP}	$V_{IH} = 2.5 V, V_{IL} = 0 V$	(Note 12)	2.5	0.6	V
Dynamic VOL		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	(Note 12)	3.3	0.8	
Quiet Output Minimum		$V_{IH} = 1.8 V, V_{IL} = 0 V$	(Note 12)	1.8	- 0.25	
Dynamic VOL	VOLV	$V_{IH} = 2.5 V, V_{IL} = 0 V$	(Note 12)	2.5	- 0.6	V
Dynamic VOL		$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	(Note 12)	3.3	- 0.8	
Quiet Quanua Minimum		V _{IH} = 1.8 V, V _{IL} = 0 V	(Note 12)	1.8	1.5	
Quiet Output Minimum Dynamic V _{OH}	VOHV	$V_{IH} = 2.5 V, V_{IL} = 0 V$	(Note 12)	2.5	1.9] v [
Dynamic VOH		V _{IH} = 3.3 V, V _{IL} = 0 V	(Note 12)	3.3	2.2	

(Note 12): Parameter guaranteed by design.

Capacitive characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Input Capacitance	CIN	DIR, SAB, SBA, CAB, CBA, OE	1.8, 2.5, 3.3	6	рF
Bus I/O Capacitance	CI/O	An, Bn	1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10 MHz (Note 13)	1.8, 2.5, 3.3	20	рF

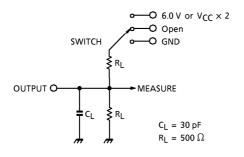
(Note 13): CpD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

ICC (opr.) = CpD·VCC·fIN + ICC / 16 (per bit)

TEST CIRCUIT

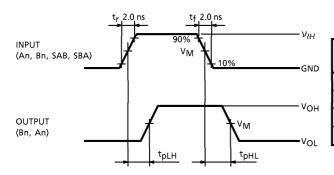
Fig.1



PARAMETER	SWITCH
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	6.0 V @V _{CC} = 3.3 ± 0.3 V V _{CC} × 2 @V _{CC} = 2.5 ± 0.2 V @V _{CC} = 1.8 V
	$V_{CC} \times 2 @V_{CC} = 2.5 \pm 0.2 V$
	$@V_{CC} = 1.8 V$
t _{pHZ} , t _{pZH}	GND

AC WAVEFORM

 $Fig. 2 \quad t_{pLH}, \ t_{pHL}$



SYMBOL	V _{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
v_{IH}	2.7 V	V _{CC}	VCC
٧M	1.5 V	V _{CC} /2	V _{CC} /2
٧x	V _{OL} + 0.3 V	V _{OL} + 0.15 V	V _{OL} + 0.15 V
VY	V _{OH} - 0.3 V	V _{OH} – 0.15 V	V _{OH} – 0.15 V

Fig.3 t_{pLH} , t_{pHL} , t_{w} , t_{s} , t_{h}

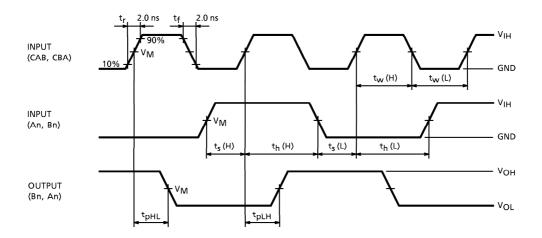


Fig.4 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

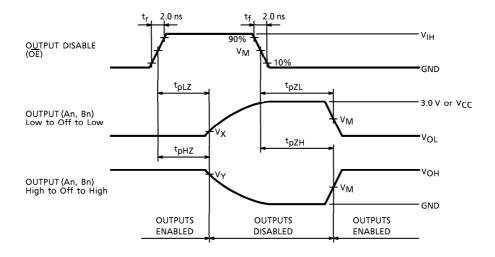
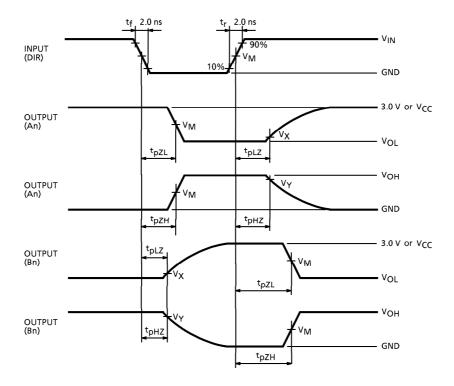
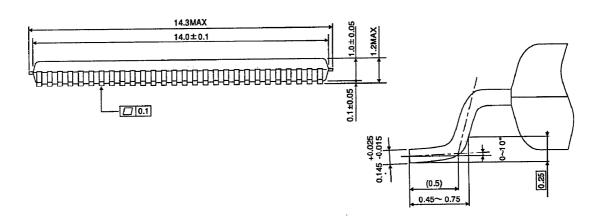


Fig.5 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}



OUTLINE DRAWING TSSOP56-P-0061-0.50 Unit: mm



Weight: 0.25 g (Typ.)

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