TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

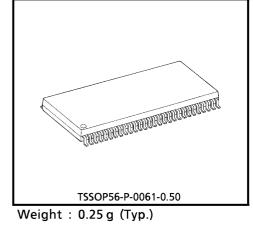
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LOW-VOLTAGE 18-BIT UNIVERSAL BUS DRIVER WITH 3.6 V TOLERANT INPUTS AND OUTPUTS

The TC74VCX16835FT is a high performance CMOS 18-bit UNIVERSAL BUS DRIVER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Data flow from A to Y is controlled by the output-enable (OE) input. The device operates in the transparent mode when the latch-enable (LE) input is high. When LE is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch / flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the highimpedance state.



All inputs are equipped with protection circuits against static discharge.

FEATURES

- Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6 V$
- High Speed Operation : t_{pd} = 3.3 ns (max.) at V_{CC} = 3.0~3.6 V : $t_{pd} = 4.2 \text{ ns} (\text{max.}) \text{ at } V_{CC} = 2.3 \sim 2.7 \text{ V}$: $t_{pd} = 8.4 \text{ ns} (\text{max.}) \text{ at } V_{CC} = 1.8 \text{ V}$ 3.6 V Tolerant inputs and outputs. **Output Current** $: I_{OH} / I_{OL} = \pm 24 \text{ mA} (\text{min.}) \text{ at } V_{CC} = 3.0 \text{ V}$
- $: I_{OH} / I_{OL} = \pm 18 \text{ mA} (\text{min.}) \text{ at } V_{CC} = 2.3 \text{ V}$ $: I_{OH} / I_{OL} = \pm 6 \text{ mA} \text{ (min.) at } V_{CC} = 1.8 \text{ V}$ Latch-up Performance : ±300mA **ESD** Performance : Human Body Model > $\pm 2000 V$
- : Machine Model > $\pm 200 V$
- : TSSOP Package

(Thin Shrink Small Outline Package)

- Power Down Protection is provided on all inputs and outputs.
- Supports live insertion / withdrawal (Note 1)

(Note 1) : To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

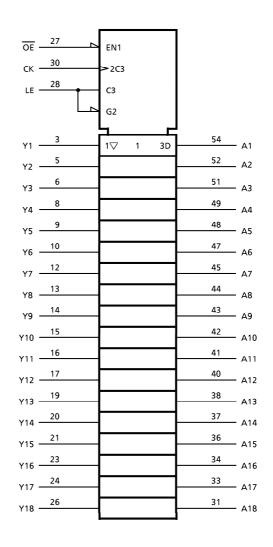
980910EBA2 980910EBA:
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1999-08-10 1/13

PIN ASSIGNMENT

NC	1	56	GND
NC	2	55	NC
Y1	3	54	A1
GND	4	53	GND
Y2	5	52	A2
Y3	6	51	A3
V _{CC}	7	50	VCC
Y4	8	49	A4
Y5	9	48	A5
Y6	10	47	A6
GND	11	46	GND
Y7	12	45	A7
Y8	13	44	A8
Y9	14	43	A9
Y10	15	42	A10
Y11	16	41	A11
Y12	17	40	A12
GND	18	39	GND
Y13	19	38	A13
Y14	20	37	A14
Y15	21	36	A15
V _{CC}	22	35	VCC
Y16	23	34	A16
Y17	24	33	A17
GND	25	32	GND
Y18	26	31	A18
OE	27	30	СК
LE	28	29	GND

SYMBOL



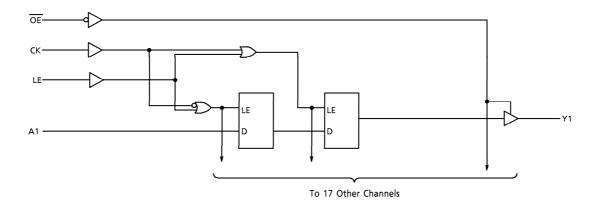
(TOP VIEW)

TRUTH TABLE

	INP		OUTPUTS	
OE	LE	СК	А	Y
Н	Х	Х	Х	Z
L	Н	Х	L	L
L	Н	Х	Н	Н
L	L	<u> </u>	L	L
L	L		Н	Н
L	L	Н	Х	Y0 *
L	L	L	Х	Y0 *

(*) : Output level before the indicated steady-state input conditions were established, provided that CK was high or low before LE went low.

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V _{CC}	-0.5~4.6	V
DC Input Voltage	VIN	-0.5~4.6	V
DC Output Voltage	Maxim	-0.5~4.6 (Note 2)	v
DC Output Voltage	VOUT	-0.5~V _{CC} + 0.5 (Note 3)	v
Input Diode Current	liκ	- 50	mA
Output Diode Current	юк	±50 (Note 4)	mA
DC Output Current	Ιουτ	± 50	mA
Power Dissipation	PD	400	mW
DC V _{CC} /Ground Current Per Supply Pin	ICC / IGND	± 100	mA
Storage Temperature	T _{stg}	- 65~150	°C

(Note 2) : Off-State

(Note 3) : High or Low State. $I_{\mbox{OUT}}$ absolute maximum rating must be observed.

(Note 4) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT			
Supply Voltage	Maa	1.8~3.6	V			
Supply Voltage	Vcc	1.2~3.6 (Note 5)	v			
Input Voltage	VIN	-0.3~3.6	V			
Output Voltage	No. c	0~3.6 (Note 6)	V			
	V _I /O 0~ V _{CC} (Note 7)					
		±24 (Note 8)				
Output Current	IOH/IOL	± 18 (Note 9)	mA			
		±6 (Note 10)	- V			
Operating Temperature	T _{opr}	- 40~85	°C			
Input Rise And Fall Time	dt/dv	0~10 (Note 11)	ns/V			

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = $-40 \sim 85^{\circ}$ C, 2.7 V < V_{CC} \leq 3.6 V)

-									
PARA	METER	SYMBOL	TEST	CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT	
Input	"H" Level	VIH			2.7~3.6	2.0	—	v	
Voltage	"L" Level	VIL			2.7~3.6	_	0.8	v	
	"!!" ! evel			I _{OH} = −100 μA	2.7~3.6	V _{CC} - 0.2			
	"H" Level	∨он		VIN =	$I_{OH} = -12 \text{ mA}$	2.7	2.2	—	
			VIH or VIL	$I_{OH} = -18 \text{ mA}$	3.0	2.4	—		
Output	Voltage			$I_{OH} = -24 \text{ mA}$	3.0	2.2	_	V	
Voltage			I _{OL} = 100 μA	2.7~3.6	_	0.2			
// / / aa	"L" Level	Max	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12 mA	2.7	_	0.4		
	L Levei	VOL		I _{OL} = 18 mA	3.0	_	0.4		
				I _{OL} = 24 mA	3.0	_	0.55		
Input Leaka	age Current	l _{IN}	$V_{IN} = 0 \sim 3.$	6 V	2.7~3.6	_	± 5.0	μA	
3-State Out Off-State C	urrent	loz	V _{IN} = V _{IH} V _{OUT} = 0~	or V _{IL} -3.6 V	2.7~3.6	_	± 10.0	μΑ	
Power Off Current	Leakage	lOFF	VIN, VOUT	= 0~3.6 V	0	_	10.0	μA	
Quiescent S	Supply	1	$V_{IN} = V_{CC}$	or GND	2.7~3.6	—	20.0		
Current	-	lcc	$V_{CC} \leq (V_{IN})$	$V, V_{OUT}) \leq 3.6 V$	2.7~3.6	_	±20.0	μA	
Increase In Input	ICC Per	⊿ارر	V _{IH} = V _{CC}	– 0.6 V	2.7~3.6		750	μΑ	

ELECTRICAL CHARACTERISTICS DC characteristics (Ta = $-40{\sim}85^\circ\text{C}\text{, }2.3~\text{V} \leq \text{V}_{CC} \leq 2.7~\text{V}\text{)}$

PARA	METER	SYMBOL	TEST	CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT
Input	"H" Level	VIH			2.3~2.7	1.6		N/
Voltage	"L" Level	VIL			2.3~2.7	_	0.7	V
	"H" Lovol			I _{OH} = -100 μA	2.3~2.7	V _{CC} - 0.2	_	
"H" Level Output Voltage	∨он	VIN =	I _{OH} = -6 mA 2.3 2.0	_				
		VIH or VIL	$I_{OH} = -12 \text{ mA}$	2.3	1.8	— v	V	
				I _{OH} = -18 mA	2.3	1.7		v
			V	l _{OL} = 100 μA	2.3~2.7	—	0.2	
	"L" Level	VOL	V _{IN} = V _{IH} or V _{IL}	l _{OL} = 12 mA	2.3	_	- 0.4	
			VIH OF VIL	I _{OL} = 18 mA	2.3	_	0.6	
Input Leak	age Current	IIN	$V_{IN} = 0 \sim 3.$	6 V	2.3~2.7	_	± 5.0	μA
3-State Our Off-State C		loz	V _{IN} = V _{IH} V _{OUT} = 0~		2.3~2.7	_	± 10.0	μΑ
Power Off Current	Leakage	lOFF	VIN, VOUT	= 0~3.6 V	0	_	10.0	μΑ
Quiescent S	Supply		$V_{IN} = V_{CC}$	or GND	2.3~2.7	_	20.0	
Current		lcc	$V_{CC} \leq (V_{IN})$	<mark>∖</mark> , V _{OUT}) ≦ 3.6 V	2.3~2.7	-	±20.0	μΑ

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = $-40 \sim 85^{\circ}$ C, $1.8 V \leq V_{CC} < 2.3 V$)

PARA	METER	SYMBOL	TEST	CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT
Input	"H" Level	VIH			1.8~2.3	0.7 × V _{CC}		V
Voltage	"L" Level	VIL			1.8~2.3	_	0.2 × V _{CC}	v
Output "H" Level VOH	V _{OH}	V _{IN} =	l _{OH} = – 100 μA	1.8	V _{CC} - 0.2	_		
			V _{IH} or V _{IL}	$I_{OH} = -6 \text{mA}$	1.8	1.4	_	V
voltage	ltage "L" Level Vol	V _{IN} =	l _{OL} = 100 μA	1.8	_	0.2		
	L Level	V _{OL}	V _{IH} or V _{IL}	l _{OL} = 6 mA	1.8	_	0.3	
Input Leak	age Current	^I IN	$V_{IN} = 0 \sim 3.$	6 V	1.8	_	± 5.0	μA
3-State Out Off-State C		loz	V _{IN} = V _{IH} (V _{OUT} = 0~		1.8	_	± 10.0	μΑ
Power Off Leakage		VIN, VOUT	= 0~3.6 V	0		10.0	μΑ	
Quiescent S	Quiescent Supply		$V_{IN} = V_{CC}$	or GND	1.8		20.0	
Current		lcc	$V_{CC} \leq (V_{IN})$	Ⅰ, V _{OUT}) ≦ 3.6 V	1.8	_	±20.0	μΑ

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT
Mawimum Clask			1.8	100	—	
Maximum Clock	fMAX	(Fig.1, 2)	2.5 ± 0.2	200	_	MHz
Frequency			3.3 ± 0.3	250	_	
Proposition Dolou Time	4		1.8	1.5	8.4	
Propagation Delay Time (An-Yn)	^t pLH	(Fig.1, 2)	2.5 ± 0.2	0.8	4.2	ns
<u>(~</u> ,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	^t pHL		3.3 ± 0.3	0.6	3.3	
			1.8	2.0	9.2	
Propagation Delay Time (CK-Yn)	^t pLH	(Fig.1, 3)	2.5 ± 0.2	1.5	5.2	ns
(CK-TII)	^t pHL		3.3 ± 0.3	1.4	4.2	
Deservation Dalay Times	4		1.8	1.5	9.8	
Propagation Delay Time	^t pLH	(Fig.1, 4)	2.5 ± 0.2	0.8	4.9	ns
(LE-Yn)	^t pHL		3.3 ± 0.3	0.6	3.8	
Output Enable Time			1.8	1.5	9.8	
	^t pZL	(Fig.1, 5)	2.5 ± 0.2	0.8	4.9	ns
	^t pZH		3.3 ± 0.3	0.6	3.8	
			1.8	1.5	7.6	
Output Disable Time	^t pLZ	(Fig.1, 5)	2.5 ± 0.2	0.8	4.5	ns
	^t pHZ		3.3 ± 0.3	0.6	3.9	ns
			1.8	4.0	_	
Minimum Pulse Width	^t w (H)	(Fig.1, 3, 4)	2.5 ± 0.2	1.5	_	ns
	^t w (L)		3.3 ± 0.3	1.5	_	
			1.8	2.5	_	
Minimum Set-up Time	ts	(Fig.1, 3, 4)	2.5 ± 0.2	1.5	_	ns
(An-CK, An-LE)	_		3.3 ± 0.3	1.5	_	
			1.8	1.0	_	
Minimum Hold Time	th	(Fig.1, 3, 4)	2.5 ± 0.2	0.7	_	ns
(An-CK, An-LE)			3.3 ± 0.3	0.7	_	
			1.8	—	0.5	
Output to Output Skew	tosLH	(Note 12)	2.5 ± 0.2		0.5	ns
	tosHL		3.3 ± 0.3	_	0.5	

AC characteristics (Ta = $-40 \sim 85^{\circ}$ C, Input t_r = t_f = 2.0 ns, C_L = 30 pF, R_L = 500 Ω)

(Note 12) : Parameter guaranteed by design.

 $(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT
Propagation Delay Time (An-Yn) (Note 13)	^t pLH ^t pHL	(Fig.1, 2)	3.3 ± 0.15	0.9	2.0	ns
Propagation Delay Time (CK-Yn) (Note 13)	^t pLH ^t pHL	(Fig.1, 3)	3.3 ± 0.15	1.5	2.9	ns
Propagation Delay Time (LE-Yn) (Note 13)	^t pLH ^t pHL	(Fig.1, 4)	3.3 ± 0.15	0.7	2.6	ns
Output Enable Time (Note 13)	^t pZL ^t pZH	(Fig.1, 5)	3.3 ± 0.15	0.7	2.6	ns
Output Disable Time (Note 13)	^t pLZ ^t pHZ	(Fig.1, 5)	3.3 ± 0.15	0.7	2.7	ns
Minimum Set-up Time (An-CK, An-LE) (Note 13)	ts	(Fig.1, 3, 4)	3.3 ± 0.15	1.5		ns
Minimum Hold Time (An-CK, An-LE) (Note 13)	^t h	(Fig.1, 3, 4)	3.3 ± 0.15	0.7	_	ns

AC characteristics (Ta = 0~85°C, Input $t_r = t_f = 2.0 \text{ ns}$, $C_L = 0 \text{ pF}$, $R_L = 500 \Omega$)

(Note 13) : TOSHIBA SPICE simulation data.

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT
Propagation Delay Time (An-Yn)	^t pLH ^t pHL	(Fig.1, 2)	3.3 ± 0.15	1.0	3.6	ns
Propagation Delay Time (CK-Yn)	^t pLH ^t pHL	(Fig.1, 3)	3.3 ± 0.15	1.7	4.5	ns
Propagation Delay Time (LE-Yn)	^t pLH ^t pHL	(Fig.1, 4)	3.3 ± 0.15	1.0	4.1	ns
Output Enable Time	^t pZL ^t pZH	(Fig.1, 5)	3.3 ± 0.15	1.0	4.1	ns
Output Disable Time	^t pLZ ^t pHZ	(Fig.1, 5)	3.3 ± 0.15	1.0	4.2	ns
Minimum Set-up Time (An-CK, An-LE)	ts	(Fig.1, 3, 4)	3.3 ± 0.15	1.5		ns
Minimum Hold Time (An-CK, An-LE)	t _h	(Fig.1, 3, 4)	3.3 ± 0.15	0.7		ns

AC characteristics (Ta = $0 \sim 85^{\circ}$ C, Input t_r = t_f = 2.0 ns, C_L = 50 pF, R_L = 500 Ω)

<u>TOSHIBA</u>

PARAMETER	SYMBOL	TEST CONDITIO	N	V _{CC} (V)	TYP.	UNIT
Quist Quitput Mavimum		V _{IH} = 1.8 V, V _{IL} = 0 V	(Note 14)	1.8	0.35	
Quiet Output Maximum	VOLP	$V_{IH} = 2.5 V, V_{IL} = 0 V$	(Note 14)	2.5	0.7	V
Dynamic V _{OL}		$V_{IH} = 3.3 V, V_{IL} = 0 V$	(Note 14)	3.3	0.9	
Quiat Qutput Minimum		$V_{IH} = 1.8 V, V_{IL} = 0 V$	(Note 14)	1.8	- 0.35	
Quiet Output Minimum Dynamic V _{OI}	VOLV	V _{IH} = 2.5 V, V _{IL} = 0 V	(Note 14)	2.5	- 0.7	V
		V _{IH} = 3.3 V, V _{IL} = 0 V	(Note 14)	3.3	- 0.9	
Quiet Qutrut Minimum		V _{IH} = 1.8 V, V _{IL} = 0 V	(Note 14)	1.8	1.3	
Quiet Output Minimum Dynamic V _{OH}	Vонv	V _{IH} = 2.5 V, V _{IL} = 0 V	(Note 14)	2.5	1.7	V
		V _{IH} = 3.3 V, V _{IL} = 0 V	(Note 14)	3.3	2.0	

Dynamic switching characteristics (Ta = 25° C, Input t_r = t_f = 2.0 ns, C_L = 30 pF)

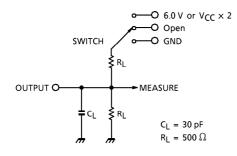
(Note 14) : Parameter guaranteed by design.

Capacitive characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Input Capacitance	C _{IN}		1.8, 2.5, 3.3	6	рF
Output Capacitance	COUT		1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10 MHz (Note 15)	1.8, 2.5, 3.3	20	pF

(Note 15) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation : I_{CC} (opr.) = C_{PD} · V_{CC} · f_{IN} + I_{CC} / 18 (per bit)

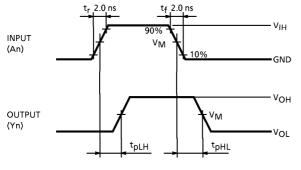
Fig.1 Test circuit



PARAMETER	SWITCH		
t _{pLH} , t _{pHL}	Open		
t _{pLZ} , t _{pZL}	6.0 V	@V _{CC} = 3.3 ± 0.3 V @V _{CC} = 2.5 ± 0.2 V	
	V _{CC} x 2	$@V_{CC} = 2.5 \pm 0.2 V$	
		@V _{CC} = 1.8 V	
t _{pHZ} , t _{pZH}	GND		

AC WAVEFORM

Fig.2 t_{pLH}, t_{pHL}



SYMBOL	V _{CC}			
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V	
VIH	2.7 V	V _{CC}	V _{CC}	
VM	1.5 V	V _{CC} / 2	V _{CC} / 2	
VX	V _{OL} + 0.3 V	V _{OL} + 0.15 V	V _{OL} + 0.15 V	
VY	V _{OH} – 0.3 V	V _{OH} – 0.15 V	V _{OH} – 0.15 V	

Fig.3 t_{pLH} , t_{pHL} , t_w , t_s , t_h

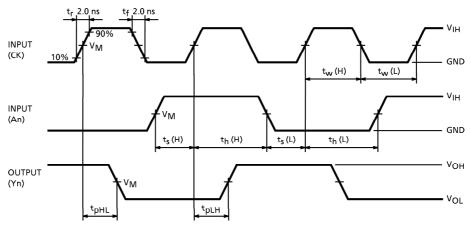


Fig.4 tpLH, tpHL, tw, ts, th

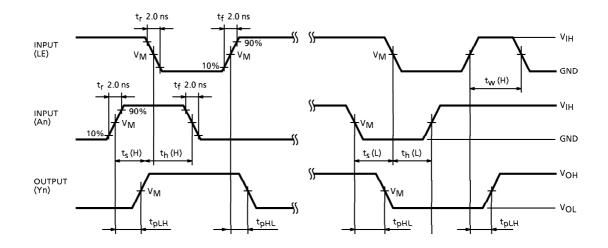
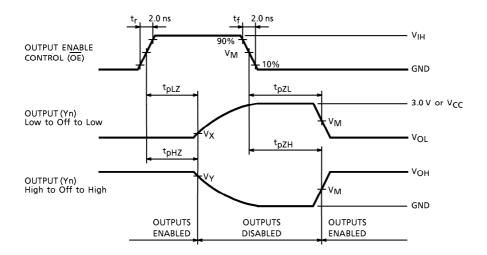
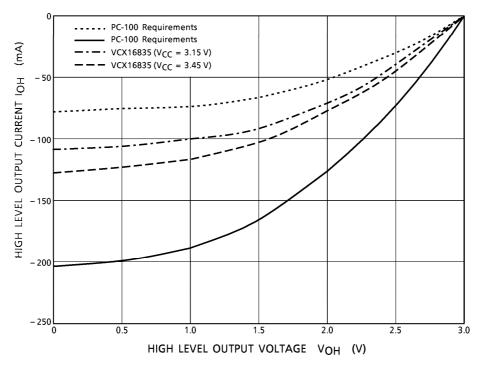


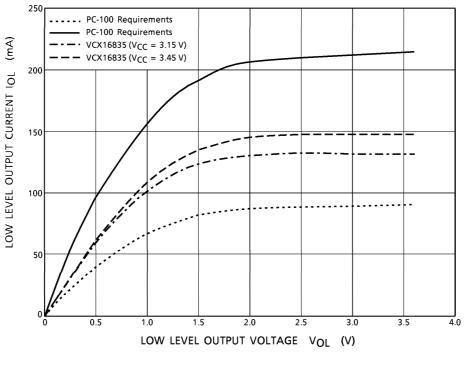
Fig.5 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}



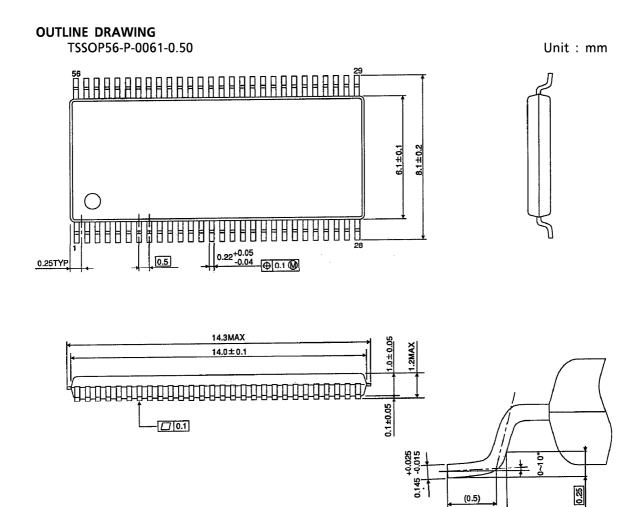
IBIS CHARACTERISTICS (Typ.)











Weight: 0.25 g (Typ.)

0.45~ 0.75

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