

TOSHIBA

TC74VCXR162501FT

ADVANCE
INFORMATION

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VCXR162501FT

LOW-VOLTAGE 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3.6 V TOLERANT INPUTS AND OUTPUTS

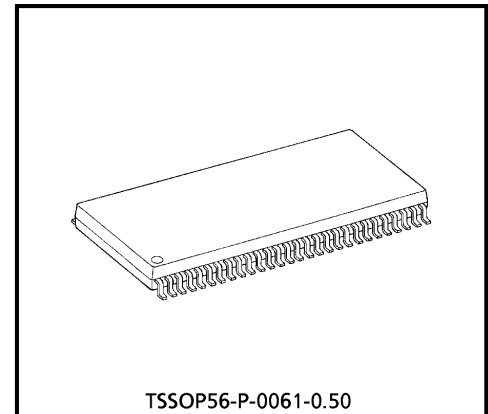
The TC74VCXR162501FT is a high performance CMOS 18-bit UNIVERSAL BUS TRANSCEIVER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CKAB and CKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CKAB is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch / flip-flop on the low-to-high transition of CKAB.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and CKBA. When the $\overline{OE}$ input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.

The 26- Ω series resistor helps reducing output overshoot and undershoot without external resistor. All inputs are equipped with protection circuits against static discharge.



Weight : 0.25 g (Typ.)

FEATURES

- 26- Ω Series Resistors on Outputs.
- Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6 \text{ V}$
- High Speed Operation : $t_{pd} = 3.8 \text{ ns (max)}$ at $V_{CC} = 3.0 \sim 3.6 \text{ V}$
 $t_{pd} = 4.9 \text{ ns (max)}$ at $V_{CC} = 2.3 \sim 2.7 \text{ V}$
 $t_{pd} = 9.8 \text{ ns (max)}$ at $V_{CC} = 1.8 \text{ V}$
- 3.6 V Tolerant inputs and outputs.
- Output Current : $I_{OH} / I_{OL} = \pm 12 \text{ mA (min)}$ at $V_{CC} = 3.0 \text{ V}$
 $I_{OH} / I_{OL} = \pm 8 \text{ mA (min)}$ at $V_{CC} = 2.3 \text{ V}$
 $I_{OH} / I_{OL} = \pm 4 \text{ mA (min)}$ at $V_{CC} = 1.8 \text{ V}$
- Latch-up Performance : $\pm 300 \text{ mA}$
- ESD Performance : Human Body Model $> \pm 2000 \text{ V}$
Machine Model $> \pm 200 \text{ V}$
- Package : TSSOP
(Thin Shrink Small Outline Package)
- Bidirectional interface between 2.5 V and 3.3 V signals.
- Power Down Protection is provided on all inputs and outputs.
- Supports live insertion / withdrawal (Note 3)

980910EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

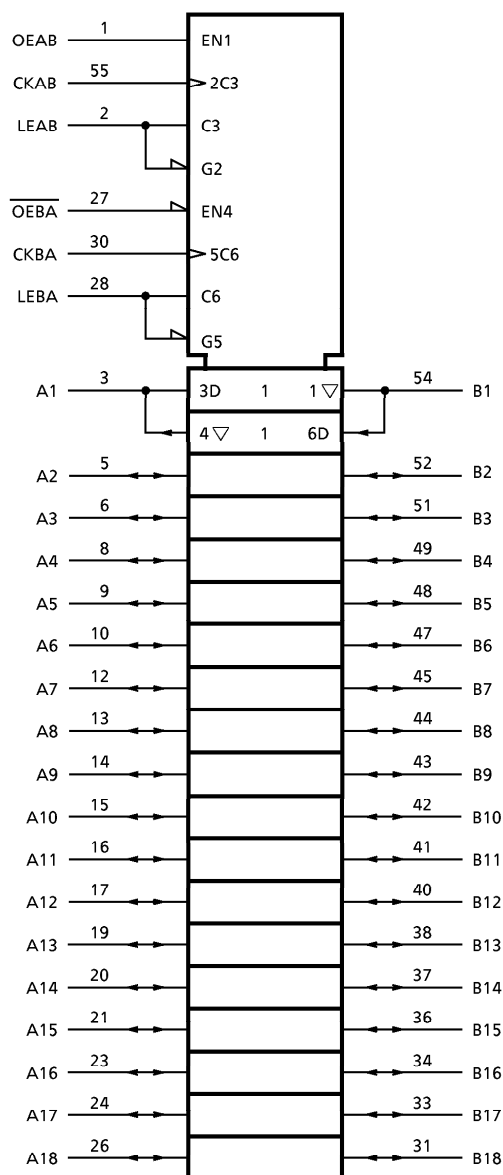
- (Note 1) : Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
- (Note 2) : All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.
- (Note 3) : To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

PIN ASSIGNMENT

OEAB	1	56	GND
LEAB	2	55	CKAB
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V _{CC}	7	50	V _{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	B9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
V _{CC}	22	35	V _{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
OEBA	27	30	CKBA
LEBA	28	29	GND

(TOP VIEW)

SYMBOL

**PRELIMINARY**

980910EBA2'

- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

TRUTH TABLE *

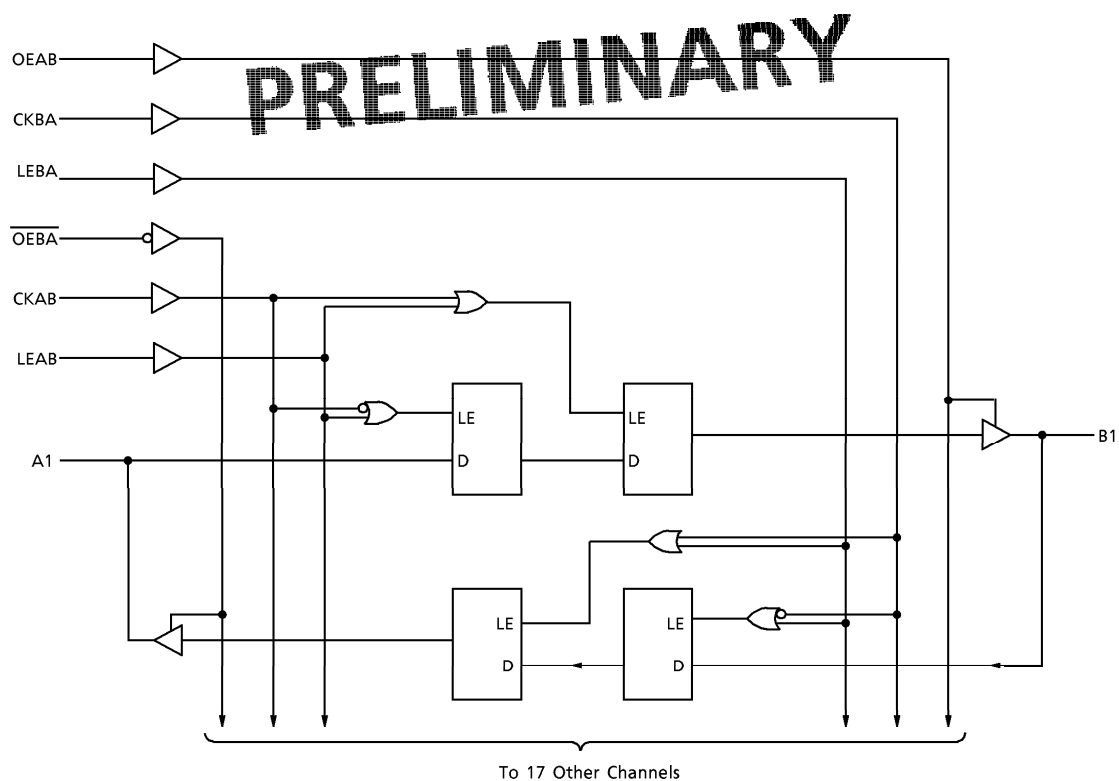
INPUTS				OUTPUTS
OEAB	LEAB	CKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	$\uparrow$	L	L
H	L	$\downarrow$	H	H
H	L	H	X	B0**
H	L	L	X	B0***

* A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and CKBA.

** Output level before the indicated steady-state input conditions were established, provided that CKAB was low before LEAB went low.

*** Output level before the indicated steady-state input conditions were established.

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	$-0.5 \sim 4.6$	V
DC Input Voltage (OEAB, $\overline{OEBA}$, LEAB, LEBA, CKAB, CKBA)	V_{IN}	$-0.5 \sim 4.6$	V
DC Bus I/O Voltage	$V_{I/O}$	$-0.5 \sim 4.6$ (Note 1)	V
		$-0.5 \sim V_{CC} + 0.5$ (Note 2)	
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	± 50 (Note 3)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} /Ground Current Per Supply Pin	I_{CC}/I_{GND}	± 100	mA
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

(Note 1) : Off-State

(Note 2) : High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 3) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$ **PRELIMINARY**

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	1.8~3.6	V
		1.2~3.6 (Note 4)	
Input Voltage (OEAB, $\overline{OEBA}$, LEAB, LEBA, CKAB, CKBA)	V_{IN}	$-0.3 \sim 3.6$	V
Bus I/O Voltage	$V_{I/O}$	0~3.6 (Note 5)	V
		0~ V_{CC} (Note 6)	
Output Current	I_{OH}/I_{OL}	± 12 (Note 7)	mA
		± 8 (Note 8)	
		± 4 (Note 9)	
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 10)	ns/V

(Note 4) : Data Retention Only

(Note 5) : Off-State

(Note 6) : High or Low State

(Note 7) : $V_{CC} = 3.0 \sim 3.6$ V(Note 8) : $V_{CC} = 2.3 \sim 2.7$ V(Note 9) : $V_{CC} = 1.8$ V(Note 10) : $V_{IN} = 0.8 \sim 2.0$ V, $V_{CC} = 3.0$ V

ELECTRICAL CHARACTERISTICS

DC characteristics ($T_a = -40\sim 85^\circ\text{C}$, $2.7\text{ V} < V_{CC} \leq 3.6\text{ V}$)

PARAMETER		SYMBOL	TEST CONDITION		V _{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V _{IH}			2.7~3.6	2.0	—	V
	"L" Level	V _{IL}			2.7~3.6	—	0.8	
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 100 μA	2.7~3.6	V _{CC} - 0.2	—	V
				I _{OH} = - 6 mA	2.7	2.2	—	
				I _{OH} = - 8 mA	3.0	2.4	—	
				I _{OH} = - 12 mA	3.0	2.2	—	
	"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.7~3.6	—	0.2	
				I _{OL} = 6 mA	2.7	—	0.4	
				I _{OL} = 8 mA	3.0	—	0.55	
				I _{OL} = 12 mA	3.0	—	0.8	
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6 V		2.7~3.6	—	± 5.0	μA
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6 V		2.7~3.6	—	± 10.0	μA
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6 V		0	—	10.0	μA
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		2.7~3.6	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V		2.7~3.6	—	± 20.0	
Increase In I _{CC} Per Input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6 V		2.7~3.6	—	750	μA

PRELIMINARY

ELECTRICAL CHARACTERISTICS

DC characteristics ($T_a = -40\sim 85^\circ\text{C}$, $2.3\text{ V} \leq V_{CC} \leq 2.7\text{ V}$)

PARAMETER		SYMBOL	TEST CONDITION		V _{CC} (V)	MIN	MAX	UNIT
Input Voltage	"H" Level	V _{IH}			2.3~2.7	1.6	—	V
	"L" Level	V _{IL}			2.3~2.7	—	0.7	
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -100 μA	2.3~2.7	V _{CC} - 0.2	—	V
				I _{OH} = -4 mA	2.3	2.0	—	
				I _{OH} = -6 mA	2.3	1.8	—	
				I _{OH} = -8 mA	2.3	1.7	—	
	"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	2.3~2.7	—	0.2	
				I _{OL} = 6 mA	2.3	—	0.4	
				I _{OL} = 8 mA	2.3	—	0.6	
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6 V	2.3~2.7	—	± 5.0	μA	
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6 V	2.3~2.7	—	± 10.0	μA	
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6 V	0	—	10.0	μA	
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		2.3~2.7	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V _{CC}		2.3~2.7	—	± 20.0	

ELECTRICAL CHARACTERISTICS

DC characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $1.8\text{ V} \leq V_{CC} < 2.3\text{ V}$)

PARAMETER		SYMBOL	TEST CONDITION			MIN	MAX	UNIT	
			V _{CC} (V)						
Input Voltage	“H” Level	V _{IH}	1.8~2.3			0.7 × V _{CC}	—	V	
	“L” Level	V _{IL}	1.8~2.3			—	0.2 × V _{CC}		
Output Voltage	“H” Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = − 100 μA	1.8	V _{CC} − 0.2	—	V	
				I _{OH} = − 4 mA	1.8	1.4	—		
	“L” Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.8	—	0.2		
				I _{OL} = 4 mA	1.8	—	0.3		
Input Leakage Current		I _{IN}	V _{IN} = 0~3.6V			1.8	—	± 5.0	μA
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~3.6 V			1.8	—	± 10.0	μA
Power Off Leakage Current		I _{OFF}	V _{IN} , V _{OUT} = 0~3.6 V			0	—	10.0	μA
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND			1.8	—	20.0	μA
			V _{CC} ≤ (V _{IN} , V _{OUT}) ≤ 3.6 V			1.8	—	± 20.0	

PRELIMINARY

AC characteristics (Ta = -40~85°C, Input $t_r = t_f = 2.0$ ns, $C_L = 30$ pF, $R_L = 500 \Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	MIN	MAX	UNIT
Maximum Clock Frequency	f _{MAX}	(Fig.1, 2)	1.8	100	—	MHz
			2.5 ± 0.2	200	—	
			3.3 ± 0.3	250	—	
Propagation Delay Time (An, Bn-Bn, An)	t _{pLH} t _{pHL}	(Fig.1, 2)	1.8	1.5	9.8	ns
			2.5 ± 0.2	1.0	4.9	
			3.3 ± 0.3	0.8	3.8	
Propagation Delay Time (CKAB, CKBA-Bn, An)	t _{pLH} t _{pHL}	(Fig.1, 5)	1.8	1.5	9.8	ns
			2.5 ± 0.2	1.0	5.8	
			3.3 ± 0.3	0.8	4.4	
Propagation Delay Time (LEAB, LEBA-Bn, An)	t _{pLH} t _{pHL}	(Fig.1, 2)	1.8	1.5	9.8	ns
			2.5 ± 0.2	1.0	6.3	
			3.3 ± 0.3	0.8	4.7	
Output Enable Time (OEAB, OEBA-Bn, An)	t _{pZL} t _{pZH}	(Fig.1, 3, 4)	1.8	1.5	9.8	ns
			2.5 ± 0.2	1.0	5.9	
			3.3 ± 0.3	0.8	4.3	
Output Disable Time (OEAB, OEBA-Bn, An)	t _{pLZ} t _{pHZ}	(Fig.1, 3, 4)	1.8	1.5	8.8	ns
			2.5 ± 0.2	1.0	4.9	
			3.3 ± 0.3	0.8	4.3	
Minimum Pulse Width	t _w (H) t _w (L)	(Fig.1, 5)	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum Set-up Time	t _s	(Fig.1, 5)	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum Hold Time	t _h	(Fig.1, 5)	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to Output Skew	t _{osLH} t _{osHL}	(Note 11)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.

(Note 11) : Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

PRELIMINARY

Dynamic switching characteristics (Ta = 25°C, Input $t_r = t_f = 2.0$ ns, $C_L = 30$ pF)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	V _{IH} = 1.8 V, V _{IL} = 0 V (Note 12)	1.8	0.15	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note 12)	2.5	0.25	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note 12)	3.3	0.35	
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	V _{IH} = 1.8 V, V _{IL} = 0 V (Note 12)	1.8	-0.15	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note 12)	2.5	-0.25	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note 12)	3.3	-0.35	
Quiet Output Minimum Dynamic V _{OH}	V _{OHV}	V _{IH} = 1.8 V, V _{IL} = 0 V (Note 12)	1.8	1.55	V
		V _{IH} = 2.5 V, V _{IL} = 0 V (Note 12)	2.5	2.05	
		V _{IH} = 3.3 V, V _{IL} = 0 V (Note 12)	3.3	2.65	

(Note 12) : Parameter guaranteed by design.

Capacitive characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Input Capacitance	C _{IN}	—	1.8, 2.5, 3.3	6	pF
Bus I/O Capacitance	C _{I/O}		1.8, 2.5, 3.3	7	pF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10 MHz (Note 13)	1.8, 2.5, 3.3	20	pF

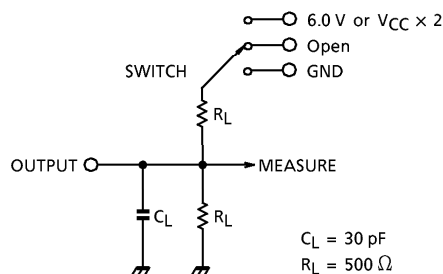
(Note 13) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/18 \text{ (per bit)}$$

PRELIMINARY

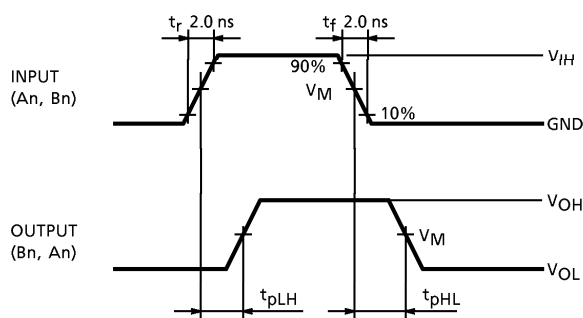
TEST CIRCUIT
Fig.1



PARAMETER	SWITCH
t_{pLH} , t_{pHL}	Open
t_{pLZ} , t_{pZL}	6.0 V @ $V_{CC} = 3.3 \pm 0.3 \text{ V}$ $V_{CC} \times 2$ @ $V_{CC} = 2.5 \pm 0.2 \text{ V}$ @ $V_{CC} = 1.8 \text{ V}$
t_{pHZ} , t_{pZH}	GND

PRELIMINARY

AC WAVEFORM
Fig.2 t_{pLH} , t_{pHL}



SYMBOL	V_{CC}		
	$3.3 \pm 0.3 \text{ V}$	$2.5 \pm 0.2 \text{ V}$	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC} / 2$	$V_{CC} / 2$
V_X	$V_{OL} + 0.3 \text{ V}$	$V_{OL} + 0.15 \text{ V}$	$V_{OL} + 0.15 \text{ V}$
V_Y	$V_{OH} - 0.3 \text{ V}$	$V_{OH} - 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$

Fig.3 t_{pLH} , t_{pHL} , t_w , t_s , t_h

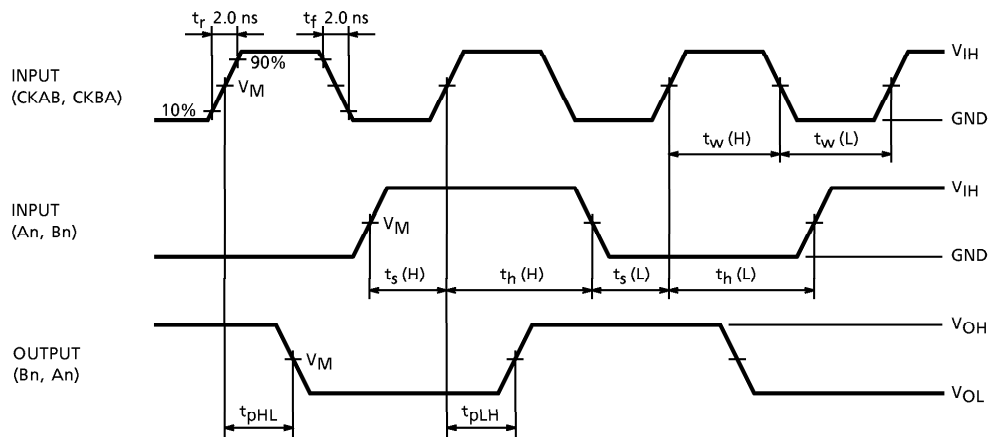
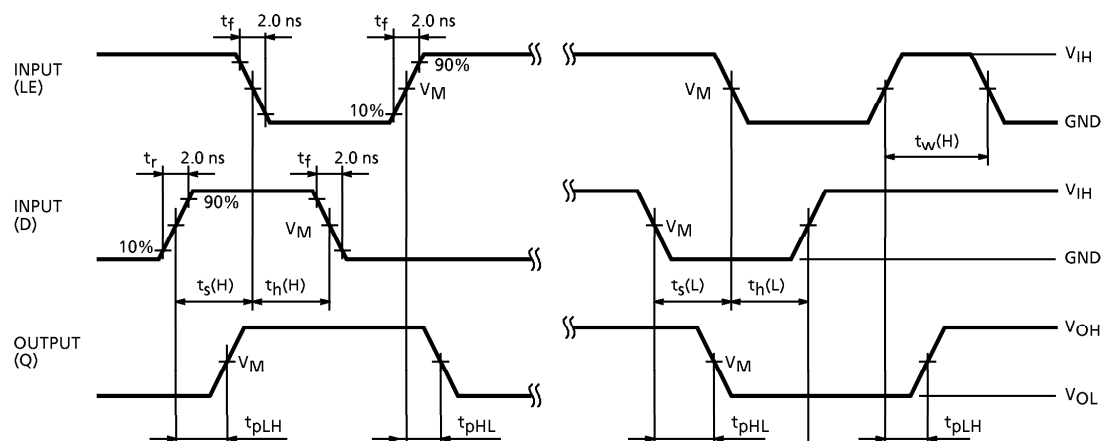
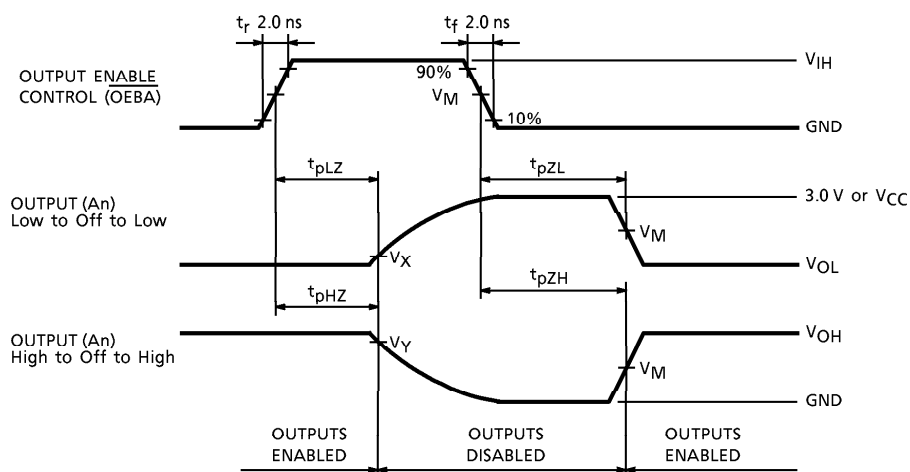
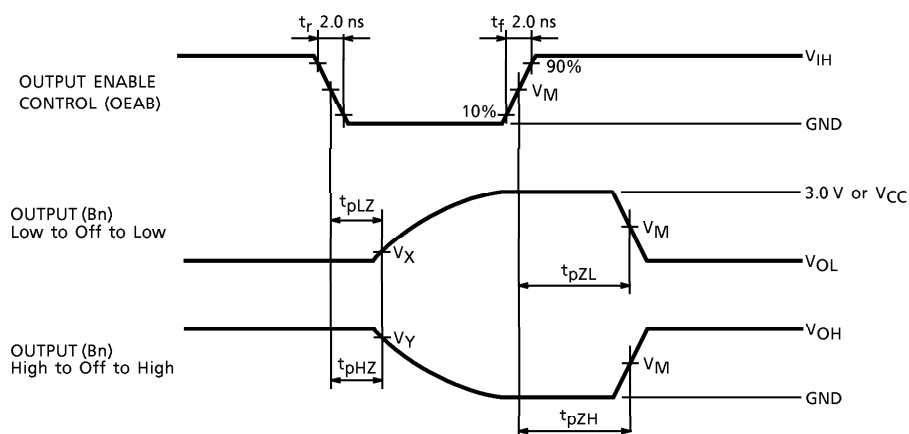
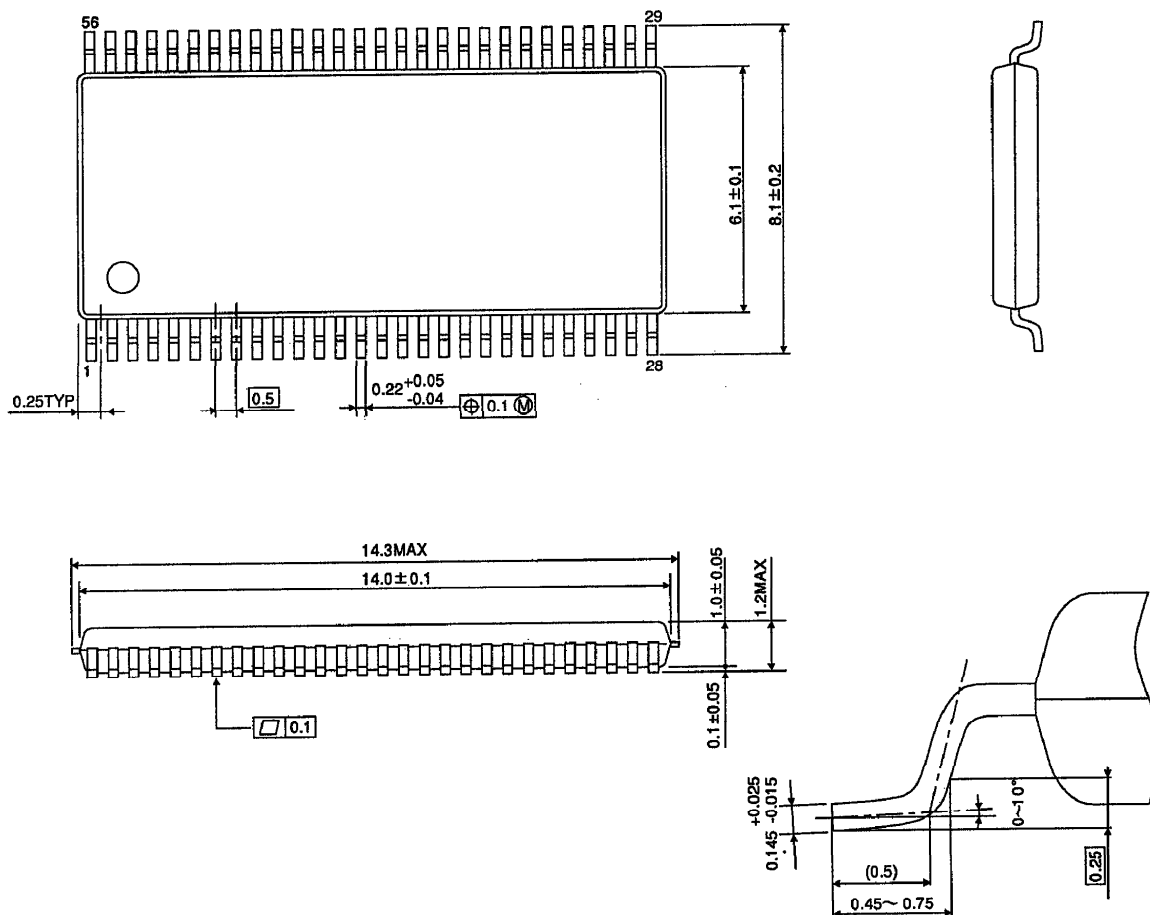


Fig.4 t_{pLH} , t_{pHL} , t_w , t_s , t_h Fig.5 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH} Fig.6 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH} 

OUTLINE DRAWING

TSSOP56-P-0061-0.50

Unit : mm



Weight : 0.25 g (Typ.)

PRELIMINARY

Copyright Each Manufacturing Company.

All Datasheets cannot be modified without permission.

This datasheet has been download from :

www.AllDataSheet.com

100% Free DataSheet Search Site.

Free Download.

No Register.

Fast Search System.

www.AllDataSheet.com