TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

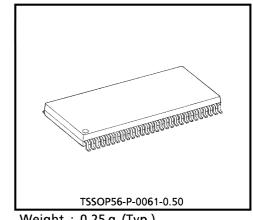
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LOW-VOLTAGE 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3.6 V TOLERANT INPUTS AND OUTPUTS

The TC74VCXR162600FT is a high performance CMOS 18bit UNIVERSAL BUS TRANSCEIVER. Designed for use in 1.8, 2.5 or 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

It is also designed with over voltage tolerant inputs and outputs up to 3.6 V.

Data flow in each direction is controlled by outputenable (OEAB and OEBA), latch-enable (LEAB and LEBA), and clock (CKAB and CKBA) inputs. The clock can be controlled by the clock-enable (CKENAB and CKENBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CKAB is held at a high or low logic level. If LEAB is low, the A-bus data is stored in the latch / flip-flop on the high-to-low transition of CKAB.



Weight : 0.25 g (Typ.)

Data flow for B to A is similar to that of A to B but uses OEBA, LEBA, CKBA, and CKENBA. When the \overline{OE} input is high, the outputs are in a high impedance state. This device is designed to be used with 3-state memory address drivers, etc.

The 26- Ω series resistor helps reducing output overshoot and undershoot without external resistor. All inputs are equipped with protection circuits against static discharge.

FEATURES

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- 26-Ω Series Resistors on Outputs.
- Low Voltage Operation : $V_{CC} = 1.8 \sim 3.6V$

٠	High Speed Operation	: $t_{pd} = 3.8 \text{ ns} (\text{max}) \text{ at } V_{CC} = 3.0 \sim 3.6 \text{ V}$
		$t_{pd} = 5.1 \text{ ns} (\text{max}) \text{ at } V_{CC} = 2.3 \sim 2.7 \text{ V}$
		$t_{pd} = 9.8 \text{ ns} (\text{max}) \text{ at } V_{CC} = 1.8 \text{ V}$
٠	3.6 V Tolerant inputs ar	nd outputs.
٠	Output Current	$: I_{OH} / I_{OL} = \pm 12 \text{ mA} (min) \text{ at } V_{CC} = 3.0 \text{ V}$
		$: I_{OH} / I_{OL} = \pm 8 \text{ mA} (\text{min}) \text{ at } V_{CC} = 2.3 \text{ V}$
		$: I_{OH} / I_{OL} = \pm 4 \text{ mA} (\text{min}) \text{ at } V_{CC} = 1.8 \text{ V}$
	Latch up Parformanco	$+ 200 m \Lambda$

- Latch-up Performance : ± 300 mA
- ESD Performance : Human Body Model > ±2000 V : Machine Model > $\pm 200 V$
- : TSSOP (Thin Shrink Small Outline Package) Package
- Bidirectional interface between 2.5 V and 3.3 V signals.
- Power Down Protection is provided on all inputs and outputs.
- Supports live insertion / withdrawal (Note 3)

TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

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- (Note 1) : Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
- (Note 2) : All floating (high impedance) bus terminal must have their input level fixed by means of pull up or pull down resistors.
- (Note 3) : To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

PIN ASSIGNMENT

OEAB	1	56	CKENAB
LEAB	2	55	СКАВ
A1	3	54	B1
GND	4	53	GND
A2	5	52	B2
A3	6	51	B3
V _{CC}	7	50	V _{CC}
A4	8	49	B4
A5	9	48	B5
A6	10	47	B6
GND	11	46	GND
A7	12	45	B7
A8	13	44	B8
A9	14	43	В9
A10	15	42	B10
A11	16	41	B11
A12	17	40	B12
GND	18	39	GND
A13	19	38	B13
A14	20	37	B14
A15	21	36	B15
Vcc	22	35	V _{CC}
A16	23	34	B16
A17	24	33	B17
GND	25	32	GND
A18	26	31	B18
OEBA	27	30	СКВА
LEBA	28	29	CKENBA
T)	OP VIEW)	-	

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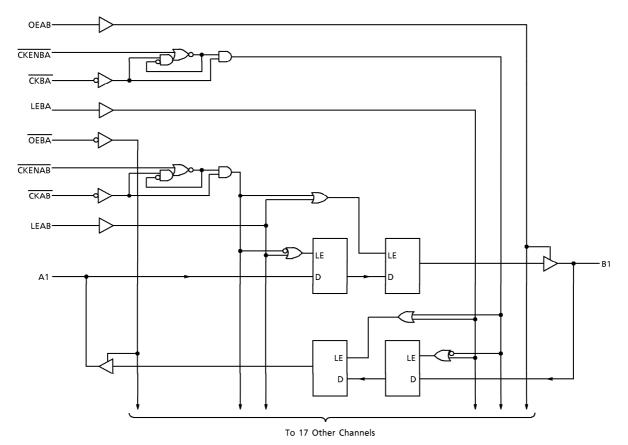
TRUTH TABLE *

	INPUTS								
CKENAB	OEAB	LEAB	CKAB	А	В				
Х	Н	Х	Х	Х	Z				
Х	L	Н	Х	L	L				
Х	L	Н	Х	Н	Н				
Н	L	L	Х	Х	B0**				
Н	L	L	Х	Х	B0**				
L	L	L	7	L	L				
L	L	L	7	Н	Н				
L	L	L	Н	Х	B0**				
L	L	L	L	Х	B0**				

* A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CKBA, and CKNBA.

** Output level before the indicated steady-state input conditions were established, provided that CKAB was low or high before LEAB went low.

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V _{CC}	-0.5~4.6	V
DC Input Voltage (OEAB, OEBA, LEAB, LEBA, CKAB, CKBA, CKENAB, CKENBA)	V _{IN}	-0.5~4.6	V
	Maria	-0.5~4.6 (Note 1)	V
DC Bus I/O Voltage	VI/O	-0.5~V _{CC} + 0.5 (Note 2)	v
Input Diode Current	IК	- 50	mA
Output Diode Current	ΙΟΚ	±50 (Note 3)	mA
DC Output Current	ΙΟυτ	± 50	mA
Power Dissipation	PD	400	mW
DC V _{CC} /Ground Current Per Supply Pin	ICC / IGND	± 100	mA
Storage Temperature	T _{stg}	- 65~150	°C

(Note 1) : Off-State

(Note 2) : High or Low State. IOUT absolute maximum rating must be observed.

(Note 3) : $V_{OUT} < GND$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	Vac	1.8~3.6	v
supply voltage	Vcc	1.2~3.6 (Note 4)	v
Input Voltage (OEAB, OEBA, LEAB, LEBA, CKAB, CKBA)	VIN	-0.3~3.6	V
	Nu i a	0~3.6 (Note 5)	v
Bus I/O Voltage	VI/O	0~V _{CC} (Note 6)	
		±12 (Note 7)	
Output Current	IOH/IOL	±8 (Note 8)	mA
		±4 (Note 9)	
Operating Temperature	T _{opr}	- 40~85	°C
Input Rise And Fall Time	dt/dv	0~10 (Note 10)	ns / V

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = $-40 \sim 85^{\circ}$ C, 2.7 V < V_{CC} \leq 3.6 V)

PARA	METER	SYMBOL	TEST	CONDITION	V _{CC} (V)	MIN	MAX	UNIT	
Input	"H" Level	VIH			2.7~3.6	2.0	-	V	
Voltage	"L" Level	VIL			2.7~3.6	_	0.8	v	
				I _{OH} = −100 μA	2.7~3.6	V _{CC} - 0.2	-		
	"H" Level	∨он	VIN =	$I_{OH} = -6 \text{mA}$	2.7	2.2	_		
Output			VIH or VIL	$I_{OH} = -8 \text{mA}$	3.0	2.4	—		
				$I_{OH} = -12 \text{ mA}$	3.0	2.2	—	V	
Voltage	"L" Level VOI		V _{IN} = V _{IH} or V _{IL}	l _{OL} = 100 μA	2.7~3.6	—	0.2		
		V _{OL}		I _{OL} = 6 mA	2.7	_	0.4		
	LLEVEI	VOL		V _{IH} or V _{IL}	VIH or VIL	I _{OL} = 8 mA	3.0		0.55
				I _{OL} = 12 mA	3.0	_	0.8		
Input Leaka	ge Current	IIN	$V_{IN} = 0 \sim 3.$	6 V	2.7~3.6		± 5.0	μA	
3-State Out Off-State Co	urrent	loz	V _{IN} = V _{IH} V _{OUT} = 0~		2.7~3.6	_	± 10.0	μΑ	
Power Off Leakage Current		loff	V _{IN} , V _{OUT}	V _{IN} , V _{OUT} = 0~3.6 V		_	10.0	μΑ	
Quiescent S	upply		$V_{IN} = V_{CC}$	or GND	2.7~3.6		20.0		
Current		lcc	$V_{CC} \leq (V_{IN})$	I, V _{OUT}) ≦ 3.6 V	2.7~3.6	—	±20.0	μΑ	
Increase In Input	ICC Per	∆ا∠	V _{IH} = V _{CC}	– 0.6 V	2.7~3.6		750	μΑ	

ELECTRICAL CHARACTERISTICS DC characteristics (Ta = $-40{\sim}85^\circ\text{C},~2.3~\text{V} \leq \text{V}_{CC} \leq 2.7~\text{V})$

PARAMETER SYI		SYMBOL	TEST	TEST CONDITION		MIN	MAX	UNIT																	
Input	"H" Level	VIH			2.3~2.7	1.6	_	v																	
Voltage	"L" Level	VIL			2.3~2.7	_	0.7	v																	
				I _{OH} = -100 μA	2.3~2.7	V _{CC} - 0.2																			
	"H" Level	∨он	V _{IN} =	$I_{OH} = -4 mA$	2.3	2.0																			
Output			VIH or VIL	$I_{OH} = -6 \text{mA}$	2.3	1.8	_	v																	
Voltage				$I_{OH} = -8 \text{mA}$	2.3	1.7	_																		
			V _{IN} = V _{IH} or V _{IL}	l _{OL} = 100 μA	2.3~2.7	_	0.2																		
	"L" Level	VOL																			I _{OL} = 6 mA	2.3	_	0.4	
					I _{OL} = 8 mA	2.3	_	0.6																	
Input Leak	age Current	^I IN	V _{IN} = 0~3.6 V		2.3~2.7	_	± 5.0	μA																	
3-State Output Off-State Current		loz		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = 0 \sim 3.6 \text{ V}$		_	± 10.0	μΑ																	
Power Off Leakage Current		lOFF	V _{IN} , V _{OUT} = 0~3.6 V		0		10.0	μΑ																	
Quiescent	Quiescent Supply		V _{IN} = V _{CC} or GND		2.3~2.7	_	20.0																		
Current		lcc	$V_{CC} \leq (V_{IN})$	l, V _{OUT}) ≦ 3.6 V	2.3~2.7	_	±20.0	μΑ																	

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ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = $-40 \sim 85^{\circ}$ C, $1.8 V \leq V_{CC} < 2.3 V$)

PARA	METER	SYMBOL	TEST	CONDITION	V _{CC} (V)	MIN	MAX	UNIT
Input	"H" Level	VIH				0.7 × V _{CC}		V
Voltage	"L" Level	VIL				_	0.2 × V _{CC}	v
	"H" Level VOH	V _{IN} =	I _{OH} = -100 μA	1.8	V _{CC} – 0.2	_		
Output Voltage		V _{IH} or V _{IL}	$I_{OH} = -4 \text{mA}$	1.8	1.4	_	V	
voltage	"L" Level	Vai	V _{IN} =	l _{OL} = 100 μA	1.8		0.2	
	L Level	V _{OL}	V _{IH} or V _{IL}	I _{OL} = 4 mA	1.8	_	0.3	
Input Leak	age Current	l _{IN}	V _{IN} = 0∼3.	6 V	1.8	_	± 5.0	μA
	3-State Output Off-State Current		V _{IN} = V _{IH} (V _{OUT} = 0~		1.8		± 10.0	μΑ
Power Off Leakage Current		loff	V _{IN} , V _{OUT} = 0~3.6 V		0		10.0	μΑ
Quiescent S	Quiescent Supply		$V_{IN} = V_{CC}$	or GND	1.8		20.0	
Current		lcc	$ V_{CC} \leq (V_{IN})$	l, V _{OUT}) ≦ 3.6 V	1.8	_	±20.0	μΑ

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PARAMETER	SYMBOL		ION	V _{CC} (V)	MIN	МАХ	UNIT
				1.8	100	_	
Maximum Clock	fMAX	(Fig.1, 3)		2.5 ± 0.2	200	_	MHz
Frequency				3.3 ± 0.3	250	_	
Preneration Delay Time	4			1.8	1.5	9.8	
Propagation Delay Time (An, Bn-Bn, An)	^t pLH	(Fig.1, 2)		2.5 ± 0.2	1.0	5.1	ns
	^t pHL			3.3 ± 0.3	0.8	3.8	
Propagation Delay Time	+			1.8	1.5	9.8	
(CKAB, CKBA-Bn, An)	tpLH	(Fig.1, 3)		2.5 ± 0.2	1.0	6.4	ns
	^t pHL			3.3 ± 0.3	0.8	4.4	
Propagation Delay Time	+			1.8	1.5	9.8	
(LEAB, LEBA-Bn, An)	^t pLH	(Fig.1, 4)		2.5 ± 0.2	1.0	5.8	ns
(LEAD, LEDA-DII, AII)	^t pHL		3.3 ± 0.3	0.8	4.4		
Output Enable Time	+			1.8	1.5	9.8	
(OEAB, OEBA-Bn, An)	^t pZL	(Fig.1, 6)		2.5 ± 0.2	1.0	5.9	ns
	^t pZH		3.3 ± 0.3	0.8	4.3		
Output Disable Time	+			1.8	1.5	8.8	
(OEAB, OEBA-Bn, An)	^t pLZ	(Fig.1, 6)		2.5 ± 0.2	1.0	4.9	ns
	^t pHZ		3.3 ± 0.3	0.8	4.3		
	+ 4.0		1.8	4.0	_		
Minimum Pulse Width	^t w (H)	(Fig.1, 3, 4)		2.5 ± 0.2	1.5	—	ns
	^t w (L)			3.3 ± 0.3	1.5	—	
				1.8	2.5	_	
Minimum Set-up Time	ts	(Fig.1, 3, 4, 5)		2.5 ± 0.2	1.5		ns
				3.3 ± 0.3	1.5	—	
				1.8	2.0		
Minimum Hold Time	t _h	(Fig.1, 3, 4, 5)		2.5 ± 0.2	1.5		ns
				3.3 ± 0.3	1.0	—	
	+			1.8	_	0.5	
Output to Output Skew	t _{osLH}		(Note 11)	2.5 ± 0.2	_	0.5	ns
	tosHL			3.3 ± 0.3	_	0.5	

AC characteristics (Ta = $-40 \sim 85^{\circ}$ C, Input t_r = t_f = 2.0 ns, C_L = 30 pF, R_L = 500 Ω)

For $C_L = 50 \text{ pF}$, add approximately 300 ps to the AC maximum specification.

(Note 11) : Parameter guaranteed by design. $(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$

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PARAMETER	SYMBOL	TEST CONDITIC	DN	V _{CC} (V)	TYP.	UNIT
Quiet Output Maximum		$V_{IH} = 1.8 V, V_{IL} = 0 V$	(Note 12)	1.8	0.15	
Dynamic V _{OL}	VOLP	$V_{IH} = 2.5 V, V_{IL} = 0 V$	(Note 12)	2.5	0.25	V
		V _{IH} = 3.3 V, V _{IL} = 0 V	(Note 12)	3.3	0.35	
Quiet Qutnut Minimum		$V_{IH} = 1.8 V, V_{IL} = 0 V$	(Note 12)	1.8	- 0.15	
Quiet Output Minimum Dynamic V _{OI}	VOLV	V _{IH} = 2.5 V, V _{IL} = 0 V	(Note 12)	2.5	- 0.25	V
		V _{IH} = 3.3 V, V _{IL} = 0 V	(Note 12)	3.3	- 0.35	
		V _{IH} = 1.8 V, V _{IL} = 0 V	(Note 12)	1.8	1.55	
Quiet Output Minimum Dynamic V _{OH}	VOHV	V _{IH} = 2.5 V, V _{IL} = 0 V	(Note 12)	2.5	2.05	V
	2	V _{IH} = 3.3 V, V _{IL} = 0 V	(Note 12)	3.3	2.65	

Dynamic switching characteristics (Ta = 25° C, Input t_r = t_f = 2.0 ns, C_L = 30 pF)

(Note 12) : Parameter guaranteed by design.

Capacitive characteristics ($Ta = 25^{\circ}C$)

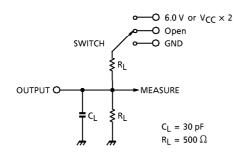
PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	UNIT
Input Capacitance	C _{IN}		1.8, 2.5, 3.3	6	рF
Bus I/O Capacitance	CI/O		1.8, 2.5, 3.3	7	рF
Power Dissipation Capacitance	C _{PD}	f _{IN} = 10 MHz (Note 13)	1.8, 2.5, 3.3	20	рF

(Note 13) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation :

 $I_{CC (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 18 (per bit)$

TEST CIRCUIT

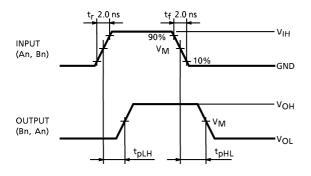
Fig.1



PARAMETER	SWITCH
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	6.0 V $@V_{CC} = 3.3 \pm 0.3 V$
	$V_{CC} \times 2 @V_{CC} = 2.5 \pm 0.2 V$
	V _{CC} × 2 @V _{CC} = 2.5 ± 0.2 V @V _{CC} = 1.8 V
t _{pHZ} , t _{pZH}	GND

AC WAVEFORM

Fig.2 tpLH, tpHL



SYMBOL	V _{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
VIH	2.7 V	Vcc	Vcc
VM	1.5 V	V _{CC} / 2	V _{CC} / 2
VX	V _{OL} + 0.3 V	V _{OL} + 0.15 V	V _{OL} + 0.15 V
VY	V _{OH} – 0.3 V	V _{OH} – 0.15 V	V _{OH} – 0.15 V

Fig.3 t_{pLH}, t_{pHL}, t_w, t_s, t_h

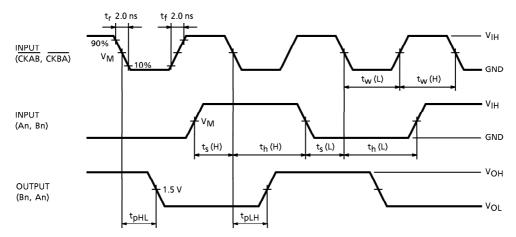


Fig.4 tpLH, tpHL, tw, ts, th

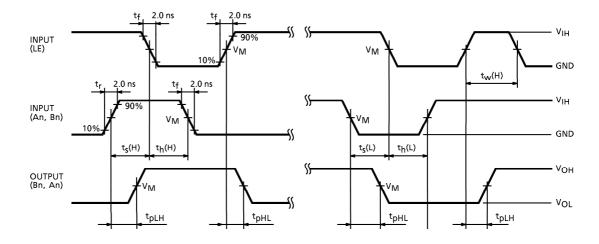


Fig.5 t_s, t_h

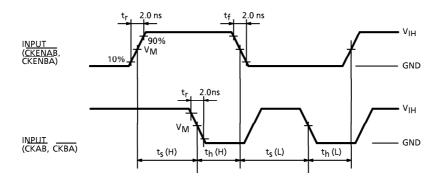
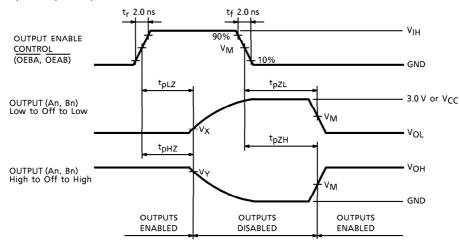
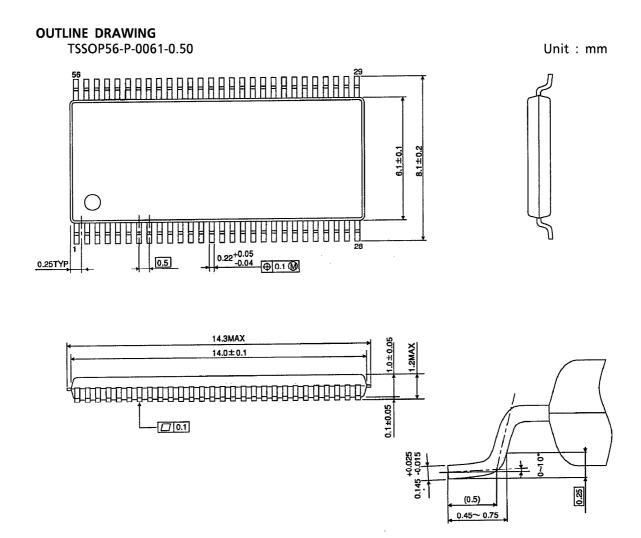


Fig.6 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}





Weight: 0.25 g (Typ.)

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