
HD74LVCZ16244A

16-bit Buffers / Line Drivers with 3-state Outputs

HITACHI

ADE-205-232 (Z)

1st. Edition

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Description

The HD74LVCZ16244A has sixteen line drivers with three state outputs in a 48 pin package. This device is a non inverting buffer and has four active low enables ($\overline{1G}$ to $\overline{4G}$). Each enable independently controls four buffers.

When V_{CC} is between 0 and 1.5 V, the device is in the high impedance state during power up or power down.

Low voltage and high speed operation is suitable at battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- $V_{CC} = 2.7$ to 5.5 V
- All inputs V_{IH} (Max) = 5.5 V (@ $V_{CC} = 0$ to 5.5 V)
- All outputs V_O (Max) = 5.5 V (@ $V_{CC} = 0$ V or output off state)
- Typical V_{OL} ground bounce < 0.8 V (@ $V_{CC} = 3.3$ V, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot > 2.0 V (@ $V_{CC} = 3.3$ V, $T_a = 25^\circ\text{C}$)
- High impedance state during power up and power down
- Power off disables outputs, permitting live insertion
- High output current ± 24 mA (@ $V_{CC} = 3.0$ to 5.5 V)

HD74LVCZ16244A

Function Table

Inputs		Output Y
$\overline{\text{G}}$	A	
H	X	Z
L	H	H
L	L	L

H : High level
L : Low level
X : Immaterial
Z : High impedance

HD74LVCZ16244A

Pin Arrangement

1 $\overline{G}$	1	48	2 $\overline{G}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V _{CC}	7	42	V _{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V _{CC}	18	31	V _{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4 $\overline{G}$	24	25	3 $\overline{G}$

(Top view)

HD74LVCZ16244A

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	−0.5 to 7.0	V	
Input voltage	V_I	−0.5 to 7.0	V	
Output voltage	V_O	−0.5 to 7.0 −0.5 to $V_{CC}+0.5$	V	Output “Z” or V_{CC} : OFF Output “H” or “L”
Input diode current	I_{IK}	−50	mA	$V_I < 0$
Output diode current	I_{OK}	−50	mA	$V_O < 0$
Output current	I_O	±50	mA	
V_{CC} , GND current	I_{CC} or I_{GND}	±100	mA	
Storage temperature	Tstg	−65 to 150	°C	

Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

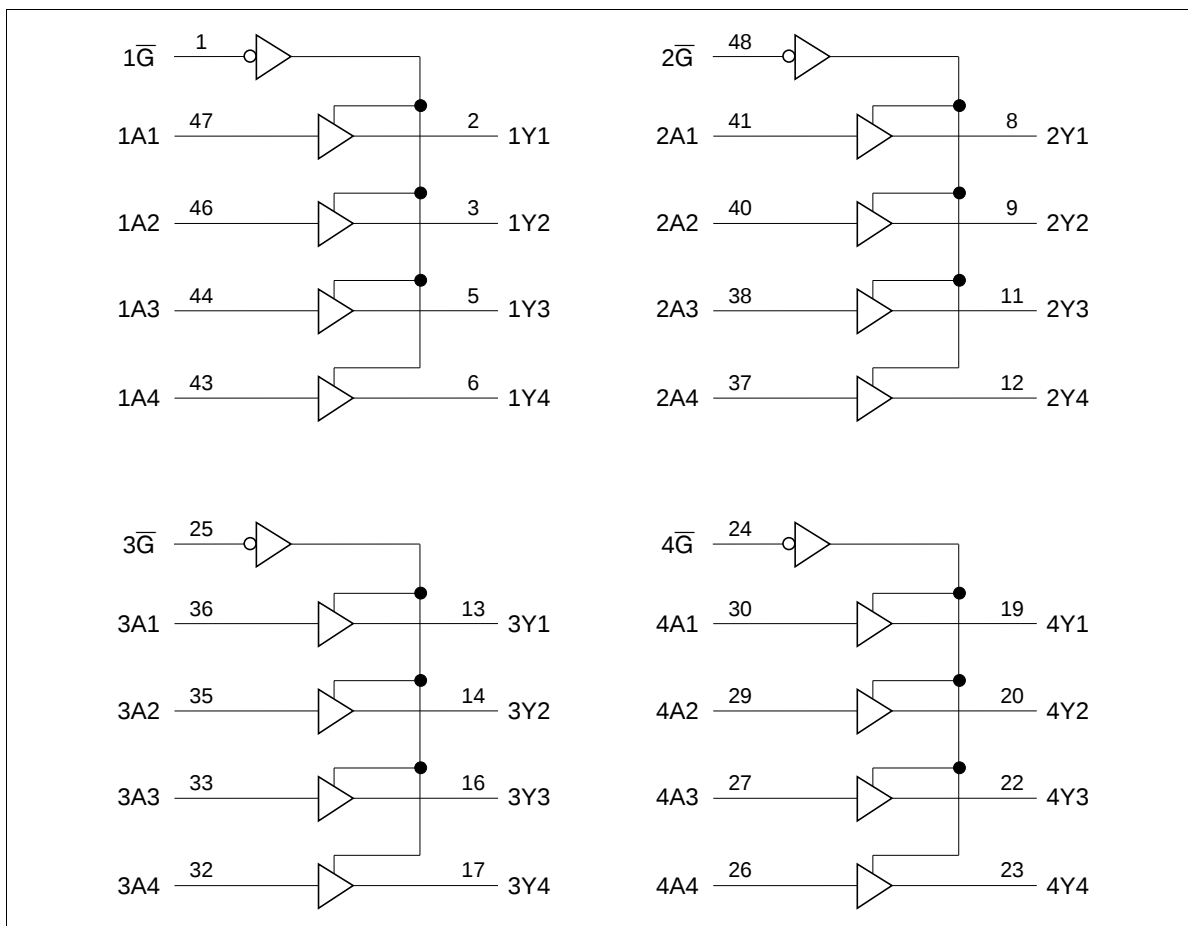
Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2.7 to 5.5	V	At operation
Input voltage	V_I	0 to 5.5	V	
Output voltage	V_O	0 to 5.5 0 to V_{CC}	V	Output “Z” or V_{CC} : OFF Output “H” or “L”
Output current	I_{OH}	−12 −24 ^{*1}	mA	$V_{CC} = 2.7$ V $V_{CC} = 3.0$ to 5.5 V
	I_{OL}	12 24 ^{*1}		$V_{CC} = 2.7$ V $V_{CC} = 3.0$ to 5.5 V
Input rise / fall time	t_r, t_f	0 to 6	ns / V	
Operating temperature	Ta	−40 to +85	°C	

Note: 1. Duty cycle ≤ 50%

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Logic Diagram



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Electrical Characteristics (Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.7 to 3.6	2.0	—	—	V	
		4.5 to 5.5	V _{CC} ×0.7	—	—		
	V _{IL}	2.7 to 3.6	—	—	0.8		
		4.5 to 5.5	—	—	V _{CC} ×0.3		
Output voltage	V _{OH}	2.7 to 5.5	V _{CC} -0.2	—	—	V	I _{OH} = -100 μA
		2.7	2.2	—	—		I _{OH} = -12 mA
		3.0	2.4	—	—		
		3.0	2.2	—	—		I _{OH} = -24 mA
		4.5	3.8	—	—		
	V _{OL}	2.7 to 5.5	—	—	0.2		I _{OL} = 100 μA
		2.7	—	—	0.4		I _{OL} = 12 mA
		3.0	—	—	0.55		I _{OL} = 24 mA
		4.5	—	—	0.55		
Input current	I _{IN}	0 to 5.5	—	—	±5	μA	V _{IN} = 0 to 5.5 V
Off state output current	I _{OZ}	2.7 to 5.5	—	—	±5	μA	V _{OUT} = 0 to 5.5 V
	I _{OZPU}	0 to 1.5	—	—	±5		V _{OUT} = 0.5 to 5.5 V,
	I _{OZPD}	1.5 to 0	—	—	±5		Output enable = don't care
Output leak current	I _{OFF}	0	—	—	±5	μA	V _{IN} or V _O = 5.5 V
Quiescent supply current	I _{CC}	2.7 to 3.6	—	—	225	μA	V _{IN} = 3.6 to 5.5 V ^{*1} , I _O = 0
		2.7 to 5.5	—	—	350		V _{IN} = V _{CC} or GND
	ΔI _{CC}	2.7 to 3.6	—	—	500		V _{IN} = one input at (V _{CC} -0.6) V, other inputs at V _{CC} or GND
Input capacitance	C _{IN}	3.3	—	4.1	—	pF	V _{IN} = V _{CC} or GND
Output capacitance	C _O	3.3	—	8.1	—	pF	V _{OUT} = V _{CC} or GND

Note: 1. This applies in the disabled state only.

HD74LVCZ16244A

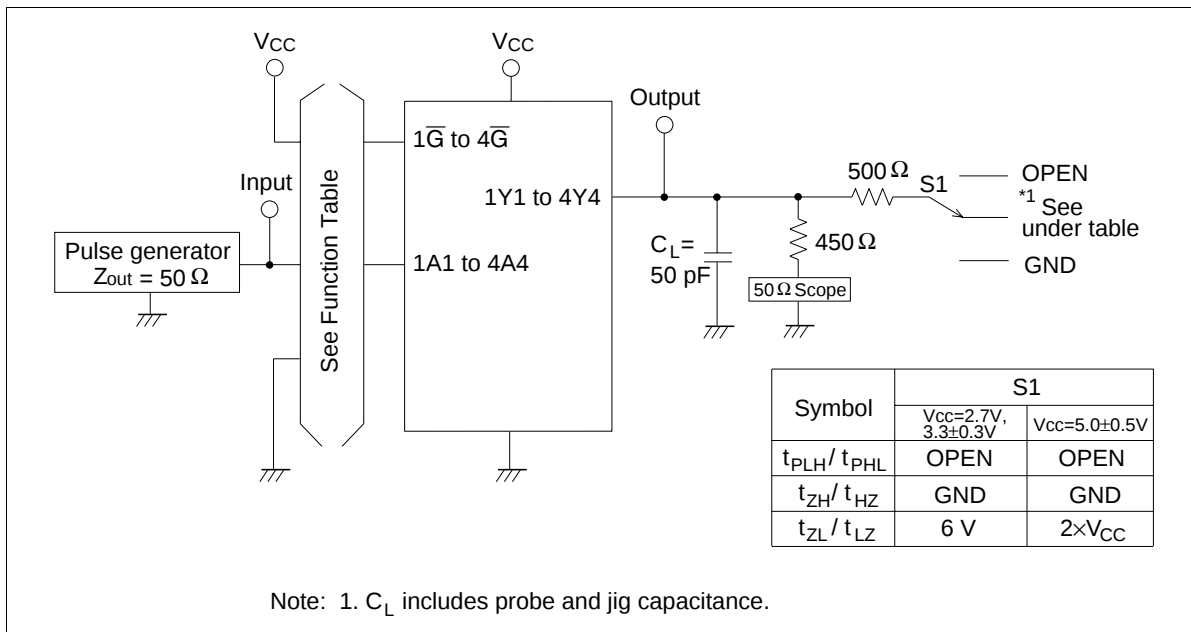
Switching Characteristics (Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Propagation delay time	t _{PLH}	2.7	—	—	4.7	ns	A	Y
	t _{PHL}	3.3±0.3	1.1	—	4.1			
		5.0±0.5	—	—	3.8			
Output enable time	t _{ZH}	2.7	—	—	5.8	ns	$\overline{G}$	Y
	t _{ZL}	3.3±0.3	1.0	—	4.6			
		5.0±0.5	—	—	4.4			
Output disable time	t _{HZ}	2.7	—	—	6.2	ns	$\overline{G}$	Y
	t _{LZ}	3.3±0.3	1.8	—	5.8			
		5.0±0.5	—	—	4.6			
Between output pin skew ^{*1}	t _{OSLH}	2.7	—	—	—	ns		
	t _{OSHL}	3.3±0.3	—	—	1.0			
		5.0±0.5	—	—	1.0			

Note : 1. This parameter is characterized but not tested.

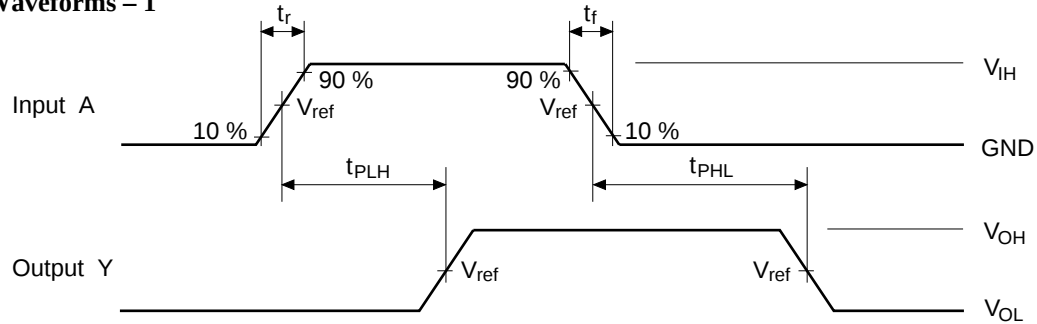
$$t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|$$

Test Circuit

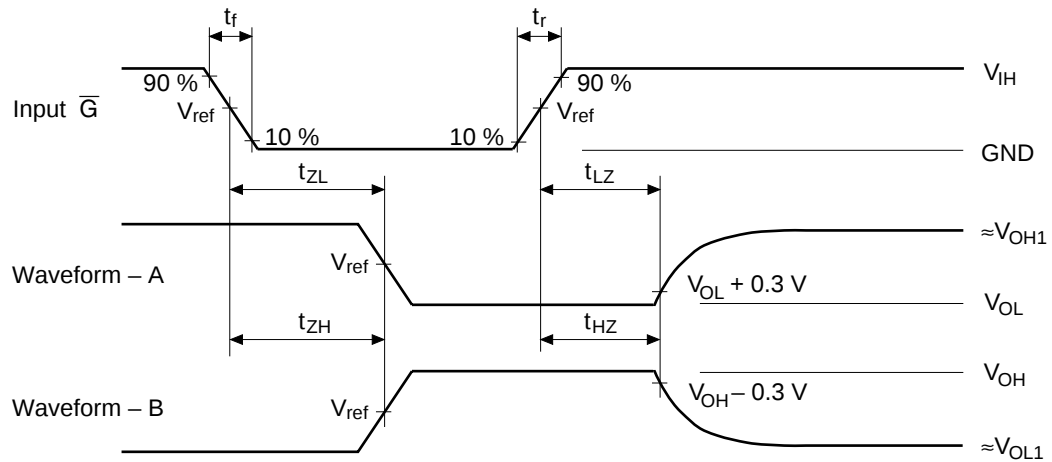


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• Waveforms – 1

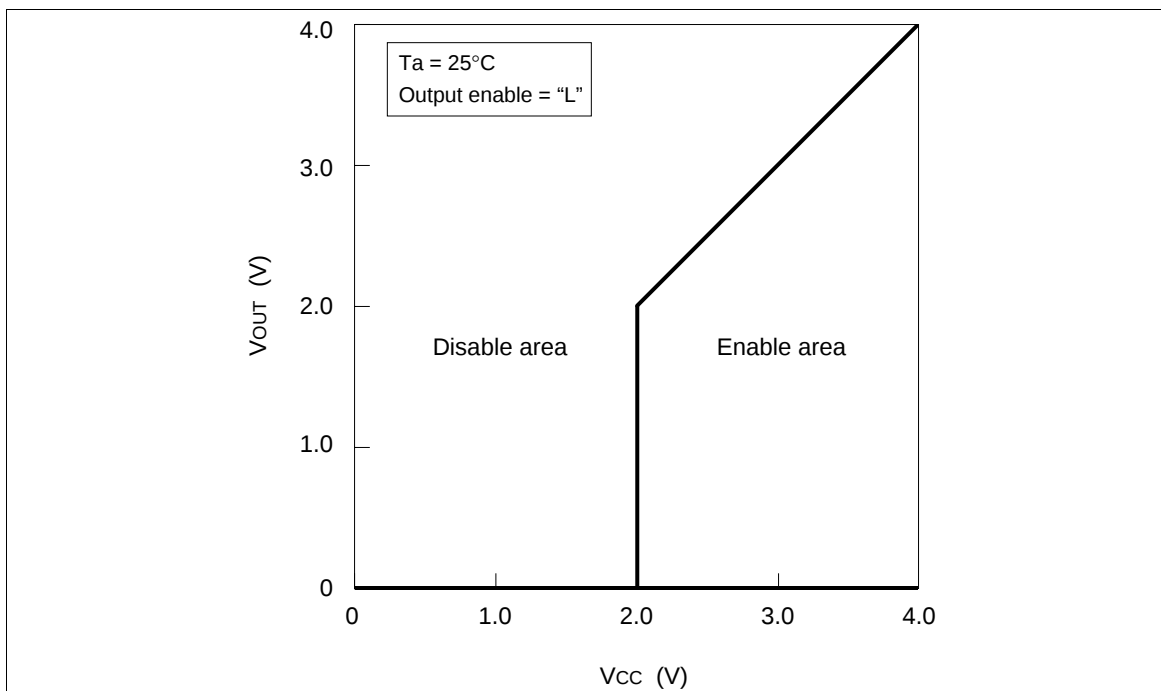


• Waveforms – 2



TEST	$V_{CC}=2.7V, 3.3\pm0.3V$	$V_{CC}=5.0\pm0.5V$
V_{IH}	2.7 V	V_{CC}
V_{ref}	1.5 V	50% V_{CC}
V_{OH1}	3 V	V_{CC}
V_{OL1}	GND	GND

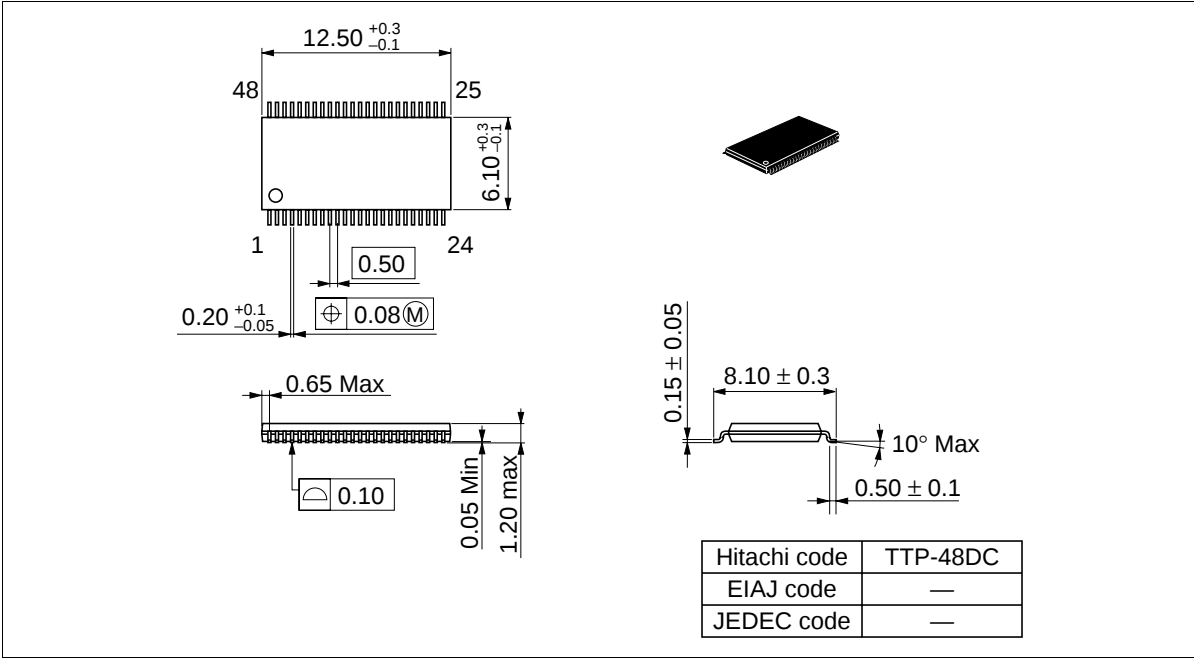
- Notes:
1. Input waveform : PRR = 10 MHz, duty cycle 50%, $t_r = 2.5$ ns, $t_f = 2.5$ ns
 2. Waveform – A shows input conditions such that the output is "L" level when enabled by the output control.
 3. Waveform – B shows input conditions such that the output is "H" level when enabled by the output control.

Power up / down Characteristics

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Package Dimensions

Unit : mm



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