

## MULTIPOINT-LVDS QUAD DIFFERENTIAL LINE DRIVER

### FEATURES

- Differential Line Drivers for 30-Ω to 55-Ω Loads and Data Rates<sup>(1)</sup> Up to 200 Mbps, Clock Frequencies up to 100 MHz
- Supports Multipoint Bus Architectures
- Meets the Requirements of TIA/EIA-899
- Operates from a Single 3.3-V Supply
- Characterized for Operation from –40°C to 85°C
- 16-Pin SOIC (JEDEC MS-012) and 16-Pin TSSOP (JEDEC MS-153) Packaging

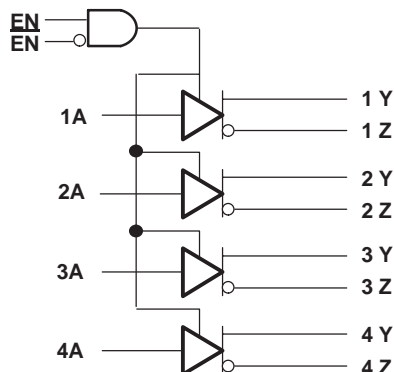
### APPLICATIONS

- AdvancedTCA™ (ATCA™) Clock Bus Driver
- Clock Distribution
- Backplane or Cabled Multipoint Data Transmission in Telecommunications, Automotive, Industrial, and Other Computer Systems
- Cellular Base Stations
- Central-Office and PBX Switching
- Bridges and Routers
- Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485

### DESCRIPTION

The SN65MLVD047 is a quadruple line driver that complies with the TIA/EIA-899 standard, Electrical Characteristics of Multipoint-Low-Voltage Differential Signaling (M-LVDS). The output current of this M-LVDS device has been increased, in comparison to standard LVDS compliant devices, in order to support doubly terminated transmission lines and heavily loaded backplane bus applications. Backplane applications generally require impedance matching termination resistors at both ends of the bus. The effective impedance of a doubly terminated bus can be as low as 30 Ω due to the bus terminations, as well as the capacitive load of bus interface devices. SN65MLVD047 drivers allow for operation with loads as low as 30 Ω. The SN65MLVD047 devices allow for multiple drivers to be present on a single bus. SN65MLVD047 drivers are high impedance when disabled or unpowered. Driver edge rate control is incorporated to support operation. The M-LVDS standard allows up to 32 nodes (drivers and/or receivers) to be connected to the same media in a backplane when multiple bus stubs are expected from the main transmission line to interface devices. The SN65MLVD047 provides 9-kV ESD protection on all bus pins.

### LOGIC DIAGRAM (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

<sup>(1)</sup>The data rate of a line, is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE/CARRIER
SN65MLVD047D	MLVD047	16-Pin SOIC/Tube
SN65MLVD047DR	MLVD047	16-Pin SOIC/Tape and Reel
SN65MLVD047PW	MLVD047	16-Pin TSSOP/Tube
SN65MLVD047PWR	MLVD047	16-Pin TSSOP/Tape and Reel

## PACKAGE DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ (1)	$T_A = 85^\circ\text{C}$ POWER RATING
D(16)	Low-K(2)	898 mW	7.81 mW/ $^\circ\text{C}$	429 mW
PW(16)	Low-K(2)	592 mW	5.15 mW/ $^\circ\text{C}$	283 mw
	High-K(3)	945 mW	8.22 mW/ $^\circ\text{C}$	452 mw

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51–3.

(3) In accordance with the High-K thermal metric definitions of EIA/JESD51–7.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNITS
Supply voltage range(2), $V_{CC}$			–0.5 V to 4 V
Input voltage range, $V_I$	A, EN, $\overline{\text{EN}}$		–0.5 V to 4 V
Output voltage range, $V_O$	Y, Z		–1.8 V to 4 V
Electrostatic discharge	Human Body Model(3)	Y and Z	$\pm 9$ kV
		All pins	$\pm 4$ kV
	Charged-Device Model(4)	All pins	$\pm 1500$ V
	Machine Model(5)	All pins	200 V
Junction temperature, $T_J$			140 $^\circ\text{C}$
Continuous power dissipation, $P_D$			See Dissipation Rating Table

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to the circuit ground terminal.

(3) Tested in accordance with JEDEC Standard 22, Test Method A114–B.

(4) Tested in accordance with JEDEC Standard 22, Test Method C101–A.

(5) Tested in accordance with JEDEC Standard 22, Test Method A115–A.

## RECOMMENDED OPERATING CONDITIONS (see Figure 1)

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	3	3.3	3.6	V
High-level input voltage, $V_{IH}$	2		$V_{CC}$	V
Low-level input voltage, $V_{IL}$	0		0.8	V
Voltage at any bus terminal (separate or common mode) $V_Y$ or $V_Z$	-1.4		3.8	V
Differential load resistance, $R_L$	30		55	$\Omega$
Signaling rate, $1/t_{UI}$			200	Mbps
Clock frequency			100	MHz
Junction temperature, $T_J$	-40		125	$^{\circ}\text{C}$

## THERMAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Junction-to-ambient thermal resistance, $\Theta_{JA}$	Low-K board <sup>(1)</sup> , no airflow	D		128		$^{\circ}\text{C}/\text{W}$
	Low-K board <sup>(1)</sup> , no airflow	PW		194.2		
	Low-K board <sup>(1)</sup> , 150 LFM			146.8		
	Low-K board <sup>(1)</sup> , 250 LFM			133.1		
	High-K board <sup>(2)</sup> , no airflow			121.6		
Junction-to-board thermal resistance, $\Theta_{JB}$	High-K board <sup>(2)</sup>	D		51.1		$^{\circ}\text{C}/\text{W}$
		PW		85.3		
Junction-to-case thermal resistance, $\Theta_{JC}$		D		45.4		$^{\circ}\text{C}/\text{W}$
		PW		34.7		
Device power dissipation, $P_D$	EN = $V_{CC}$ , $\overline{\text{EN}}$ = GND, $R_L = 50 \Omega$ , Input 100 MHz 50 % duty cycle square wave to 1A:4A, $T_A = 85^{\circ}\text{C}$				288.5	mW

(1) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

(2) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

## DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS		MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX	UNIT
$I_{CC}$ Supply current	Driver enabled	EN = $V_{CC}$ , $\overline{\text{EN}}$ = GND, $R_L = 50 \Omega$ , All inputs = $V_{CC}$ or GND		59	70	mA
	Driver disabled	EN = GND, $\overline{\text{EN}}$ = $V_{CC}$ , $R_L$ = No load, All inputs = $V_{CC}$ or GND		2	4	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) All typical values are at  $25^{\circ}\text{C}$  and with a 3.3-V supply voltage.

**DEVICE ELECTRICAL CHARACTERISTICS**

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX	UNIT
LVTTTL (EN, $\overline{\text{EN}}$ , 1A:4A)						
$ I_{IH} $	High-level input current	$V_{IH} = 2 \text{ V or } V_{CC}$	0		10	$\mu\text{A}$
$ I_{IL} $	Low-level input current	$V_{IL} = \text{GND or } 0.8 \text{ V}$	0		10	$\mu\text{A}$
$C_i$	Input capacitance	$V_I = 0.4 \sin(30E6\pi t) + 0.5 \text{ V}^{(3)}$		5		pF
M-LVDS (1Y/1Z:4Y/4Z)						
$ V_{YZ} $	Differential output voltage magnitude	See Figure 2	480		650	mV
$\Delta V_{YZ} $	Change in differential output voltage magnitude between logic states		-50		50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	See Figure 3	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage				150	mV
$V_{Y(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 7	0		2.4	V
$V_{Z(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	See Figure 5			$1.2V_{SS}$	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output		$-0.2V_{SS}$			V
$ I_{OS} $	Differential short-circuit output current magnitude	See Figure 4			24	mA
$I_{OZ}$	High-impedance state output current	$-1.4 \text{ V} \leq (V_Y \text{ or } V_Z) \leq 3.8 \text{ V}$ , Other output = 1.2 V	-15		10	$\mu\text{A}$
$I_{O(OFF)}$	Power-off output current	$-1.4 \text{ V} \leq (V_Y \text{ or } V_Z) \leq 3.8 \text{ V}$ , Other output = 1.2 V, $V_{CC} = 0 \text{ V}$	-10		10	$\mu\text{A}$
$C_Y \text{ or } C_Z$	Output capacitance	$V_Y \text{ or } V_Z = 0.4 \sin(30E6\pi t) + 0.5 \text{ V}$ , <sup>(3)</sup> Other input at 1.2 V, driver disabled		3		pF
$C_{YZ}$	Differential output capacitance	$V_{YZ} = 0.4 \sin(30E6\pi t) \text{ V}$ , <sup>(3)</sup> Driver disabled			2.5	pF
$C_{Y/Z}$	Output capacitance balance, $(C_Y/C_Z)$		0.99	1.01		

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

(2) All typical values are at 25°C and with a 3.3-V supply voltage.

(3) HP4194A impedance analyzer (or equivalent)

## SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$t_{pLH}$ Propagation delay time, low-to-high-level output	See Figure 5	1	1.5	2.4	ns
$t_{pHL}$ Propagation delay time, high-to-low-level output		1	1.5	2.4	ns
$t_r$ Differential output signal rise time		1		1.9	ns
$t_f$ Differential output signal fall time		1		1.9	ns
$t_{sk(o)}$ Output skew				100	ps
$t_{sk(p)}$ Pulse skew ( $ t_{pHL} - t_{pLH} $ )			22	100	ps
$t_{sk(pp)}$ Part-to-part skew(2)				600	ps
$t_{jit(per)}$ Period jitter, rms (1 standard deviation)(3)	All inputs 100 MHz clock input		0.2	1	ps
$t_{jit(c-c)}$ Cycle-to-cycle jitter(3)	All inputs 100 MHz clock input		5	36	ps
$t_{jit(pp)}$ Peak-to-peak jitter(3)(4)	All inputs 200 Mbps 2 <sup>15</sup> -1 PRBS input		46	158	ps
$t_{pZH}$ Enable time, high-impedance-to-high-level output	See Figure 6			7	ns
$t_{pZL}$ Enable time, high-impedance-to-low-level output				7	ns
$t_{pHZ}$ Disable time, high-level-to-high-impedance output	See Figure 6			8	ns
$t_{pLZ}$ Disable time, low-level-to-high-impedance output				8	ns

(1) All typical values are at 25°C and with a 3.3-V supply voltage.

(2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) Stimulus jitter has been subtracted from the measurements.

(4) Peak-to-peak jitter includes jitter due to pulse skew ( $t_{sk(p)}$ ).

## PARAMETER MEASUREMENT INFORMATION

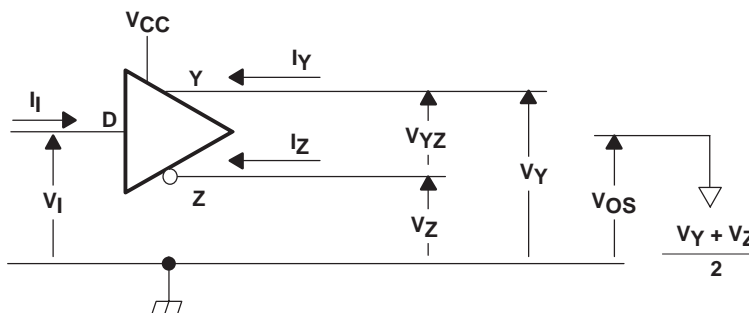
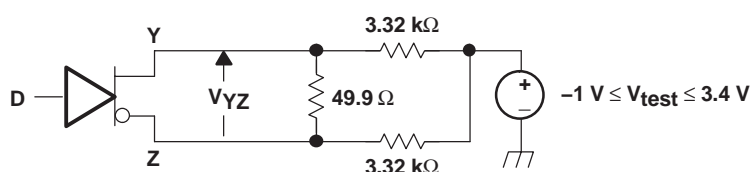
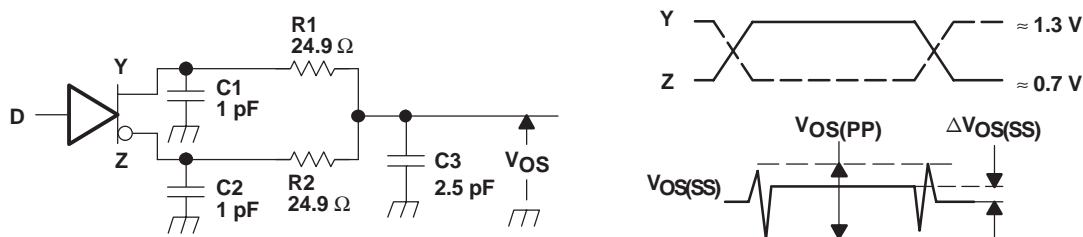


Figure 1. Driver Voltage and Current Definitions



NOTE: All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



- NOTES:
- A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse frequency = 500 kHz, duty cycle =  $50 \pm 5\%$ .
  - B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are  $\pm 20\%$ .
  - C. R1 and R2 are metal film, surface mount,  $\pm 1\%$ , and located within 2 cm of the D.U.T.
  - D. The measurement of  $V_{OS(PP)}$  is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Common-Mode Output Voltage

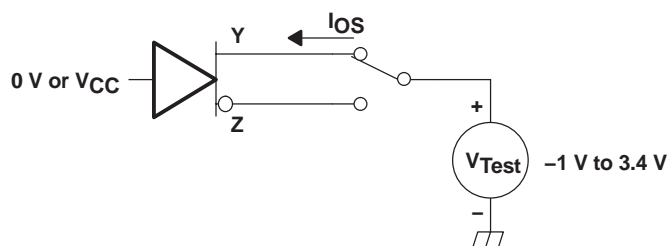
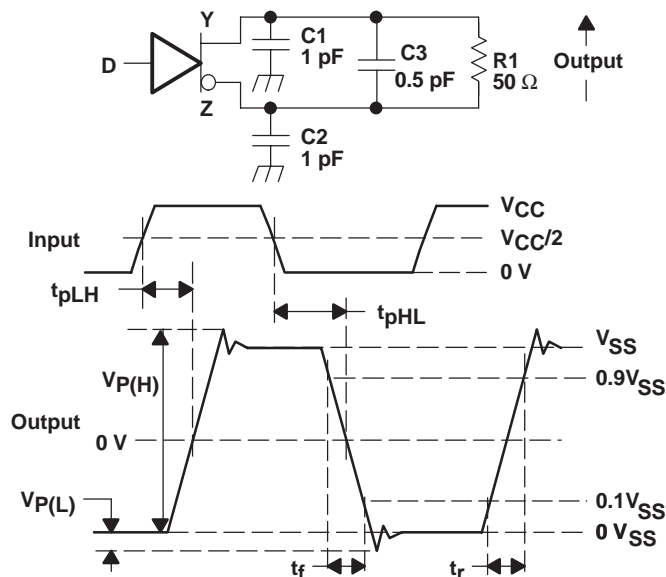
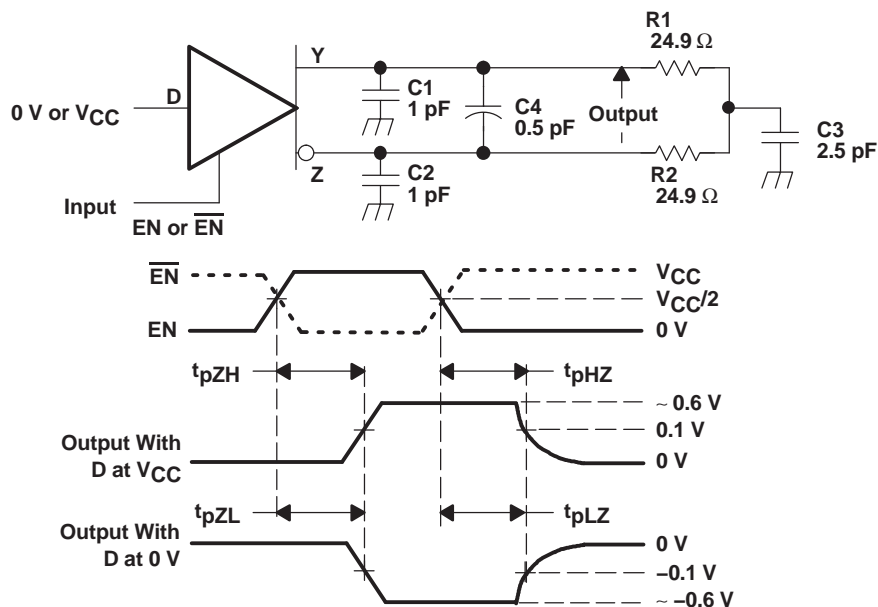


Figure 4. Short-Circuit Test Circuit



- NOTES: A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 500 kHz, duty cycle =  $50 \pm 5\%$ .  
 B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are  $\pm 20\%$ .  
 C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.  
 D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



- NOTES: A. All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, frequency = 500 kHz, duty cycle =  $50 \pm 5\%$ .  
 B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are  $\pm 20\%$ .  
 C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.  
 D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 6. Driver Enable and Disable Time Circuit and Definitions

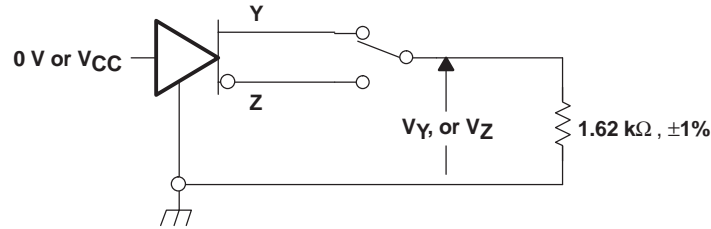
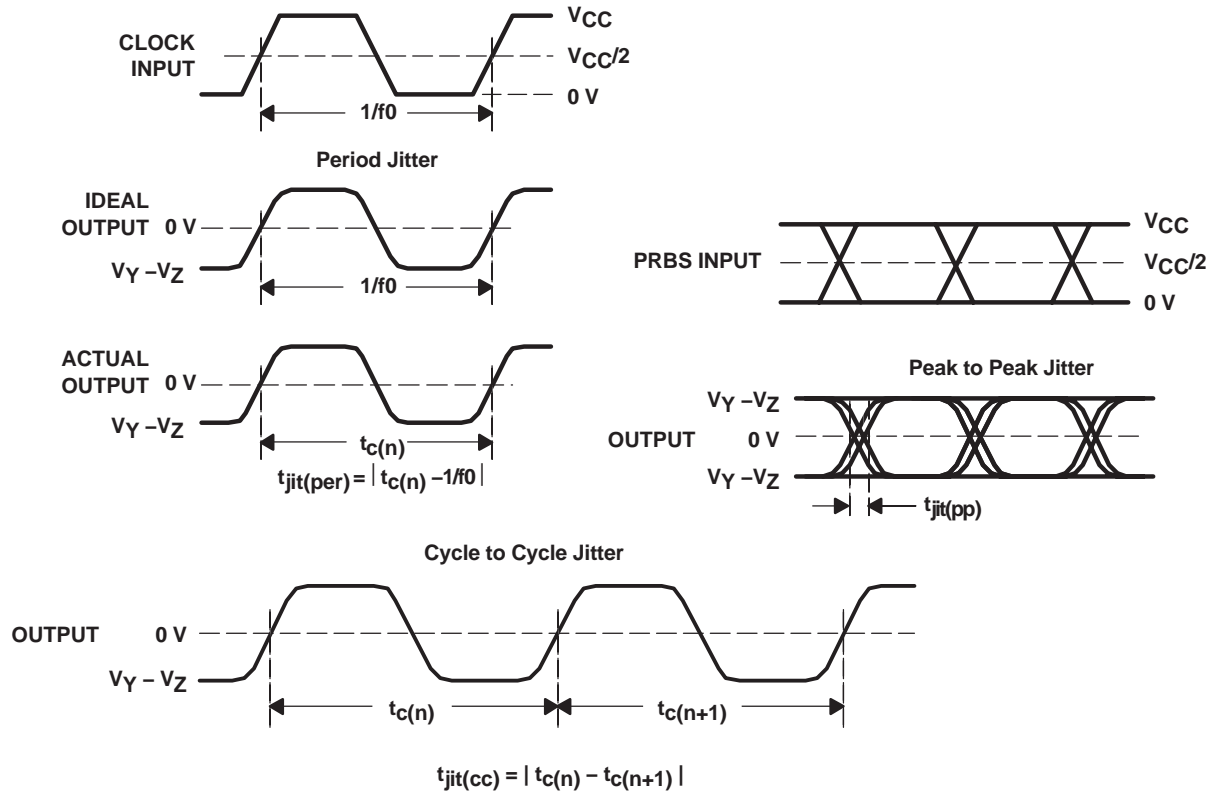


Figure 7. Driver Maximum Steady State Output Voltage



- NOTES:
- A. All input pulses are supplied by an Agilent 8304A Stimulus System.
  - B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
  - C. Period jitter and cycle-to-cycle jitter are measured using a 100 MHz 50  $\pm$ 1% duty cycle clock input.
  - D. Peak-to-peak jitter is measured using a 200 Mbps  $2^{15}-1$  PRBS input.

Figure 8. Driver Jitter Measurement Waveforms

## DEVICE INFORMATION

### PIN ASSIGNMENTS





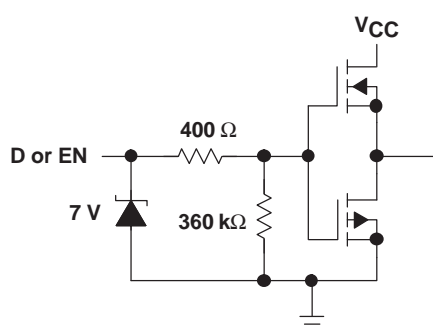
DEVICE FUNCTION TABLE

INPUTS			OUTPUTS	
D	EN	$\overline{\text{EN}}$	Y	Z
L	H	L	L	H
H	H	L	H	L
OPEN	H	L	L	H
X	L or OPEN	X	Z	Z
X	X	H or OPEN	Z	Z

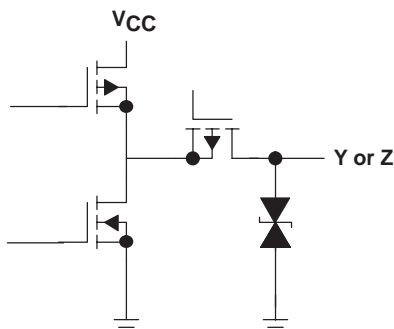
H = high level, L = low level, Z = high impedance, X = Don't care

## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

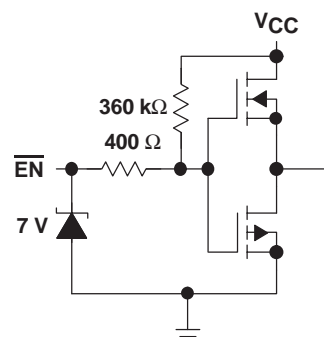
DRIVER INPUT AND POSITIVE DRIVER ENABLE



DRIVER OUTPUT



NEGATIVE DRIVER ENABLE



## TYPICAL CHARACTERISTICS

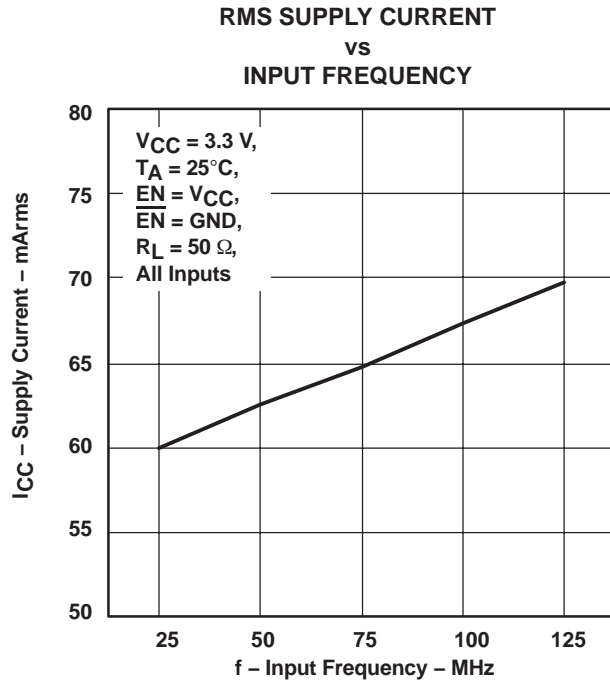


Figure 9

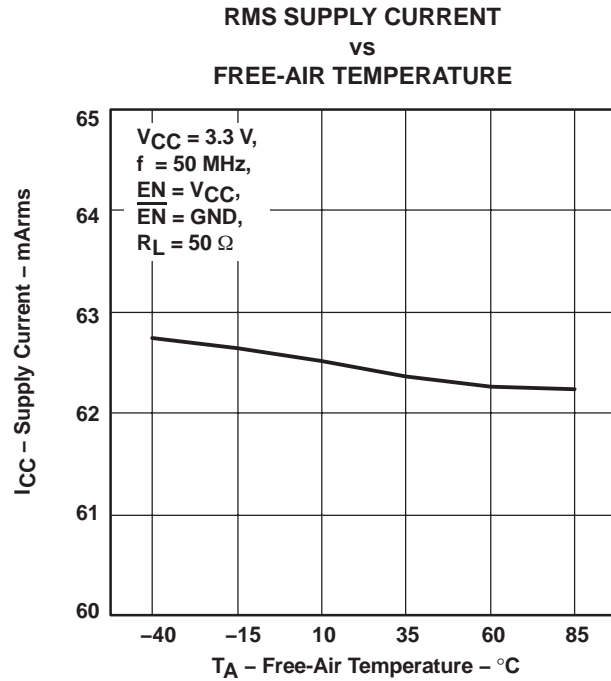


Figure 10

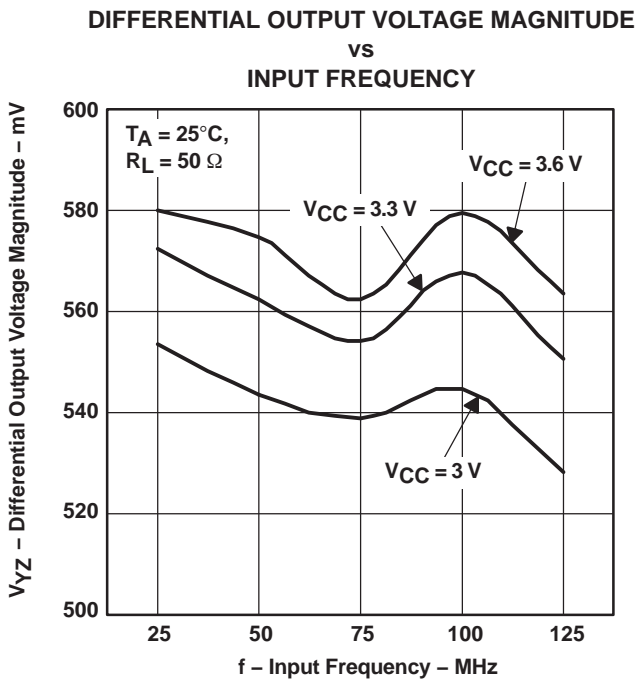


Figure 11

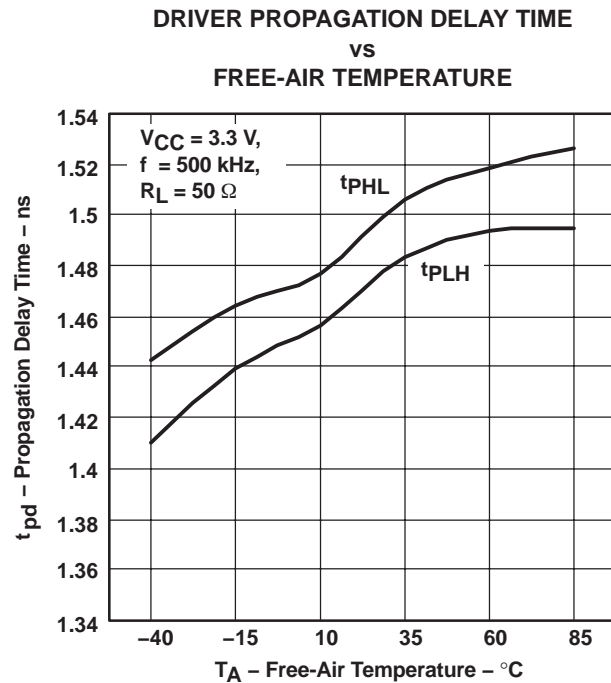


Figure 12

## TYPICAL CHARACTERISTICS

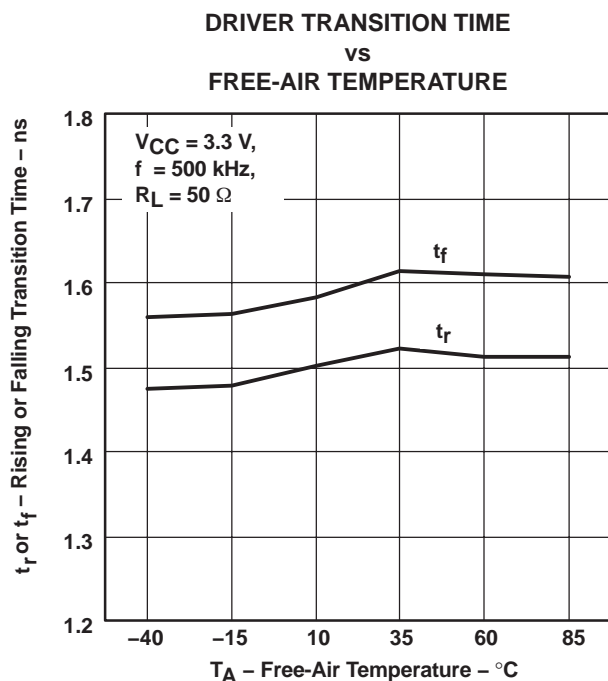


Figure 13

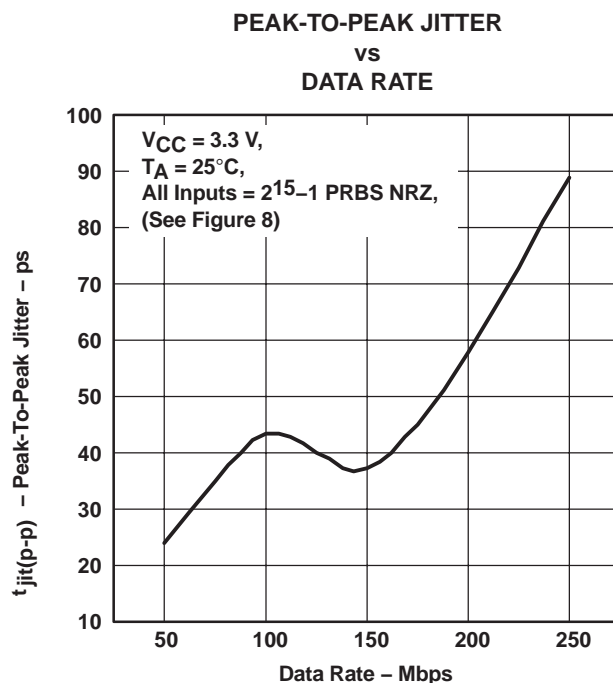


Figure 14

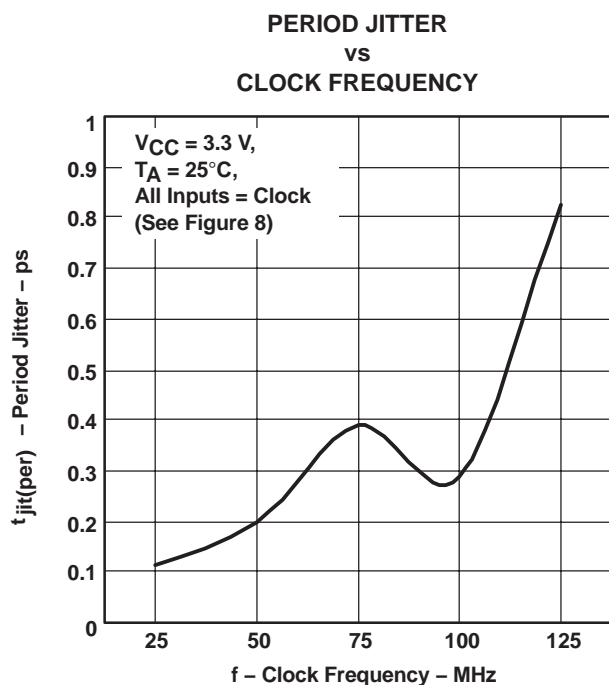


Figure 15

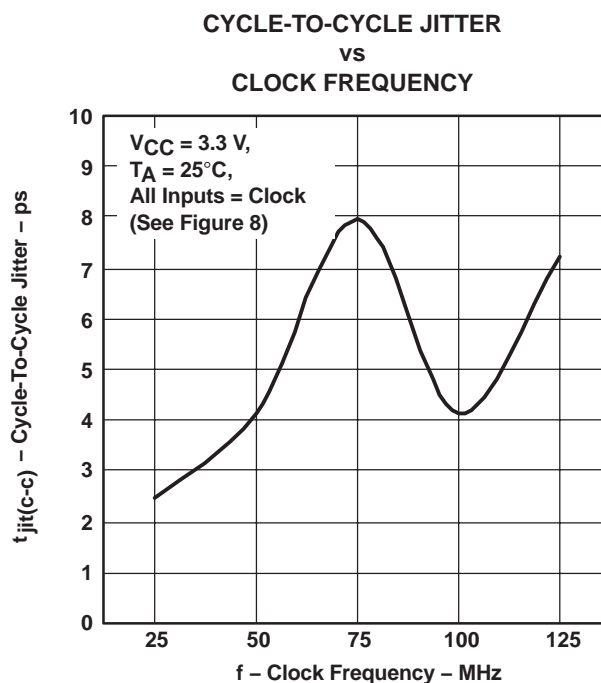


Figure 16

## APPLICATION INFORMATION

### SYNCHRONIZATION CLOCK IN ADVANCEDTCA

Advanced Telecommunications Computing Architecture, also known as AdvancedTCA, is an open architecture to meet the needs of the rapidly changing communications network infrastructure. M-LVDS based clocking is recommended by the ATCA.

The ATCA specification includes requirements for three redundant clock signals. An 8-KHz and a 19.44-MHz clock signal, as well as an user-defined clock signal are included in the specification. The SN65MLVD047 quad driver supports distribution of these three ATCA clock signals, supporting operation beyond 100 MHz, which is the highest clock frequency included in the ATCA specification. A pair of SN65MLVD047 devices can be used to support the ATCA redundancy requirements.

### MULTIPOINT CONFIGURATION

The SN65MLVD047 is designed to meet or exceed the requirement of the TIA/EIA-899 (M-LVDS) standard, which allows multipoint communication on a shared bus.

Multipoint is a bus configuration with multiple drivers and receivers present. An example is shown in Figure 17. The figure shows transceivers interfacing to the bus, but a combination of drivers, receivers, and transceivers is also possible. Termination resistors need to be placed on each end of the bus, with the termination resistor value matched to the loaded bus impedance.

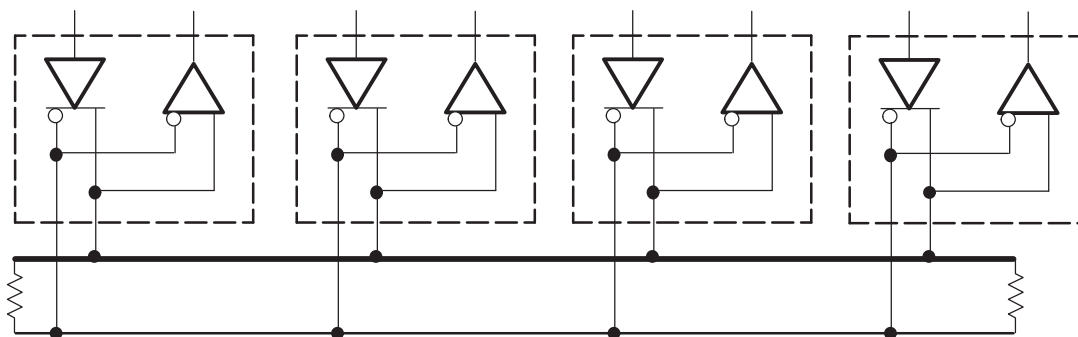
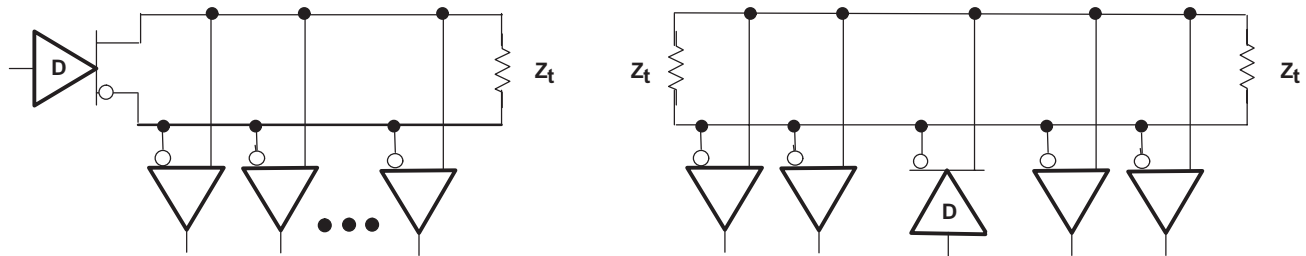


Figure 17. Multipoint Architecture

### MULTIDROP CONFIGURATION

Multidrop configuration is similar to multipoint configuration, but only one driver is present on the bus. A multidrop system can be configured with the driver at one end of the bus, or in the middle of the bus. When a driver is located at one end, a single termination resistor is located at the far end, close to the last receiver on the bus. Alternatively, the driver can be located in the middle of the bus, to reduce the maximum flight time. With a centrally located driver, termination resistors are located at each end of the bus. In both cases the termination resistor value should be matched to the loaded bus impedance. Figure 18 shows examples of both cases.



**Figure 18. Multidrop Architectures With Different Driver Locations**

### UNUSED CHANNEL

The SN65MLVD047 is designed to meet or exceed the requirement of the TIA/EIA-899 (M-LVDS) standard, which allows multipoint communication on a standard bus. A 360-k $\Omega$  pull-down resistor is built in every LVTTTL input. The unused driver inputs and outputs may be left floating.

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65MLVD047D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD047DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD047PW	ACTIVE	TSSOP	PW	16	90	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65MLVD047PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD047PWR	ACTIVE	TSSOP	PW	16	2000	TBD	CU NIPDAU	Level-1-220C-UNLIM
SN65MLVD047PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/F 07/2004

## NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- Falls within JEDEC MS-012 variation AC.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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