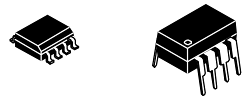


WIDE SUPPLY RANGE RS-485 TRANSCEIVER

FEATURES

- **Operates With a 3-V to 5.5-V Supply**
- **Consumes Less Than 90 mW Quiescent Power**
- **Open-Circuit, Short Circuit, and Idle-Bus Failsafe Receiver**
- **1/8th Unit-Load (up to 256 nodes on the bus)**
- **Bus-Pin ESD Protection Exceeds 16 kV HBM**
- **Driver Output Voltage Slew-Rate Limited for Optimum Signal Quality at 10 Mbps**
- **Electrically Compatible With ANSI TIA/EIA-485 Standard**

APPLICATIONS

- **Data Transmission With Remote Stations Powered From the Host**
- **Isolated Multipoint Data Buses**
- **Industrial Process Control Networks**
- **Point-of-Sale Networks**
- **Electric Utility Metering**

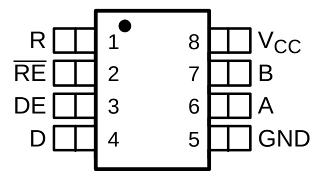
DESCRIPTION

The SN65HVD08 combines a 3-state differential line driver and differential line receiver designed for balanced data transmission and interoperation with ANSI TIA/EIA-485-A and ISO-8482E standard-compliant devices.

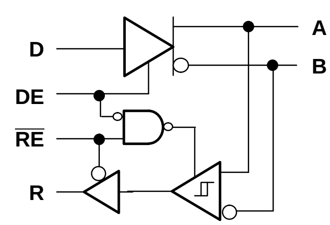
The wide supply voltage range and low quiescent current requirements allow the SN65HVD08s to operate from a 5-V power bus in the cable with as much as a 2-V line voltage drop. Busing power in the cable can alleviate the need for isolated power to be generated at each connection of a ground-isolated bus.

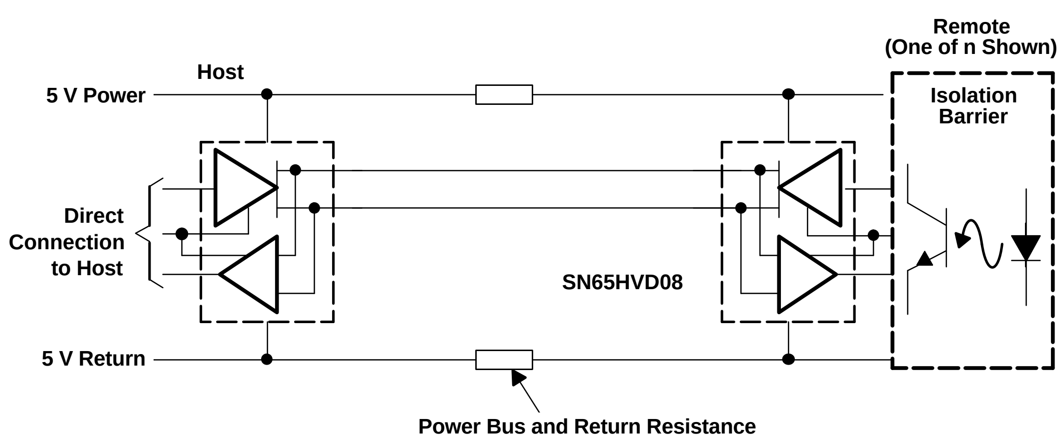
The driver differential outputs and receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus whenever the driver is disabled or not powered. The drivers and receivers have active-high and active-low enables respectively, which can be externally connected together to function as a direction control.

D or P PACKAGE
(TOP VIEW)



LOGIC DIAGRAM (Positive Logic)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE	PACKAGE MARKING
SN65HVD08D	–40°C to 85°C	SOIC	VP08
SN65HVD08P	–40°C to 85°C	PDIP	65HVD08
SN75HVD08D	0°C to 70°C	SOIC	VN08
SN75HVD08P	0°C to 70°C	PDIP	75HVD08

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq$ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
SOIC (D)	710 mW	5.7 mW/°C	369 mW
PDIP (P)	1000 mW	8 mW/°C	520 mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[(1)(2)]

			UNIT
Supply voltage, V_{CC}			-0.3 V to 6 V
Voltage range at A or B			-9 V to 14 V
Input voltage range at D, DE, R or $\overline{RE}$			-0.5 V to V_{CC} + 0.5 V
Voltage input range, transient pulse, A and B, through 100 Ω			-25 V to 25 V
Electrostatic discharge	Human Body Model [(3)]	A, B, and GND	16 kV
		All pins	4 kV
	Charged-Device Model[(4)]	All pins	1 kV
Continuous total power dissipation			See Dissipation Rating Table
Storage temperature, T_{stg}			-65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3		5.5	V
Input voltage at any bus terminal (separately or common mode), V_I[(1)]		–7		12	V
High-level input voltage, V_{IH}	Driver, driver enable, and receiver enable inputs	2.25		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	
Differential input voltage, V_{ID}		–12		12	
High-level output current, I_{OH}	Driver	–60			mA
	Receiver	–8			
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A	SN75HVD08	0		70	°C
	SN65HVD08	–40		85	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L= 60 Ω, 375 Ω on each output to -7 V to 12 V, See Figure 1	1.5		V_{CC}	V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L= 54 Ω	–0.2		0.2	V
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See Figure 2		0.5		V
V_{IT+}	Positive-going receiver differential input voltage threshold				–10	mV
V_{IT-}	Negative-going receiver differential input voltage threshold		–200			mV
V_{hys}	Receiver differential input voltage threshold hysteresis(V_{IT+} - V_{IT-})			35		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = -8 mA	2.4			V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.4	V
I_{IH}	Driver input, driver enable, and receiver enable high-level input current		–100		100	μA
I_{IL}	Driver input, driver enable, and receiver enable low-level input current		–100		100	μA
I_{OS}	Driver short-circuit output current	7 V < V_O < 12 V	–265		265	mA
I_I	Bus input current (disabled driver)	V_I = 12 V			130	μA
		V_I = -7 V	–100			
		V_I = 12 V, V_{CC} = 0 V			130	
		V_I = -7 V. V_{CC} = 0 V	–100			
I_{CC}	Supply current	Receiver enabled, driver disabled, no load			10	mA
		Driver enabled, receiver disabled, no load			16	
		Both disabled			5	μA
		Both enabled, no load			16	mA

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Driver high-to-low propagation delay time	R_L = 54 Ω, C_L = 50 pF,See Figure 3	18		40	ns
t_{PLH}	Driver low-to-high propagation delay time		18		40	
t_r	Driver 10%-to-90% differential output rise time		10		55	
t_f	Driver 90%-to-10% differential output fall time		10		55	
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL}$ - $t_{PLH}\|$				2.5	
t_{en}	Driver enable time	Receiver enabled, See Figures 4 and 5			55	ns
		Receiver disabled, See Figures 4 and 5			6	μs
t_{dis}	Driver disable time	Receiver enabled, See Figures 4 and 5			90	ns

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Receiver high-to-low propagation delay time	C_L = 15 pF, See Figure 6			70	ns
t_{PLH}	Receiver low-to-high propagation delay time				70	
t_r	Receiver 10%-to-90% differential output rise time				5	
t_f	Receiver 90%-to-10% differential output fall time				5	
$t_{SK(P)}$	Receiver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$				4.5	
t_{en}	Receiver enable time	Driver enabled, See Figure 7			15	ns
		Driver disabled, See Figure 8			6	µs
t_{dis}	Receiver disable time	Driver enabled, See Figure 7			20	ns

PARAMETER MEASUREMENT INFORMATION

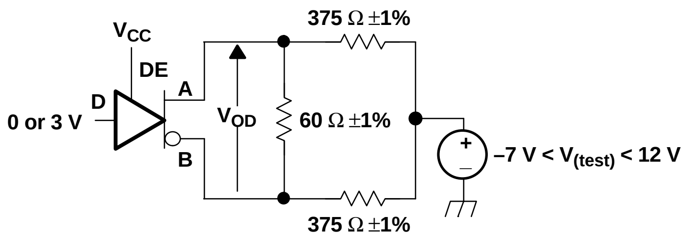
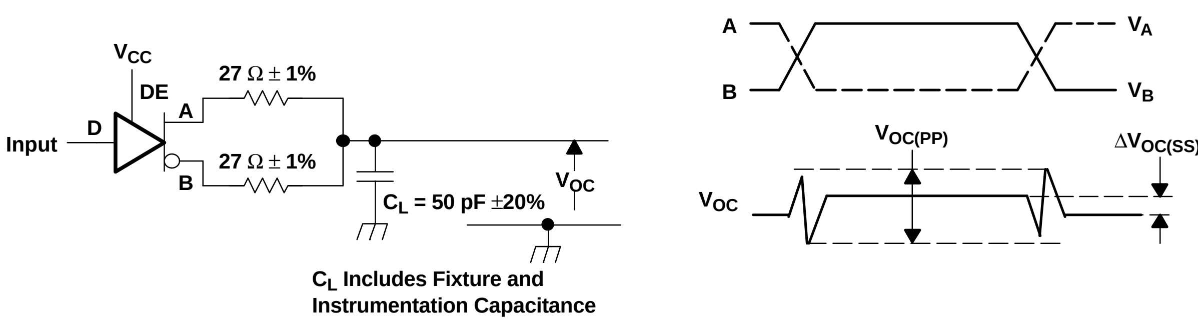
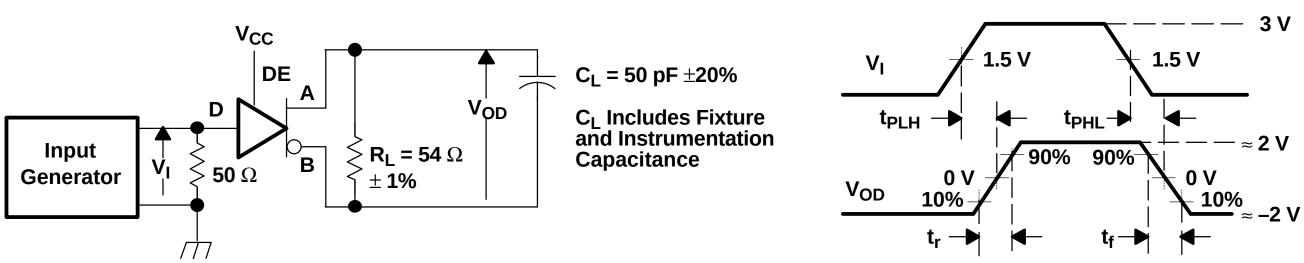


Figure 1. Driver V_{OD} With Common-Mode Loading Test Circuit



Input: PRR = 500 kHz, 50% Duty Cycle, t_r<6ns, t_f<6ns, Z_O = 50 Ω

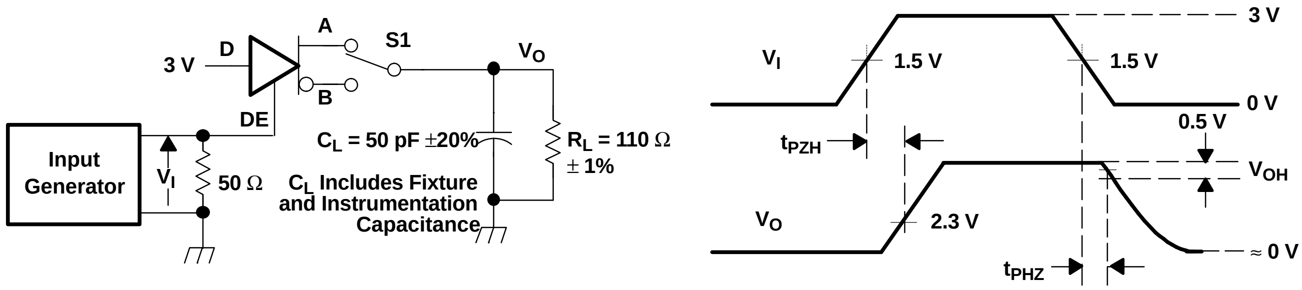
Figure 2. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

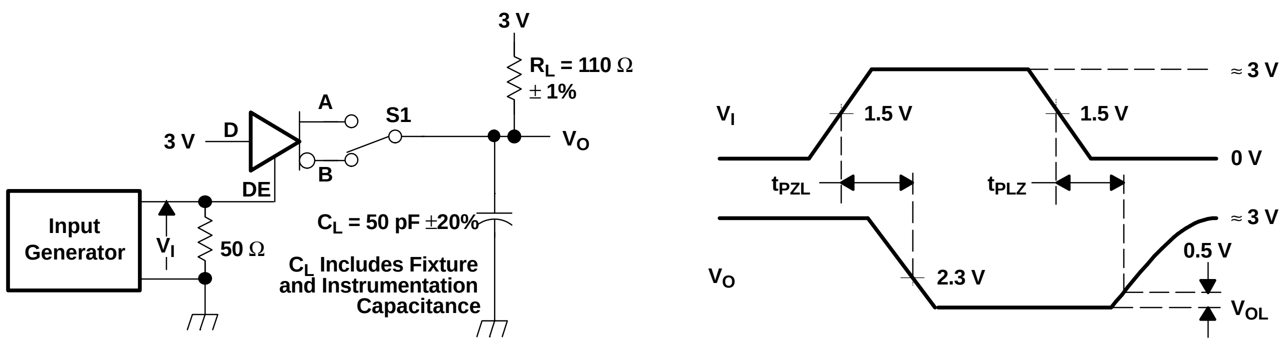
Figure 3. Driver Switching Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



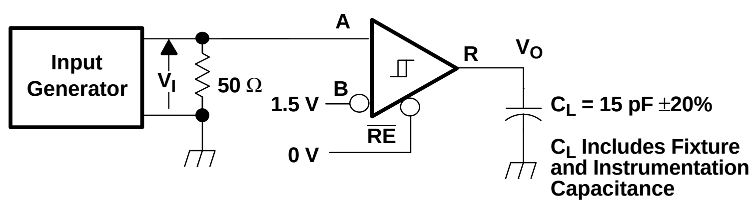
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 4. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 5. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

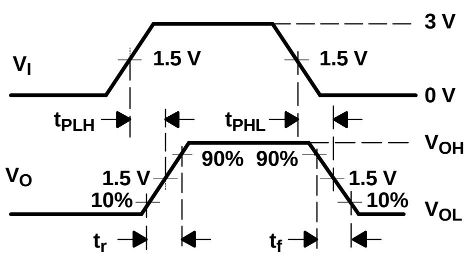


Figure 6. Receiver Switching Test Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

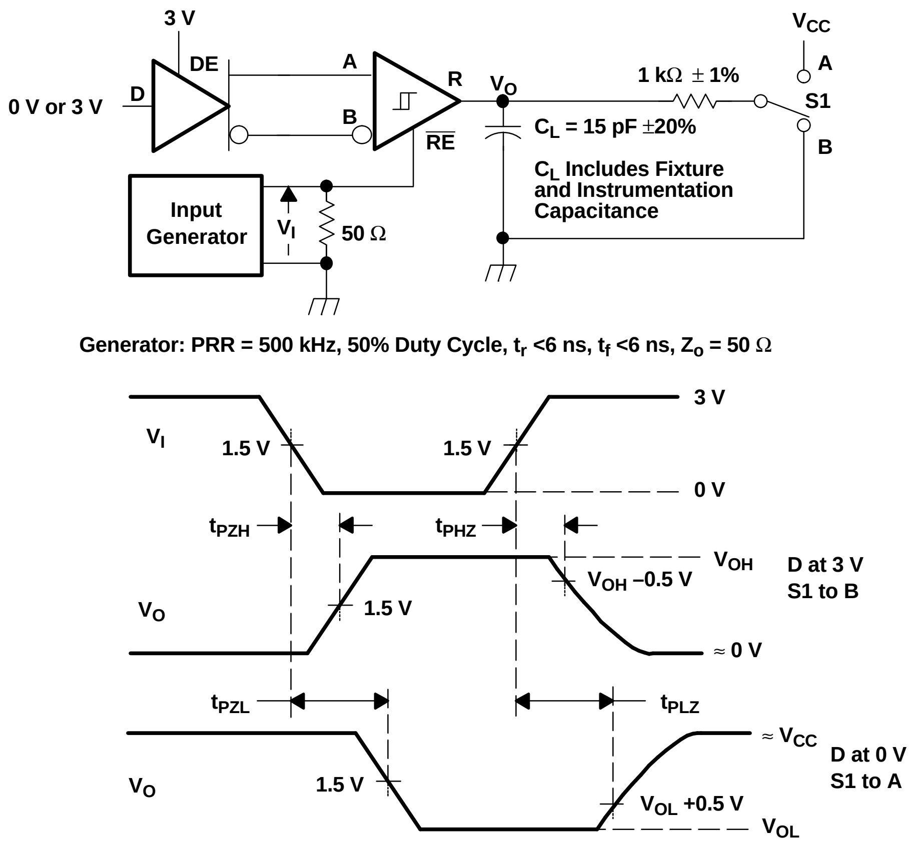


Figure 7. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

Parameter Measurement Information (continued)

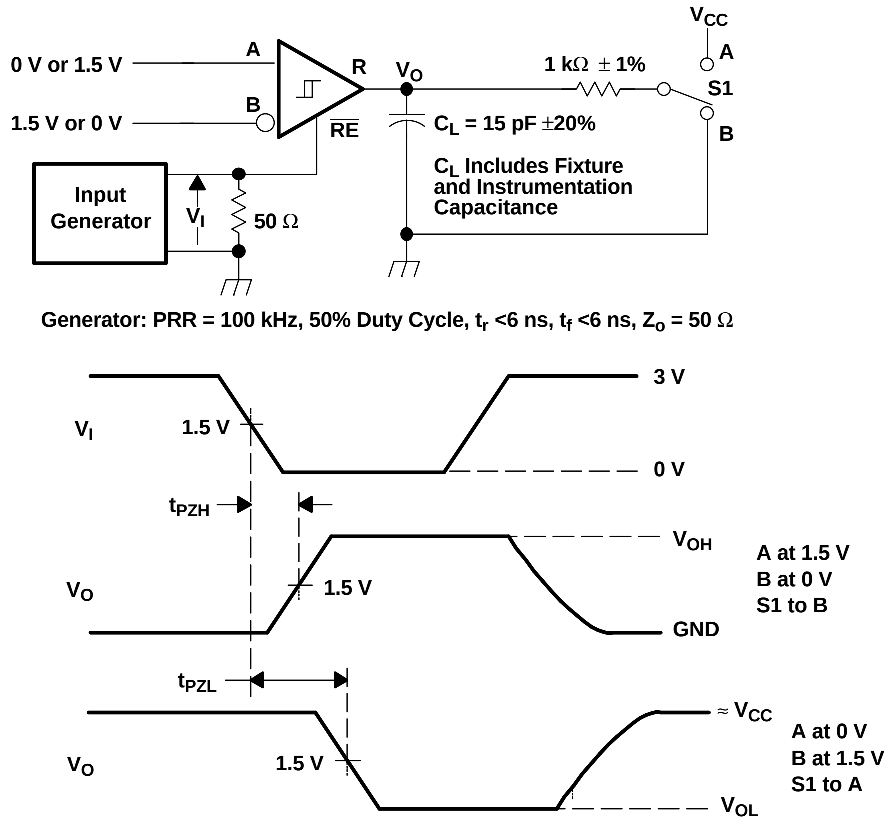


Figure 8. Receiver Enable Time From Standby (Driver Disabled)

DEVICE INFORMATION

Function Tables
DRIVER

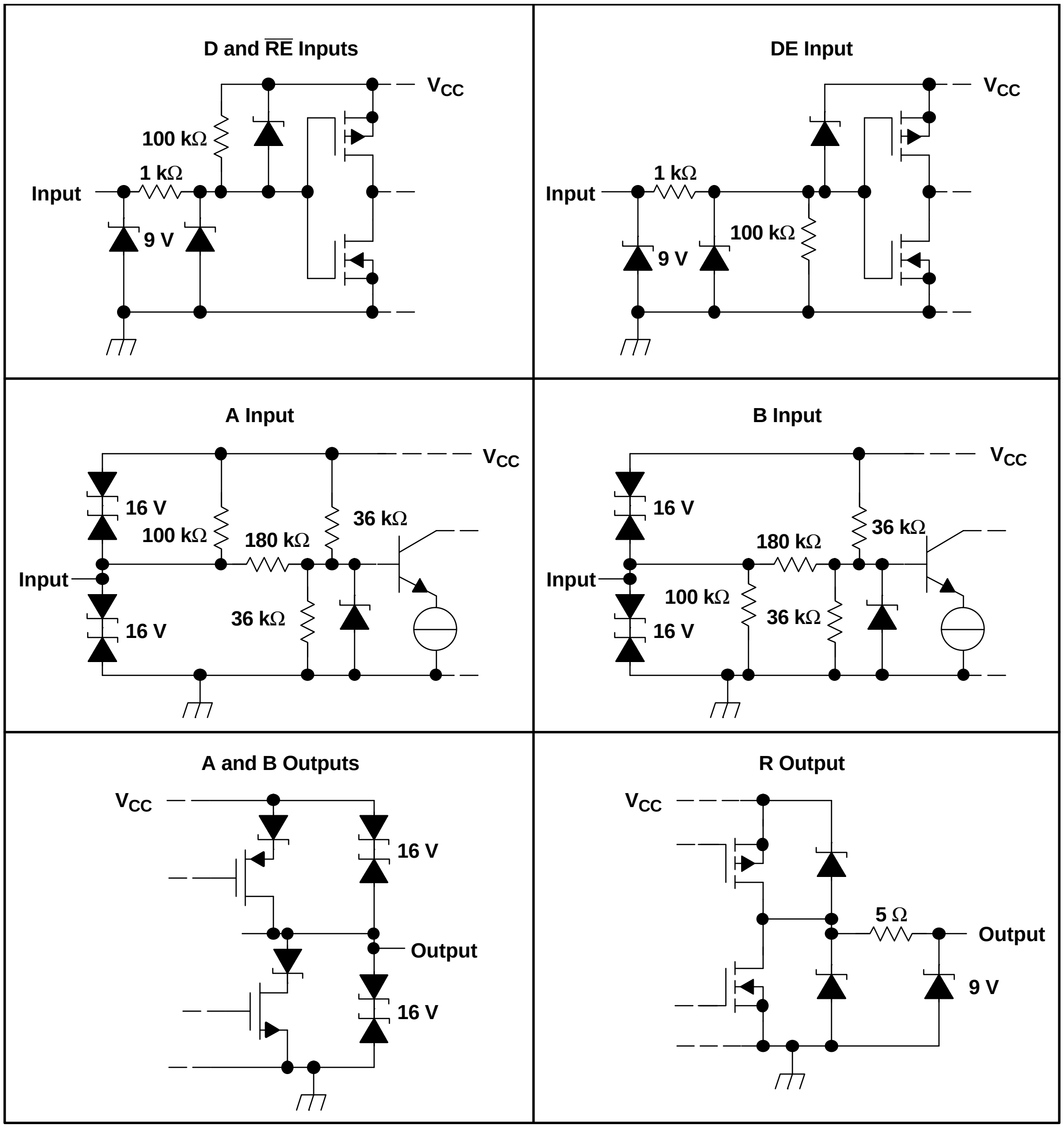
INPUT D	ENABLE DE	OUTPUTS A	OUTPUTS B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

RECEIVER

DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE(1) $\overline{RE}$	OUTPUT(1) R
$V_{ID} \leq -0.2$ V	L	L
$-0.2\text{ V} < V_{ID} < -0.01$ V	L	?
$-0.01\text{ V} \leq V_{ID}$	L	H
X	H	Z
Open Circuit	L	H
Short Circuit	L	H

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

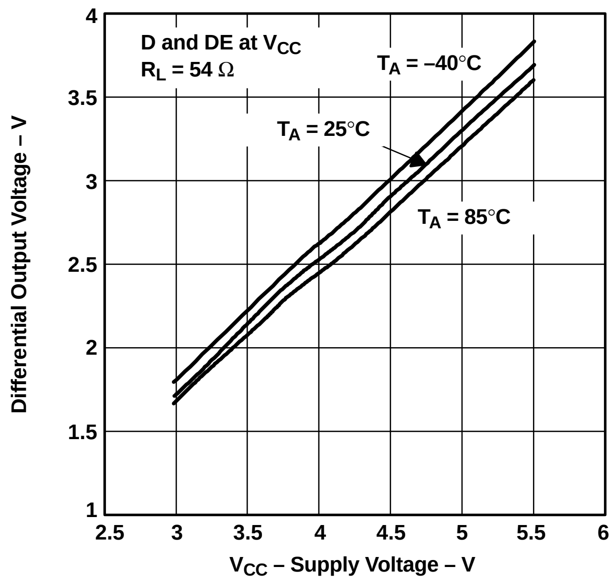


Figure 9.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

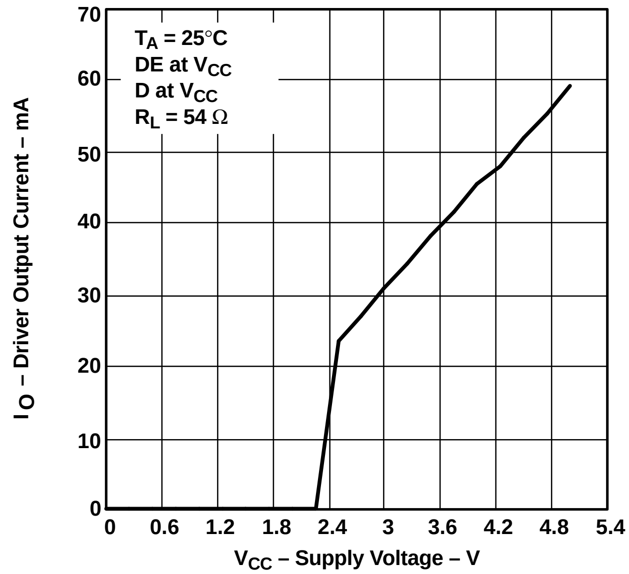


Figure 10.

RMS SUPPLY CURRENT vs SIGNALING RATE

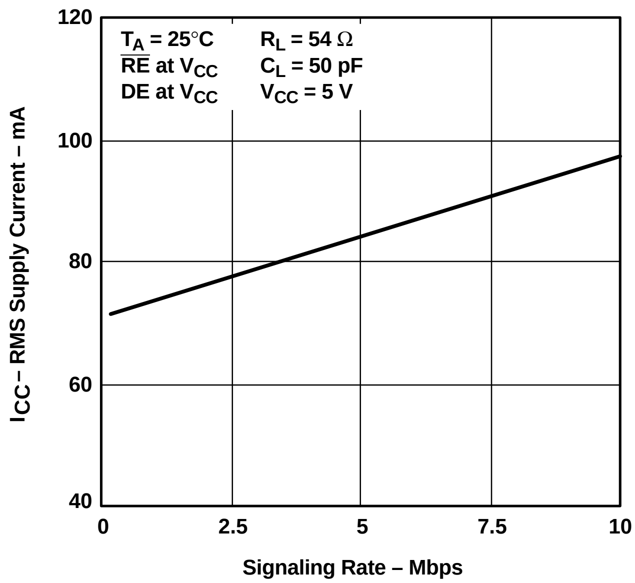


Figure 11.

LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

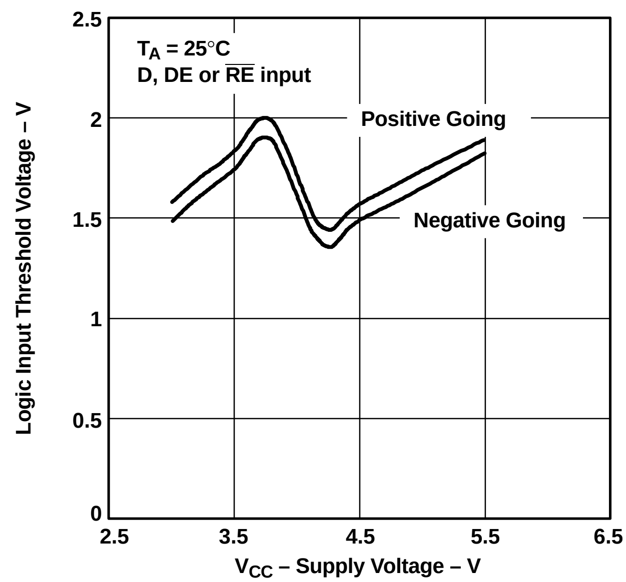


Figure 12.

APPLICATION INFORMATION

As electrical loads are physically distanced from their power source, the effects of supply and return line impedance and the resultant voltage drop must be accounted. If the supply regulation at the load cannot be maintained to the circuit requirements, it forces the use of remote sensing, additional regulation at the load, bigger or shorter cables, or a combination of these. The SN65HVD08 eases this problem by relaxing the supply requirements to allow for more variation in the supply voltage over typical RS-485 transceivers.

SUPPLY SOURCE IMPEDANCE

In the steady state, the voltage drop from the source to the load is simply the wire resistance times the load current as modeled in Figure 13.

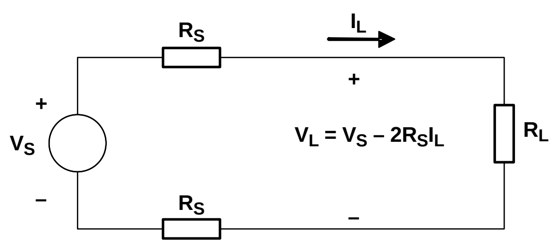


Figure 13. Steady-State Circuit Model

For example, if you were to provide 5-V ±5% supply power to a remote circuit with a maximum load requirement of 0.1 A (one SN65HVD08), the voltage at the load would fall below the 4.5-V minimum of most 5-V circuits with as little as 5.8 m of 28-GA conductors. Table 1 summarizes wire resistance and the length for 4.5 V and 3 V at the load with 0.1 A of load current. The maximum lengths would scale linearly for higher or lower load currents.

Table 1. Maximum Cable Lengths for Minimum Load Voltages at 0.1 A Load

WIRE SIZE	RESISTANCE	4.5 V LENGTH AT 0.1 A	3-v LENGTH AT 0.1 A
28 Gage	0.213 Ω/m	5.8 m	41.1 m
24 Gage	0.079 Ω/m	15.8 m	110.7 m
22 Gage	0.054 Ω/m	23.1 m	162.0 m
20 Gage	0.034 Ω/m	36.8 m	257.3 m
18 Gage	0.021 Ω/m	59.5 m	416.7 m

Under dynamic load requirements, the distributed inductance and capacitance of the power lines may not be ignored and decoupling capacitance at the load is required. The amount depends upon the magnitude and frequency of the load current change but, if only powering the SN65HVD08, a 0.1 µF ceramic capacitor is usually sufficient.

OPTO-ISOLATED DATA BUSES

Long RS-485 circuits can create large ground loops and pick up common-mode noise voltages in excess of the range tolerated by standard RS-485 circuits. A common remedy is to provide galvanic isolation of the data circuit from earth or local grounds.

Transformers, capacitors, or phototransistors most often provide isolation of the bus and the local node. Transformers and capacitors require changing signals to transfer the information over the isolation barrier and phototransistors (opto-isolators) can pass steady-state signals. Each of these methods incurs additional costs and complexity, the former in clock encoding and decoding of the data stream and the latter in requiring an isolated power supply.

Quite often, the cost of isolated power is repeated at each node connected to the bus as shown in Figure 14. The possibly lower-cost solution is to generate this supply once within the system and then distribute it along with the data line(s) as shown in Figure 15.

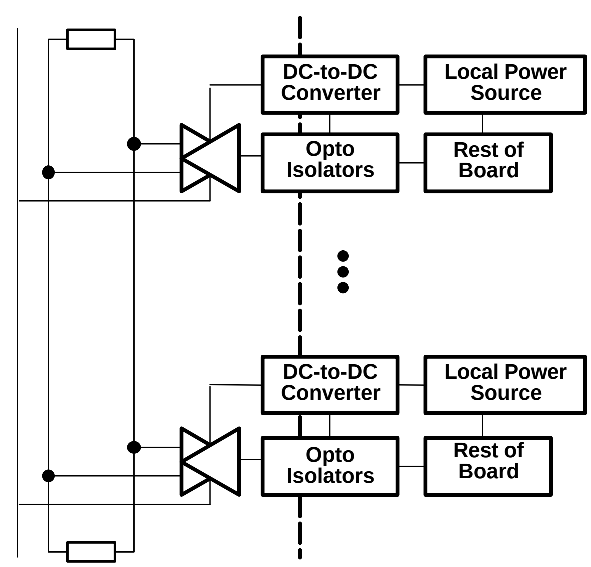


Figure 14. Isolated Power at Each Node

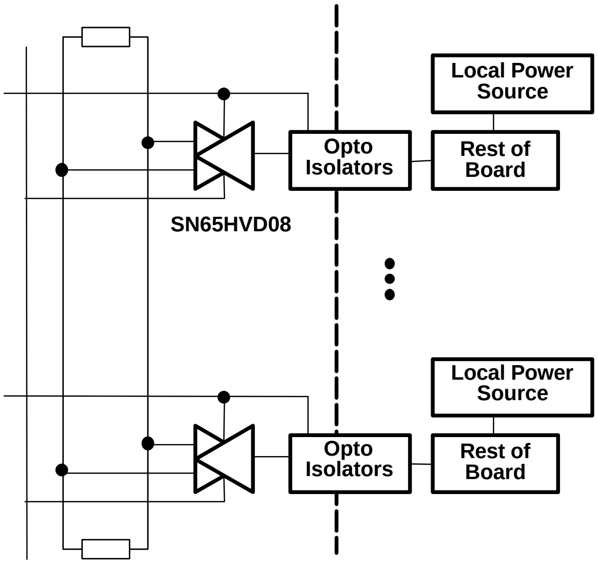


Figure 15. Distribution of Isolated Power

The features of the SN65HVD08 are particularly good for the application of Figure 15. Due to added supply source impedance, the low quiescent current requirements and wide supply voltage tolerance allow for the poorer load regulation.

AN OPTO ALTERNATIVE

The ISO150 is a two-channel, galvanically isolated data coupler capable of data rates of 80 Mbps. Each channel can be individually programmed to transmit data in either direction.

Data is transmitted across the isolation barrier by coupling complementary pulses through high-voltage 0.4-pF capacitors. Receiver circuitry restores the pulses to standard logic levels. Differential signal transmission rejects isolation-mode voltage transients up to 1.6 kV/ms.

ISO150 avoids the problems commonly associated with opto-couplers. Optically-isolated couplers require high current pulses and allowance must be made for LED aging. The ISO150's Bi-CMOS circuitry operates at 25 mW per channel with supply voltage range matching that of the SN65HVD08 of 3 V to 5.5 V.

Figure 16 shows a typical circuit.

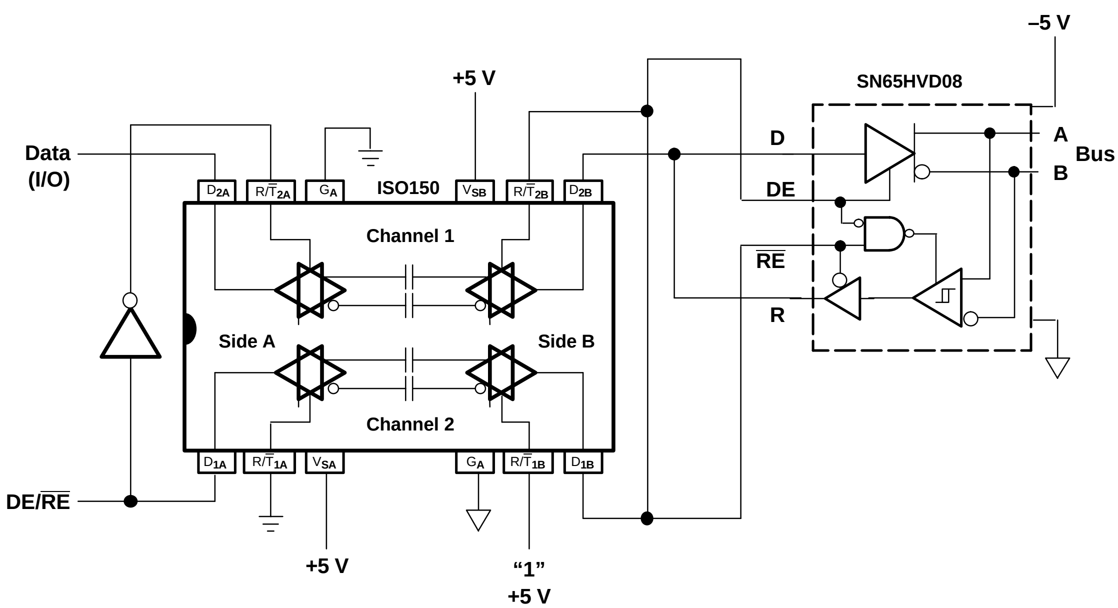
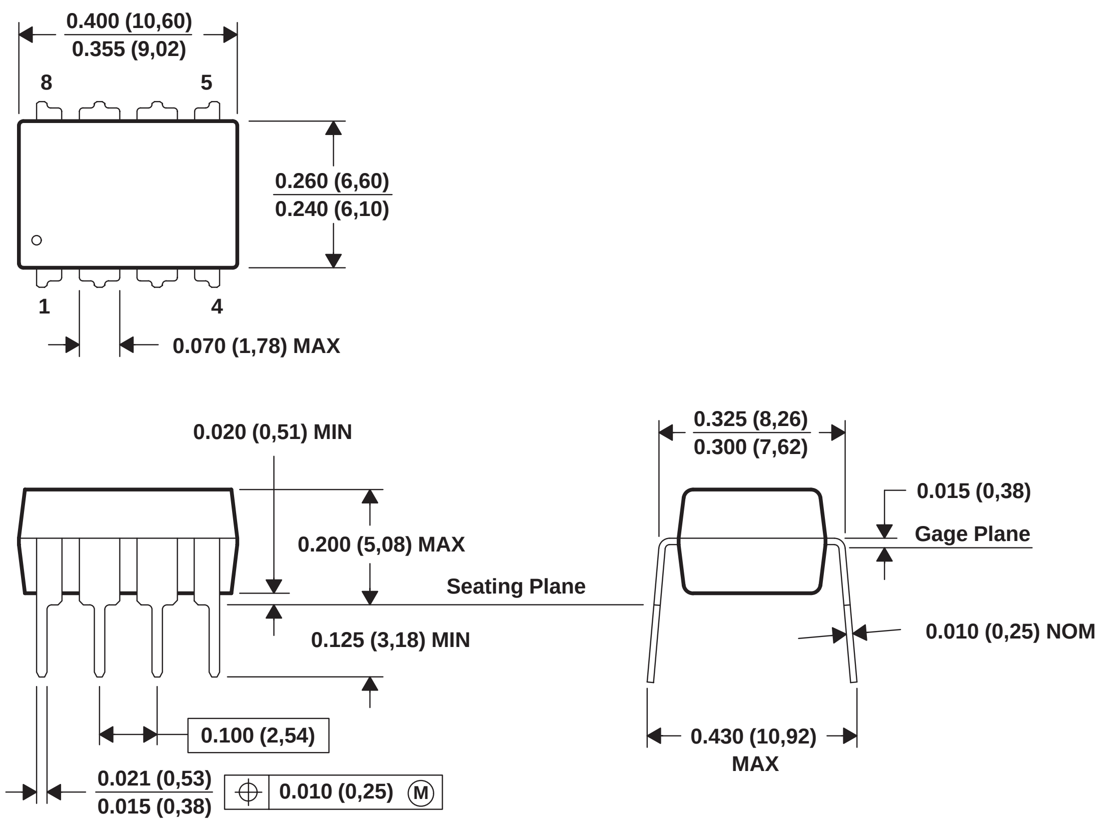


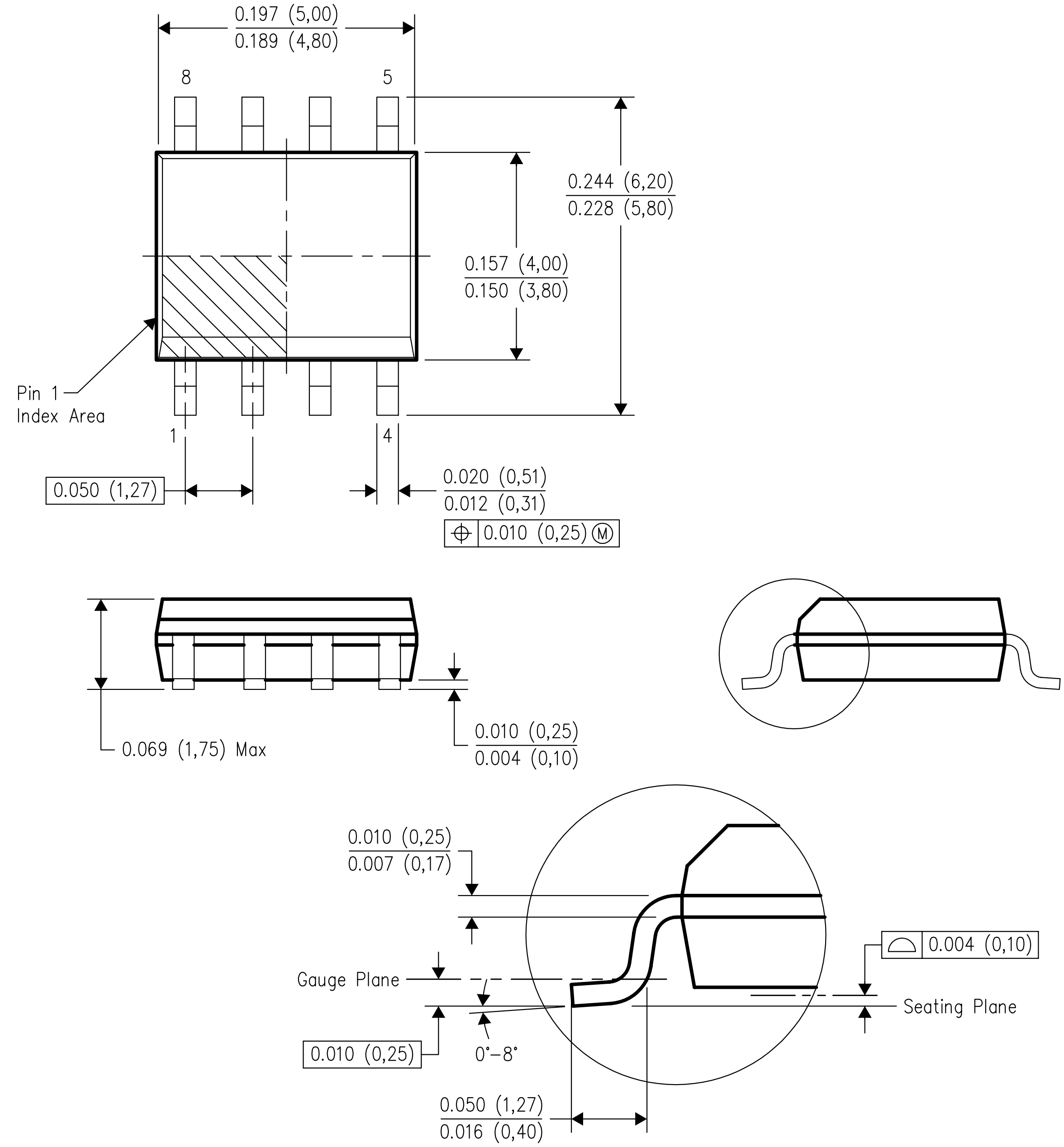
Figure 16. Isolated RS-485 Interface

P (R-PDIP-T8) PLASTIC DUAL-IN-LINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AA.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265