

HALF-DUPLEX RS-485 TRANSCEIVER

FEATURES

- Bus-Pin ESD Protection Up to 15 kV
- 1/2 Unit Load—Up to 64 Nodes on a Bus
- Bus Open Failsafe Receiver
- Available in Small MSOP-8 Package
- Meets or Exceeds the Requirements of the TIA/EIA-485A Standard
- Industry-Standard SN75176 Footprint

APPLICATIONS

- Motor Control
- Power Inverters
- Industrial Automation
- Building Automation Networks
- Industrial Process Control
- Battery-Powered Applications
- Telecommunications Equipment

DESCRIPTION

The SN65HVD485E is a half-duplex transceiver designed for RS-485 data bus networks. Powered by a 5-V supply, it is fully compliant with the TIA/EIA-485A standard. This device is suitable for data transmission up to 10 Mbps over long twisted-pair cables and is designed to operate with very low supply current, typically less than 2 mA, exclusive of the load. When in the inactive shutdown mode, the supply current drops below 1 mA.

The wide common-mode range and high ESD protection levels of this device make it suitable for demanding applications such as, electrical inverters, status/command signals across telecom racks, cabled chassis interconnects, and industrial automation networks where noise tolerance is essential. The SN65HVD485E matches the industry-standard footprint of the SN75176. Power-on reset circuits keep the outputs in a high-impedance state until the supply voltage has stabilized. A thermal shutdown function protects the device from damage due to system fault conditions. The SN65HVD485E is characterized for operation from -40°C to 85°C air temperature.

Improved Replacement for:

PART NUMBER	REPLACE WITH
ADM485	HVD485E: Better ESD protection (± 15 kV vs. unspecified) Faster signaling rate (10 Mbps vs. 5 Mbps) More nodes on a bus (64 vs. 32) Wider power supply tolerance (10% vs. 5%)
SP485E	HVD485E: More nodes on a bus (64 vs. 32) Wider power supply tolerance (10% vs. 5%)
LMS485E	HVD485E: Higher signaling rate (10 Mbps vs. 2.5 Mbps) More nodes on a bus (64 vs. 32) Wider power supply tolerance (10% vs. 5%)
DS485	HVD485E: Higher signaling rate (10 Mbps vs. 2.5 Mbps) Better ESD (± 15 kV vs. ± 2 kV) More nodes on a bus (64 vs. 32) Wider power supply tolerance (10% vs. 5%)
LTC485	HVD485E: Better ESD (± 15 kV vs. ± 2 kV) Wider power supply tolerance (10% vs. 5%)
MAX485E	HVD485E: Higher signaling rate (10 Mbps vs. 2.5 Mbps) More nodes on a bus (64 vs. 32) Wider power supply tolerance (10% vs. 5%)
ST485E	HVD485E: Higher signaling rate (10 Mbps vs. 5 Mbps) Wider power supply tolerance (10% vs. 5%)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T _A	PACKAGE TYPE		
	P	D ⁽¹⁾	DGK ⁽²⁾
-40°C to 85°C	SN65HVD485EP Marked as 65HVD485	SN65HVD485ED Marked as VP485	SN65HVD485EDGK Marked as NWJ

(1) The D package is available taped and reeled. Add an R suffix to the device type (i.e., SN65HVD485EDR).

(2) The DGK package is available taped and reeled. Add an R suffix to the device type (i.e., SN65HVD485EDGKR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾ (2)

	UNITS
Supply voltage range, V _{CC}	-0.5 V to 7 V
Voltage range at A or B	-9 V to 14 V
Voltage range at any logic pin	-0.3 V to V _{CC} + 0.3 V
Receiver output current	-24 mA to 24 mA
Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 13)	-50 V to 50 V
Storage temperature range	-65°C to 130°C
Junction temperature, T _J	170°C
Continuous total power dissipation	Refer to Package Dissipation Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

PACKAGE DISSIPATION RATINGS

PACKAGE	JEDEC BOARD MODEL	T _A < 25°C POWER RATING	DERATING FACTOR ⁽³⁾ ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
D	Low k ⁽¹⁾	507 mW	4.82 mW/°C	289 mW	217 mW
	High k ⁽²⁾	824 mW	7.85 mW/°C	471 mW	353 mW
P	Low k ⁽¹⁾	686 mW	6.53 mW/°C	392 mW	294 mW
DGK	Low k ⁽¹⁾	394 mW	3.76 mW/°C	255 mW	169 mW
	High k ⁽²⁾	583 mW	5.55 mW/°C	333 mW	250 mW

(1) In accordance with the low-k thermal metric definitions of EIA/JESD51-3

(2) In accordance with the high-k thermal metric definitions of EIA/JESD51-7

(3) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

	MIN	TYP	MAX	UNIT
Supply voltage, V _{CC}	4.5		5.5	V
Input voltage at any bus terminal (separately or common mode), V _I	-7		12	V
High-level input voltage (D, DE, or \overline{RE} inputs), V _{IH}	2		V _{CC}	V
Low-level input voltage (D, DE, or \overline{RE} inputs), V _{IL}	0		0.8	V
Differential input voltage, V _{ID}	-12		12	V
Output current, I _O	Driver		60	mA
	Receiver		8	
Differential load resistance, R _L	54	60		Ω
Signaling rate, 1/t _{UI}	0		10	Mbps
Operating free-air temperature, T _A	-40		85	°C
Junction temperature, T _J ⁽²⁾	-40		130	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.

(2) See *thermal characteristics* table for information on maintenance of this specification for the DGK package.

SUPPLY CURRENT

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
I _{CC}	Driver and receiver enabled	D at V _{CC} or open or 0V, DE at V _{CC} , RE at 0 V, No load			2	mA
	Driver and receiver disabled	D at V _{CC} or open, DE at 0 V, RE at V _{CC}			1	mA

(1) All typical values are at 25°C and with a 5-V supply.

ELECTROSTATIC DISCHARGE PROTECTION

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
Human body model		Bus terminals and GND		±15		kV
Human body model ⁽²⁾		All pins		±4		kV
Charged-device-model ⁽³⁾		All pins		±1		kV

(1) All typical values at 25°C

(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.

(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
MOD I	Differential output voltage	I _O = 0, No load	3	4.3		V
		R _L = 54 Ω, See Figure 1	1.5	2.3		
		V _{TEST} = -7 V to 12 V, See Figure 2	1.5			
ΔV _{OD I}	Change in magnitude of differential output voltage	See Figure 1 and Figure 2	-0.2	0	0.2	V
V _{OC(SS)}	Steady-state common-mode output voltage	See Figure 3	1	2.6	3	V
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage		-0.1	0	0.1	
V _{OC(PP)}		See Figure 3		500		mV
I _{OZ}	High-impedance output current	See receiver input currents				μA
I _I	Input current	D, DE	-100		100	
I _{OS}	Short-circuit output current	-7 V ≤ V _O ≤ 12 V, See Figure 7	-250		250	mA

(1) All typical values are at 25°C and with a 5V-supply.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	R _L = 54 Ω, C _L = 50 pF, See Figure 4			30	ns
t _{PHL}	Propagation delay time, high-to-low-level output				30	
t _r	Differential output signal rise time				25	
t _f	Differential output signal fall time				25	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})				5	
t _{PZH}	Propagation delay time, high-impedance-to-high-level output	R _L = 110 Ω, RE at 0 V, See Figure 5			150	ns
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output			100		
t _{PZL}	Propagation delay time, high-impedance-to-low-level output	R _L = 110 Ω, RE at 0 V			150	ns
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 6			100	
t _{PZH(SHDN)}	Propagation delay time, shutdown-to-high-level output	R _L = 110 Ω, RE at V _{CC} , See Figure 5			2600	ns
t _{PZL(SHDN)}	Propagation delay time, shutdown-to-low-level output	R _L = 110 Ω, RE at V _{CC} , See Figure 6			2600	ns

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	I _O = -8 mA		-85	-10	mV
V _{IT-}	Negative-going input threshold voltage	I _O = 8 mA	-200	-115		mV
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})			30		mV
V _{OH}	High-level output voltage	V _{ID} = 200 mV, I _{OH} = -8 mA, See Figure 8	4	4.6		V
V _{OL}	Low-level output voltage	V _{ID} = -200 mV, I _{OH} = 8 mA, See Figure 8		0.15	0.4	V
I _{OZ}	High-impedance-state output current	V _O = 0 to V _{CC} , $\overline{RE} = V_{CC}$	-1		1	μA
I _I	Bus input current	V _{IH} = 12 V, V _{CC} = 5 V			0.5	mA
		V _{IH} = 12 V, V _{CC} = 0			0.5	
		V _{IH} = -7 V, V _{CC} = 5 V	-0.4			
		V _{IH} = -7 V, V _{CC} = 0	-0.4			
I _{IH}	High-level input current (\overline{RE})	V _{IH} = 2 V	-60	-30		μA
I _{IL}	Low-level input current (\overline{RE})	V _{IL} = 0.8 V	-60	-30		μA
C _{diff}	Differential input capacitance	V _I = 0.4 sin(4E6πt) + 0.5 V, DE at 0 V		7		pF

(1) All typical values are at 25°C and with a 5-V supply.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	Propagation delay time, low-to-high-level output	V _{ID} = -1.5 V to 1.5 V, C _L = 15 pF, See Figure 9			200	ns
t _{PHL}	Propagation delay time, high-to-low-level output				200	
t _{sk(p)}	Pulse skew (t _{PHL} - t _{PLH})			8		
t _r	Output signal rise time	C _L = 15 pF, DE at 3 V, See Figure 10 and Figure 11			3	ns
t _f	Output signal fall time				3	
t _{PZH}	Output enable time to high level	C _L = 15 pF, DE at 3 V, See Figure 10 and Figure 11			50	ns
t _{PZL}	Output enable time to low level				50	
t _{PHZ}	Output enable time from high level				50	
t _{PLZ}	Output enable time from low level				50	
t _{PZH(SHDN)}	Propagation delay time, shutdown-to-high-level output	C _L = 15 pF, DE at 0 V, See Figure 12			3500	μs
t _{PZL(SHDN)}	Propagation delay time, shutdown-to-low-level output				3500	

PARAMETER MEASUREMENT INFORMATION

NOTE: Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle. $Z_0 = 50 \Omega$ (unless otherwise specified).

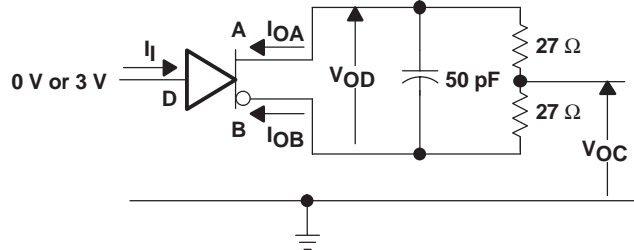


Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

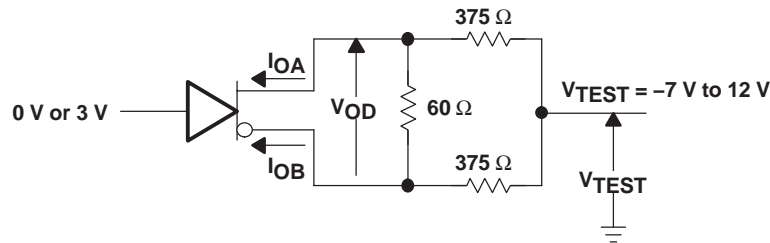


Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading

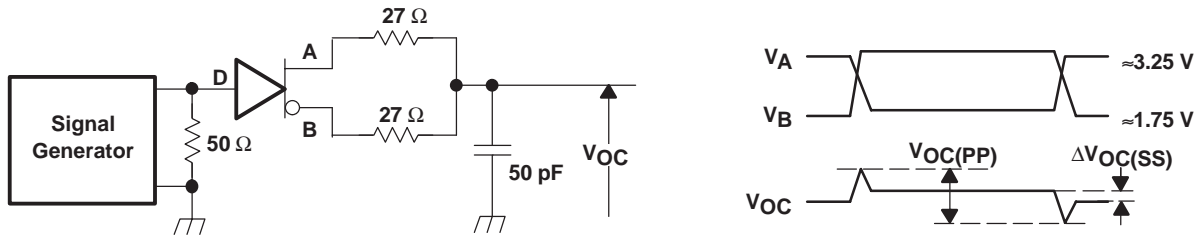


Figure 3. Driver V_{OC} Test Circuit and Waveforms

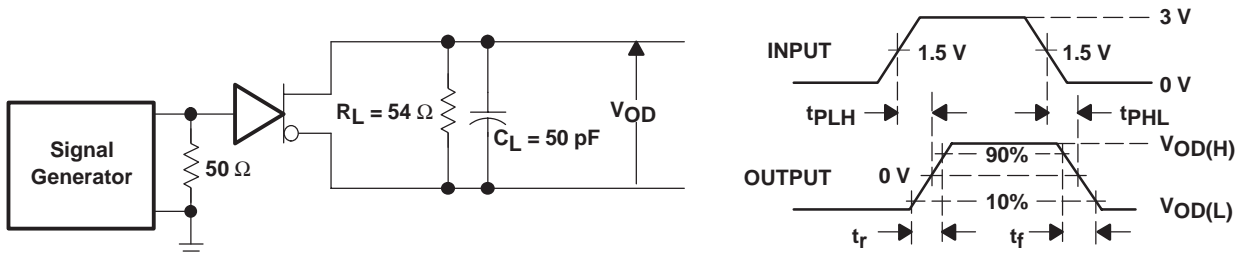


Figure 4. Driver Switching Test Circuit and Waveforms

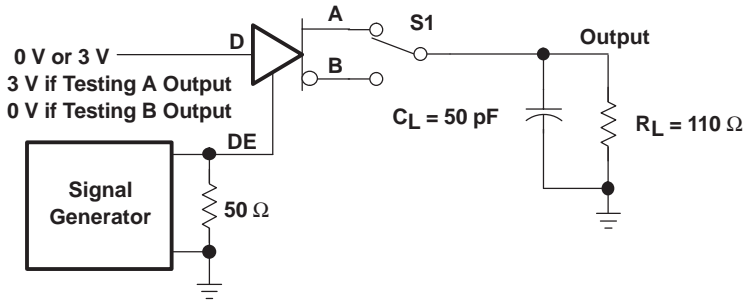


Figure 5. Driver Enable/Disable Test Circuit and Waveforms, High Output

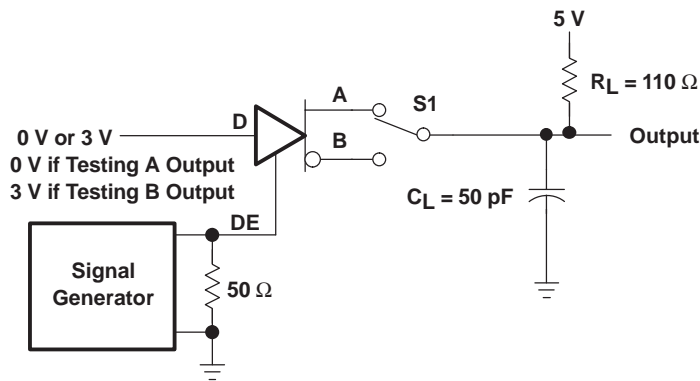


Figure 6. Driver Enable/Disable Test Circuit and Waveforms, Low Output

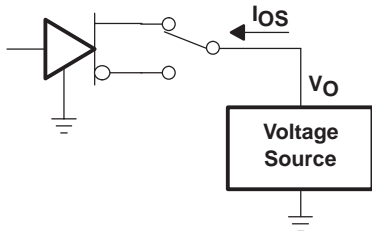


Figure 7. Driver Short-Circuit Test

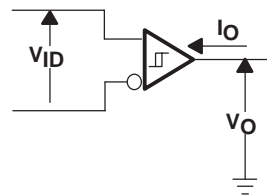


Figure 8. Receiver Parameter Definitions

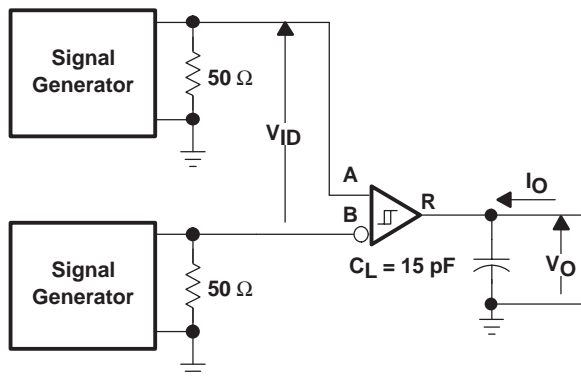


Figure 9. Receiver Switching Test Circuit and Waveforms

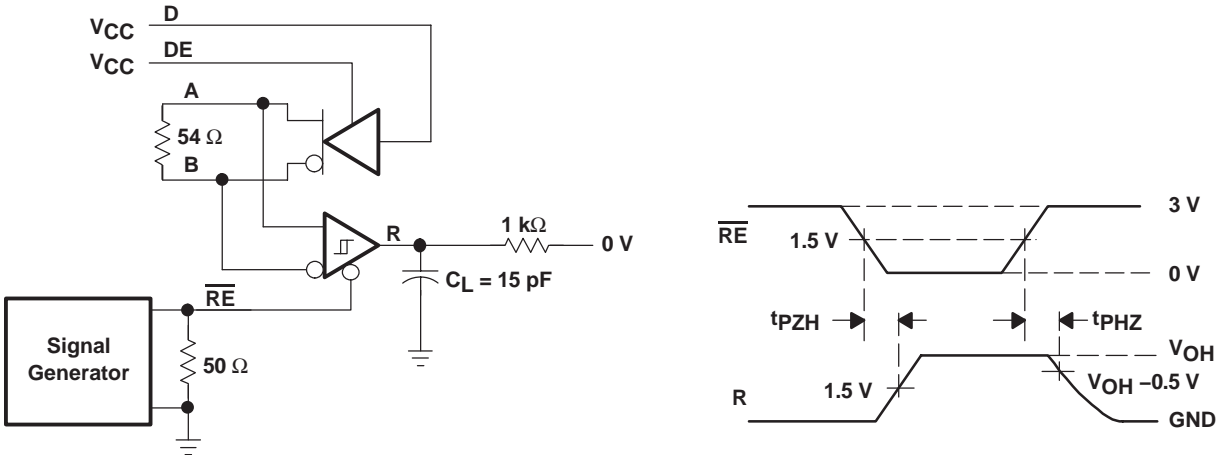


Figure 10. Receiver Enable/Disable Test Circuit and Waveforms, Data Output High

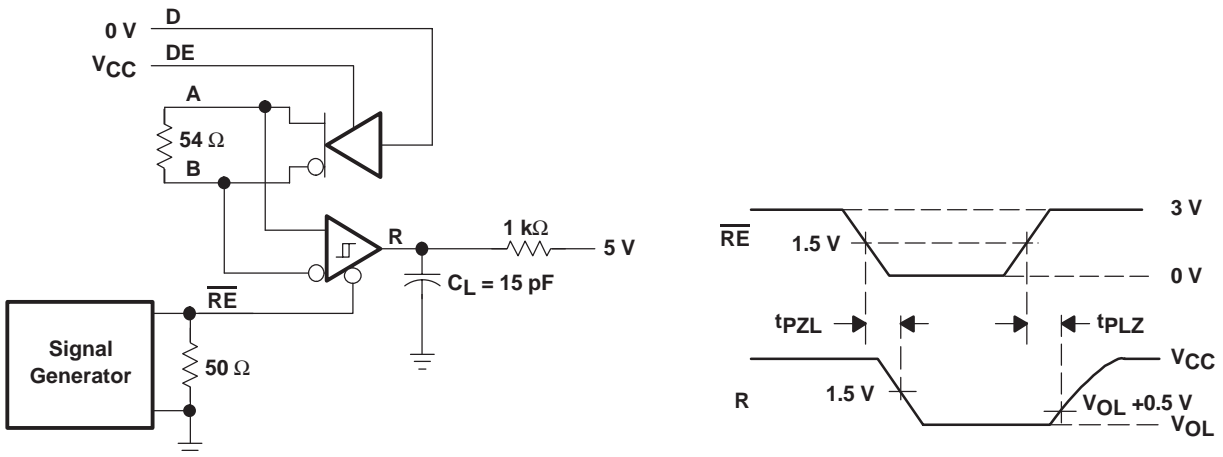


Figure 11. Receiver Enable/Disable Test Circuit and Waveforms, Data Output Low

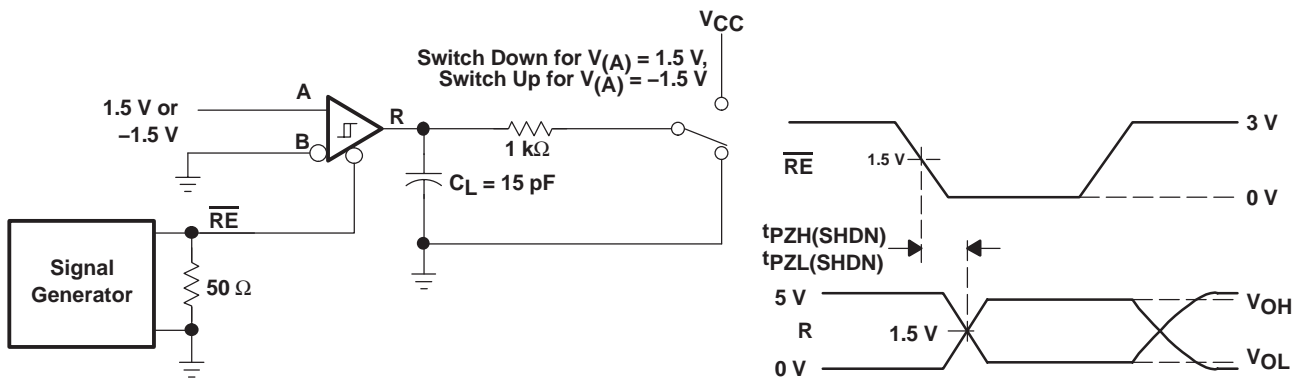


Figure 12. Receiver Enable From Shutdown Test Circuit and Waveforms

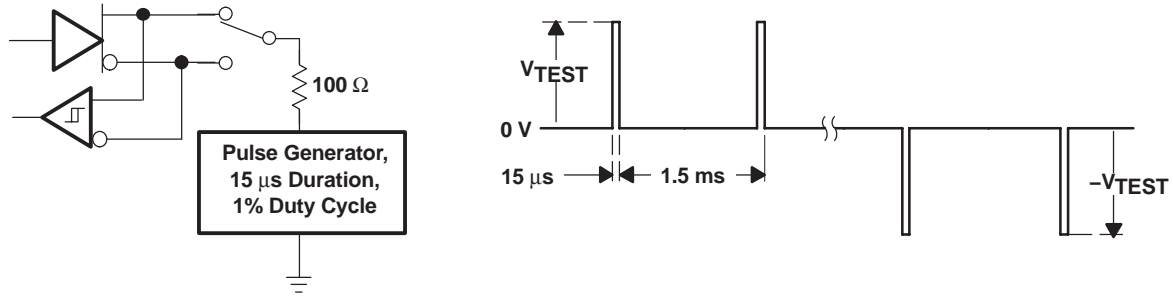
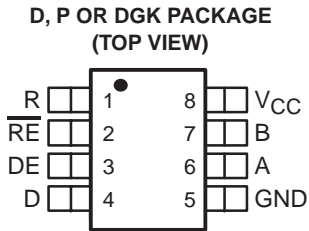


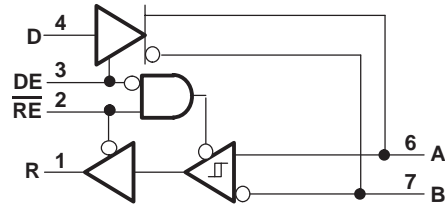
Figure 13. Test Circuit and Waveforms, Transient Over-Voltage Test

DEVICE INFORMATION

PIN ASSIGNMENTS



LOGIC DIAGRAM (POSITIVE LOGIC)

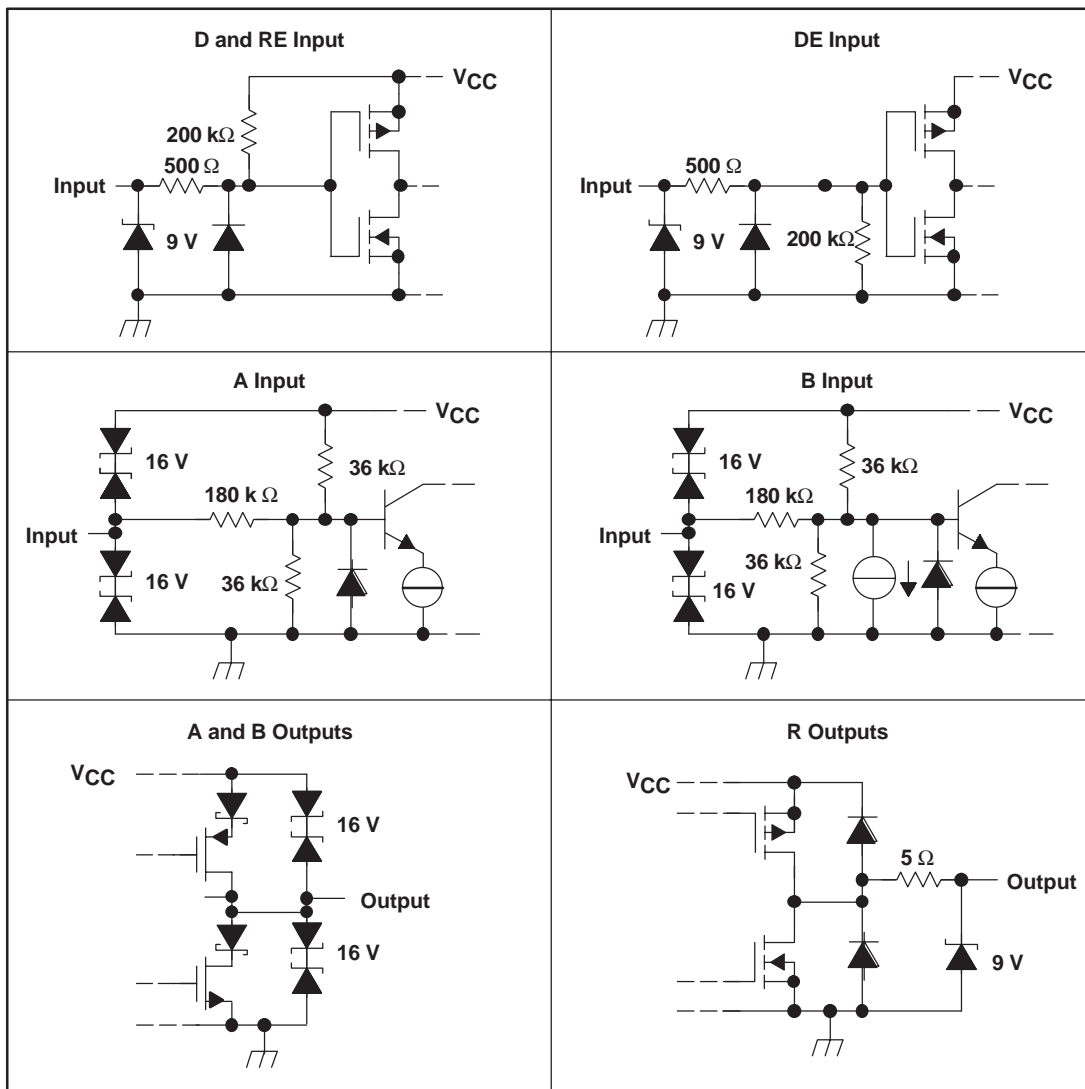


FUNCTION TABLE

DRIVER				RECEIVER		
INPUT D	ENABLE DE	OUTPUTS		DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE \overline{RE}	OUTPUT R
		A	B			
H	H	H	L	$V_{ID} \leq -0.2 V$	L	L
L	H	L	H	$-0.2 V < V_{ID} < -0.01 V$	L	?
X	L	Z	Z	$-0.01 V \leq V_{ID}$	L	H
Open	H	H	L	X	H	Z
X	Open	Z	Z	Open circuit	L	H
				X	Open	Z

NOTE: H= high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



THERMAL CHARACTERISTICS

DGK Package

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ _{JA}	Junction-to-ambient thermal resistance ⁽¹⁾		266		°C/W
	Low-k ⁽²⁾ board, no air flow				
	High-k ⁽³⁾ board, no air flow		180		
θ _{JB}	Junction-to-board thermal resistance		108		°C/W
θ _{JC}	Junction-to-case thermal resistance		66		
P(AVG)	Average power dissipation			219	mW
T _A	Ambient air temperature	R _L = 54 Ω, Input to D is a 10 Mbps 50% duty cycle square wave V _{CC} at 5.5 V, T _J = 130°C			
		JEDEC High K board model	-40	93	°C
	JEDEC Low K board model	-40	75	°C	
T _{SD}	Thermal shut-down junction temperature		165		°C

(1) See TI application note literature number SZZA003, *Package Thermal Characterization Methodologies*, for an explanation of this parameter.
 (2) JESD51-3 *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
 (3) JESD51-7 *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

TYPICAL CHARACTERISTICS

BUS INPUT CURRENT
vs
BUS INPUT VOLTAGE

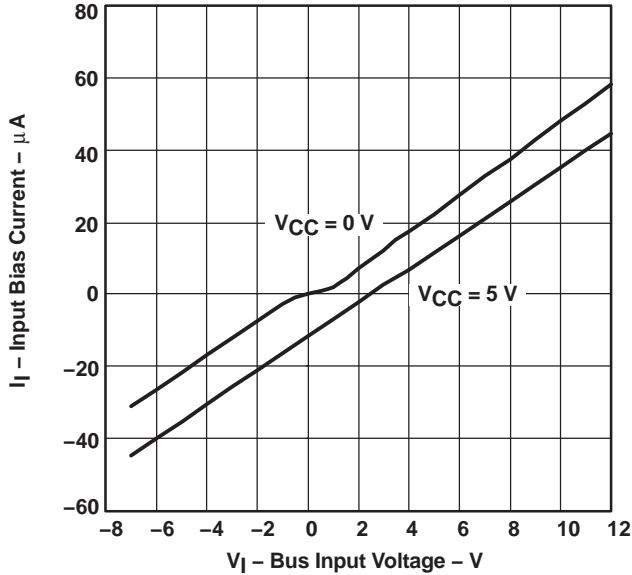


Figure 14

DRIVER DIFFERENTIAL OUTPUT VOLTAGE
vs
DIFFERENTIAL OUTPUT CURRENT

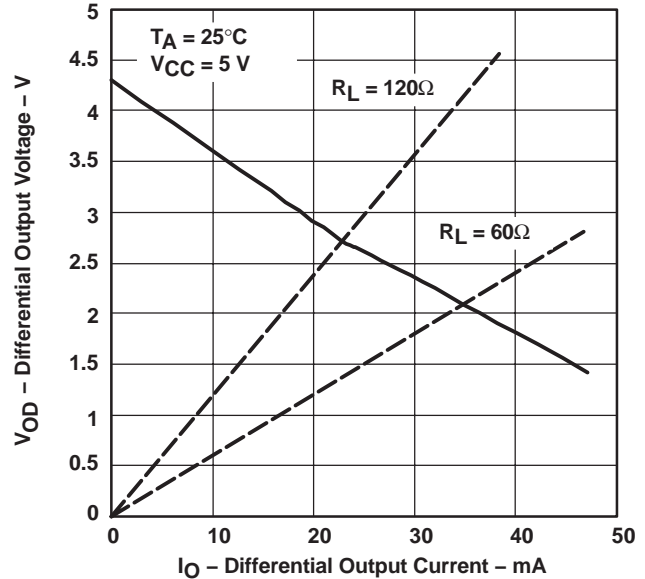
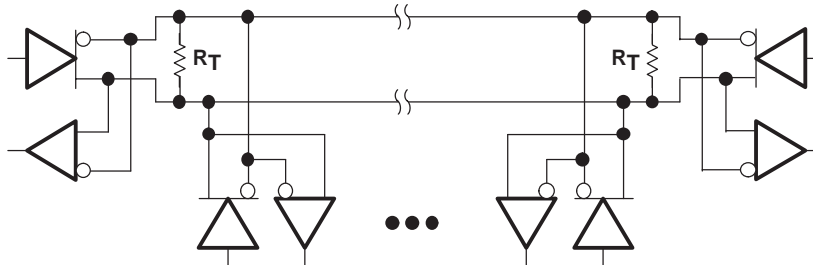


Figure 15

APPLICATION INFORMATION



NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 16. Typical Application Circuit

POWER USAGE IN AN RS-485 TRANSCEIVER

Power consumption is a concern in many applications. Power supply current is delivered to the bus load as well as to the transceiver circuitry. For a typical RS-485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes, plus the termination resistors at each end of the bus.

The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485-A standard defines a unit load as allowing up to 1 mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32 mA. The HVD485E is rated as a 1/2 unit load device, so up to 64 can be connected on a bus.

The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 120- Ω resistor at each end, this sums to 25 mA differential output current whenever the bus is active. Typically the HVD485E can drive more than 25 mA to a 60 Ω load, resulting in a differential output voltage higher than the minimum required by the standard. (See Figure 15.)

Supply current increases with signaling rate primarily due to the totum pole outputs of the driver. When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting and this creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

THERMAL CHARACTERISTICS OF IC PACKAGES

Θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

Θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

Θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. Θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives *best case* in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in Θ_{JA} can be measured between these two test cards

Θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

Θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with Θ_{JB} in 1-dimensional thermal simulation of a package system.

Θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. Θ_{JB} is only defined for the high-k test card.

Θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see figure 18).

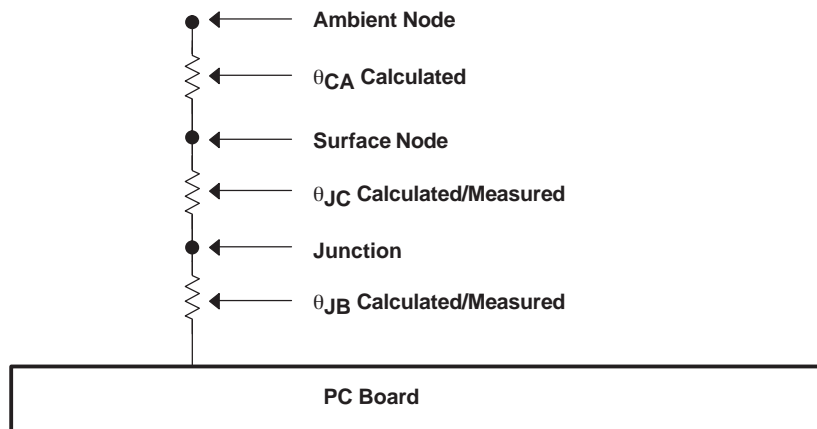


Figure 17. Thermal Resistance

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



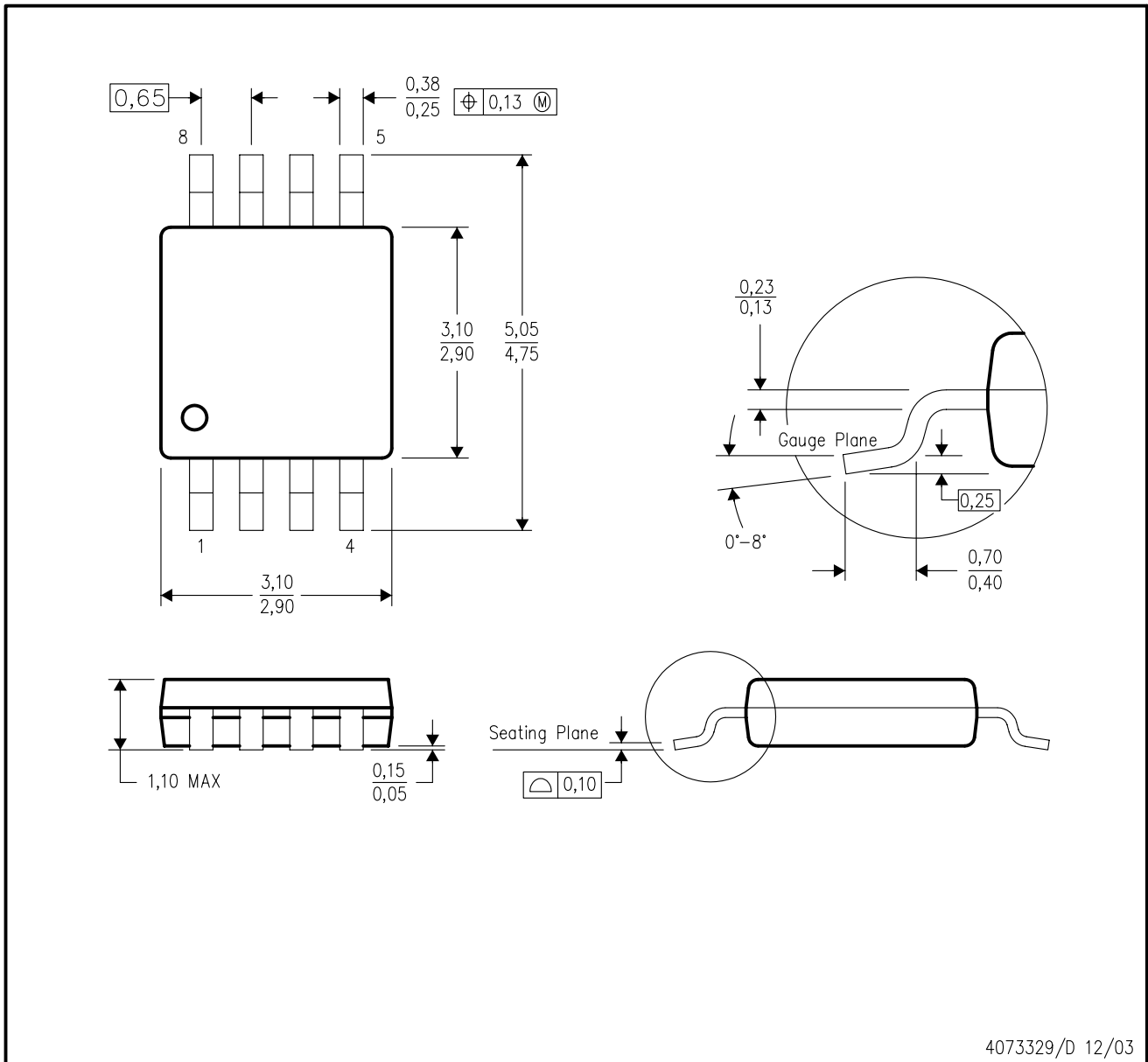
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



DGK (S-PDSO-G8)

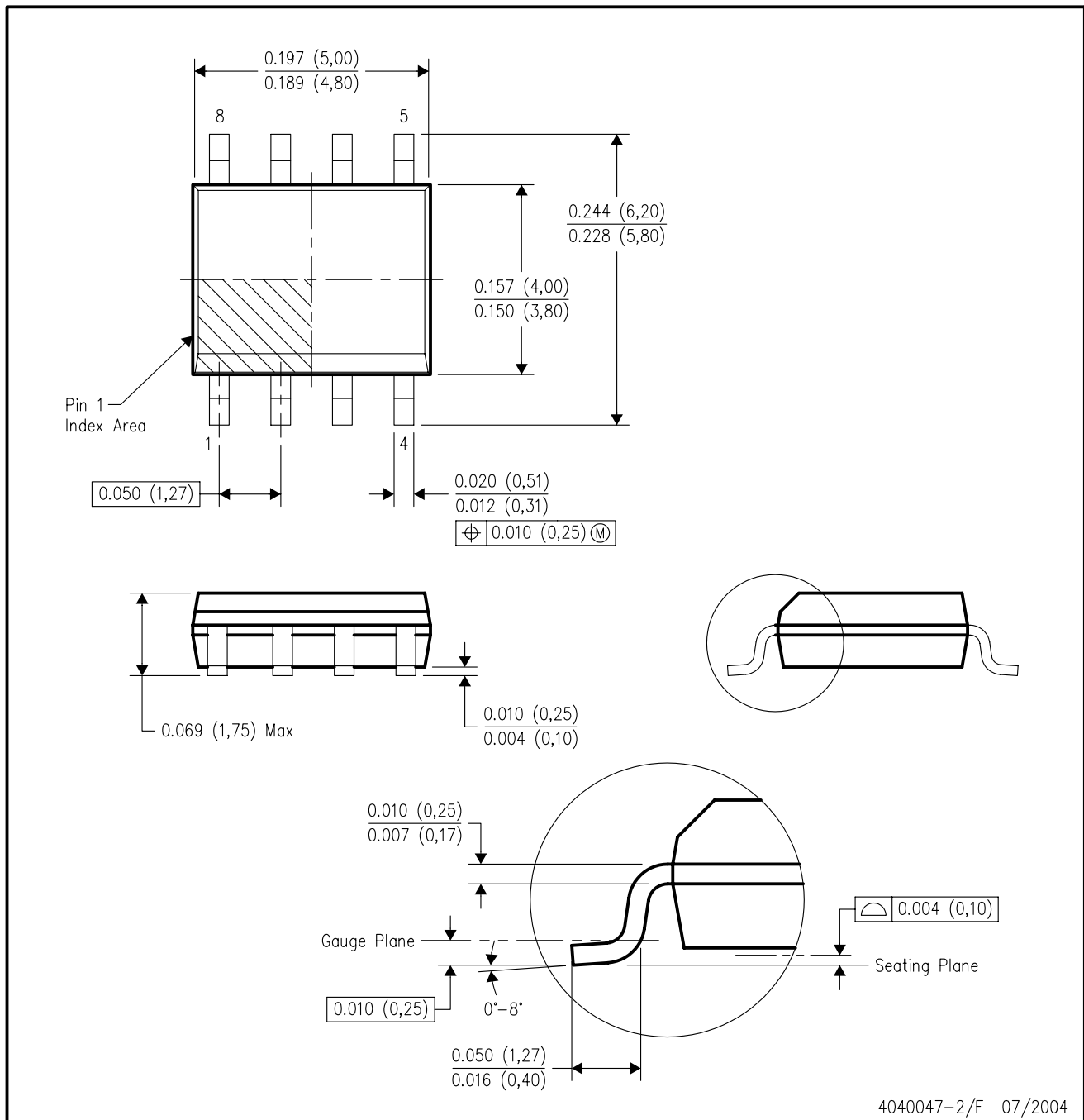
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AA.

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