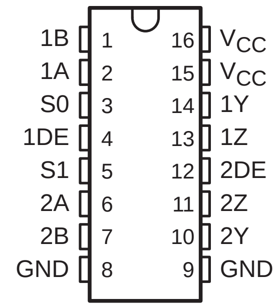
查询SN65LVDM22供应商



- **Meets or Exceeds the Requirements of ANSI TIA/EIA–644–1995 Standard**
- **Designed for Signaling Rates Up to 400 Mbit/s**
- **ESD Protection Exceeds 12 kV on Bus Pins**
- **Operates from a Single 3.3-V Supply**
- **Low-Voltage Differential Signaling with Output Voltages of 350 mVinto:**
  - **100-Ω Load (SN65LVDS22)**
  - **50-Ω Load (SN65LVDM22)**
- **Propagation Delay Time; 4 ns Typ**
- **Power Dissipation at 400 Mbit/s of 150 mW**
- **Bus Pins are High Impedance When Disabled or With $V_{CC}$ Less Than 1.5 V**
- **LVTTL Levels are 5 V Tolerant**
- **Open-Circuit Fail Safe Receiver**

**D PACKAGE**
**(TOP VIEW)**




## description

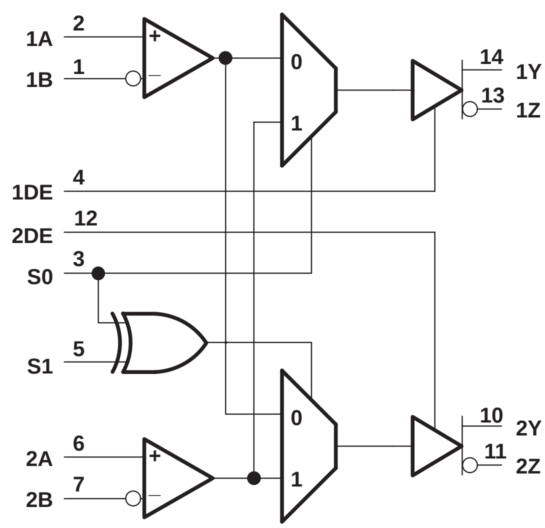
The SN65LVDS22 and SN65LVDM22 are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps. The receiver outputs can be switched to either or both drivers through the multiplexer control signals S0 and S1. This allows the flexibility to perform splitter or signal routing functions with a single device.

The TIA/EIA-644 standard compliant electrical interface provides a minimum differential output voltage magnitude of 247 mV into a 100-Ω load and receipt of 100 mV signals with up to 1 V of ground potential difference between a transmitter and receiver. The SN65LVDM22 doubles the output drive current to achieve LVDS levels with a 50 Ω load.

The intended application of these devices and signaling technique is for both point–to–point baseband (single termination) and multipoint (double termination) data transmissions over controlled impedance media. The transmission media may be printed circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics).

The SN65LVDS22 and SN65LVDM22 are characterized for operation from –40 C to 85 C.

## logic diagram (positive logic)




**MUX Truth Table**

| INPUT | | OUTPUT | | FUNCTION |
|---|---|---|---|---|
| S1 | S0 | 1Y/1Z | 2Y/2Z | |
| 0 | 0 | 1A/1B | 1A/1B | Splitter |
| 0 | 1 | 2A/2B | 2A/2B | Splitter |
| 1 | 0 | 1A/1B | 2A/2B | Router |
| 1 | 1 | 2A/2B | 1A/1B | Router |

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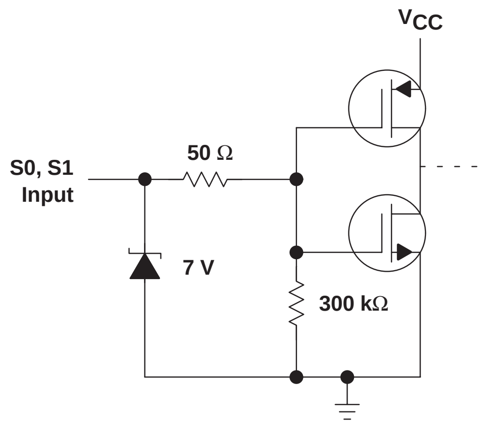
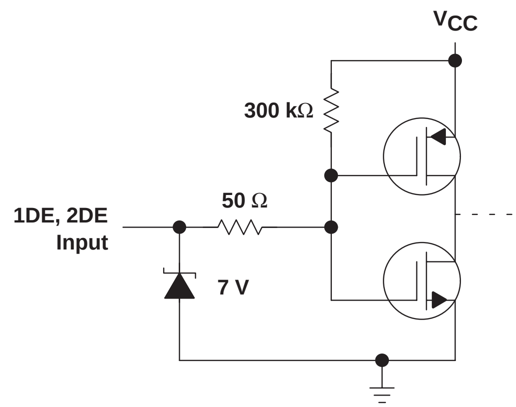
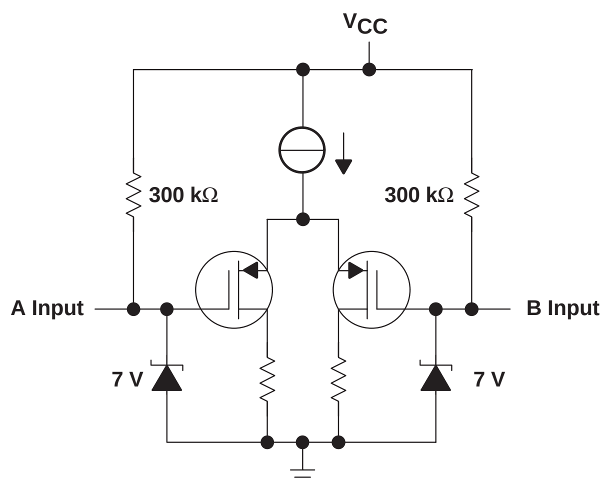
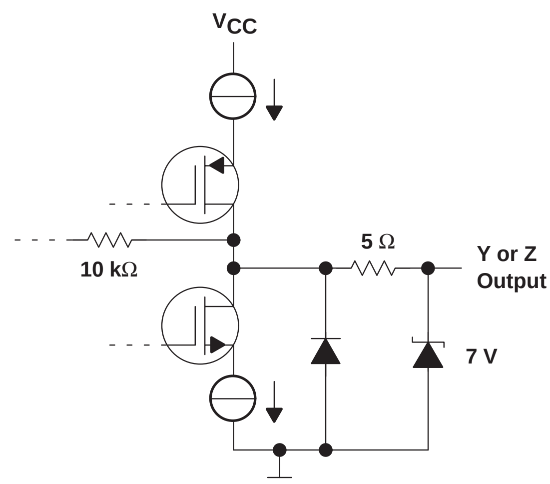
## equivalent input and output schematic diagrams



## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

| | |
|---|---|
| Supply voltage range, $V_{CC}$ (see Note 1) | –0.5 V to 4 V |
| Voltage range (DE, S0, S1) | –0.5 V to 6 V |
| Input voltage range, $V_I$ (A or B) | –0.5 V to Vcc+0.5 V |
| Electrostatic discharge: A, B, Y, Z and GND (see Note 2) | Class 3, A:12 kV, B:600 V |
| All pins | Class 3, A:5 kV, B:500 V |
| Continuous power dissipation | See Dissipation Rating Table |
| Storage temperature range | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR‡ ABOVE $T_A = 25°C$ | $T_A = 85°C$ POWER RATING |
|---|---|---|---|
| D16 | 950 mW | 7.6 mW/°C | 494 mW |

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 3 | 3.3 | 3.6 | V |
| High-level input voltage, $V_{IH}$ | S0, S1, 1DE, 2DE | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | S0, S1, 1DE, 2DE | | | 0.8 | V |
| Magnitude of differential input voltage, $\lvert V_{ID} \rvert$ | | 0.1 | | 0.6 | V |
| Common-mode input voltage, $V_{IC}$ (see Figure 1) | | $\frac{\lvert V_{ID} \rvert}{2}$ | | $2.4 - \frac{\lvert V_{ID} \rvert}{2}$ | V |
| | | | | $V_{CC}$–0.8 | V |
| Operating free-air temperature, $T_A$ | | –40 | | 85 | °C |

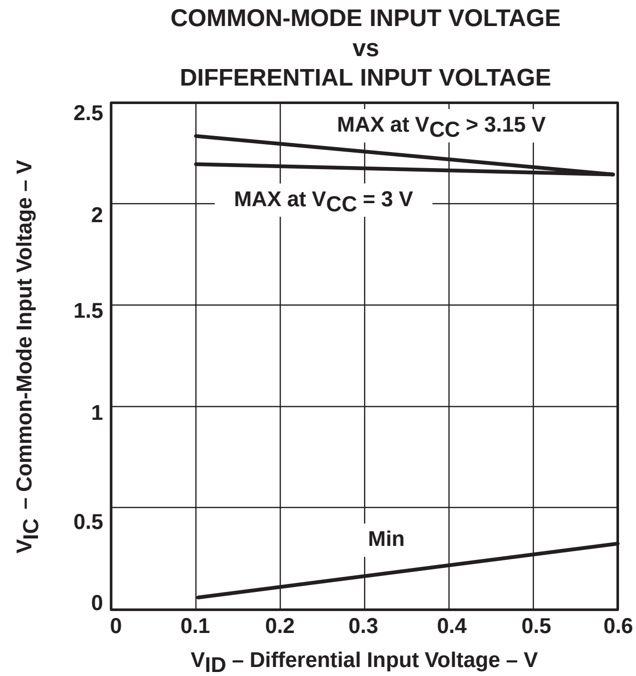



**Figure 1. Common-Mode Input Voltage vs Differential Input Voltage**

## receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{ITH+}$ | Positive-going differential input voltage threshold | | | | 100 | mV |
| $V_{ITH–}$ | Negative-going differential input voltage threshold | | –100 | | | mV |
| $I_I$ | Input current (A or B inputs) | $V_I$ = 0 V | –2 | | –20 | μA |
| | | $V_I$ = 2.4 V | –1.2 | | | |
| $I_{I(OFF)}$ | Power-off input current (A or B inputs) | $V_{CC}$ = 0 V | | | 20 | μA |

## receiver/driver electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OD}$ | Differential output voltage magnitude | | $R_L$ = 100 Ω ('LVDS22), $R_L$ = 50 Ω('LVDM22) | See Figure 2 | 247 | 340 | 454 | mV |
| $\Delta V_{OD}$ | Change in differential output voltage magnitude between logic states | | | | –50 | | 50 | mV |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | | | See Figure 3 | 1.125 | | 1.375 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage between logic states | | | | –50 | 3 | 50 | mV |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | | | | | | 150 | mV |
| $I_{CC}$ | Supply current | | No Load | | | 8 | 12 | mA |
| | | | $R_L$ = 100 Ω ('LVDS22) | | | 13 | 20 | |
| | | | $R_L$ = 50 Ω ('LVDM22) | | | 21 | 27 | |
| | | | Disabled | | | 3 | 6 | |
| $I_{IH}$ | High-level input current | DE | $V_{IH}$ = 5 | | | | –10 | µA |
| | | S0, S1 | | | | | 20 | |
| $I_{IL}$ | Low-level input current | DE | $V_{IL}$ = 0.8 V | | | | –10 | µA |
| | | S0, S1 | | | | | 10 | |
| $I_{OS}$ | Short-circuit output current | | $V_{OY}$ or $V_{OZ}$ = 0 V, $V_{OD}$ = 0 V, | ('LVDS22) | | | –10 | mA |
| | | | | | | | –10 | |
| | | | $V_{OY}$ or $V_{OZ}$ = 0 V, $V_{OD}$ = 0 V, | ('LVDM22) | | | –10 | |
| | | | | | | | –10 | |
| $I_{OZ}$ | High-impedance output current | | $V_{OD}$ = 600 mV | | | 0.015 | ±1 | µA |
| | | | $V_O$ = 0 V or $V_{CC}$ | | | 0.015 | ±1 | |
| $I_{O(OFF)}$ | Power-off output current | | $V_{CC}$ = 0 V, | $V_O$ = 3.6 V | | 0.015 | ±1 | µA |
| $C_{IN}$ | Input capacitance | | | | | 3 | | pF |

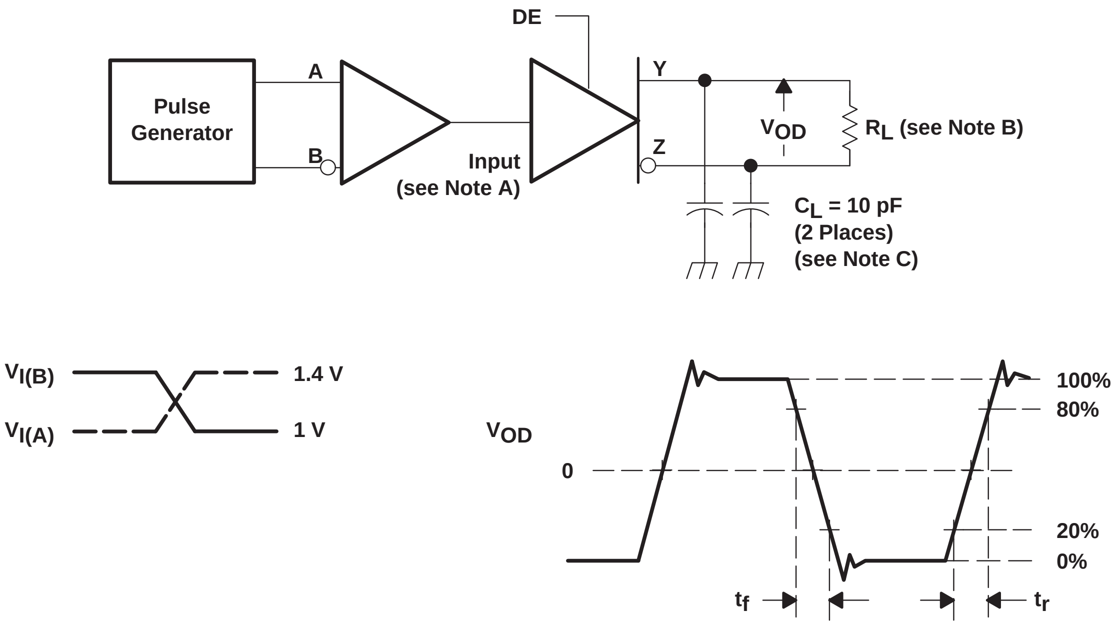
† All typical values are at 25°C and with a 3.3 V supply.

## differential receiver to driver switching characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Differential propagation delay, low-to-high | | $C_L$ = 10 pF, See Figure 4 | | 4 | 6 | ns |
| $t_{PHL}$ | Differential propagation delay, high-to-low | | | | 4 | 6 | ns |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{PHL} – t_{PLH} \rvert$) | | | | 0.5 | | ns |
| $t_r$ | Transition, low-to-high | SN65LVDS22 | | | 1 | 1.5 | ns |
| $t_r$ | Transition, low-to-high | SN65LVDM22 | | | 0.8 | 1.3 | ns |
| $t_f$ | Transition, high-to-low | SN65LVDS22 | | | 1 | 1.5 | ns |
| $t_f$ | Transition, high-to-low | SN65LVDM22 | | | 0.8 | 1.3 | ns |
| $t_{PHZ}$ | Propagation delay time, high-level-to-high-impedance output | | See Figure 5 | | 4 | 10 | ns |
| $t_{PLZ}$ | Propagation delay time, low-level-to-high-impedance output | | | | 5 | 10 | ns |
| $t_{PZH}$ | Propagation delay time, high-impedance-to-high-level output | | | | 5 | 10 | ns |
| $t_{PZL}$ | Propagation delay time, high-impedance-to-low-level output | | | | 6 | 10 | ns |
| $t_{PHL\_R1\_Dx}$ | Channel-to-channel skew, receiver to driver‡ | | | | 0.2 | | ns |
| $t_{PLH\_R1\_Dx}$ | | | | | 0.2 | | |
| $t_{PHL\_R2\_Dx}$ | | | | | 0.2 | | |
| $t_{PLH\_R2\_Dx}$ | | | | | 0.2 | | |

† All typical values are at 25°C and with a 3.3 V supply.
‡ These parametric values are measured over supply voltage and temperature ranges recommended for the device.

## PARAMETER MEASUREMENT INFORMATION

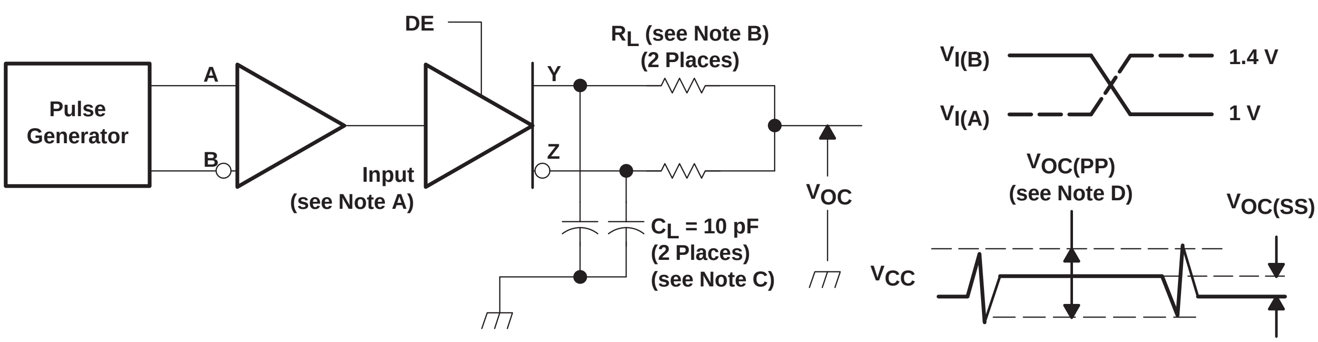



NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.

NOTES: B. $R_L$ = 100 Ω or 50 Ω ±1%

C. CL includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

**Figure 2. Test Circuit and Voltage Definitions for the Differential Output Signal**




NOTES: A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.

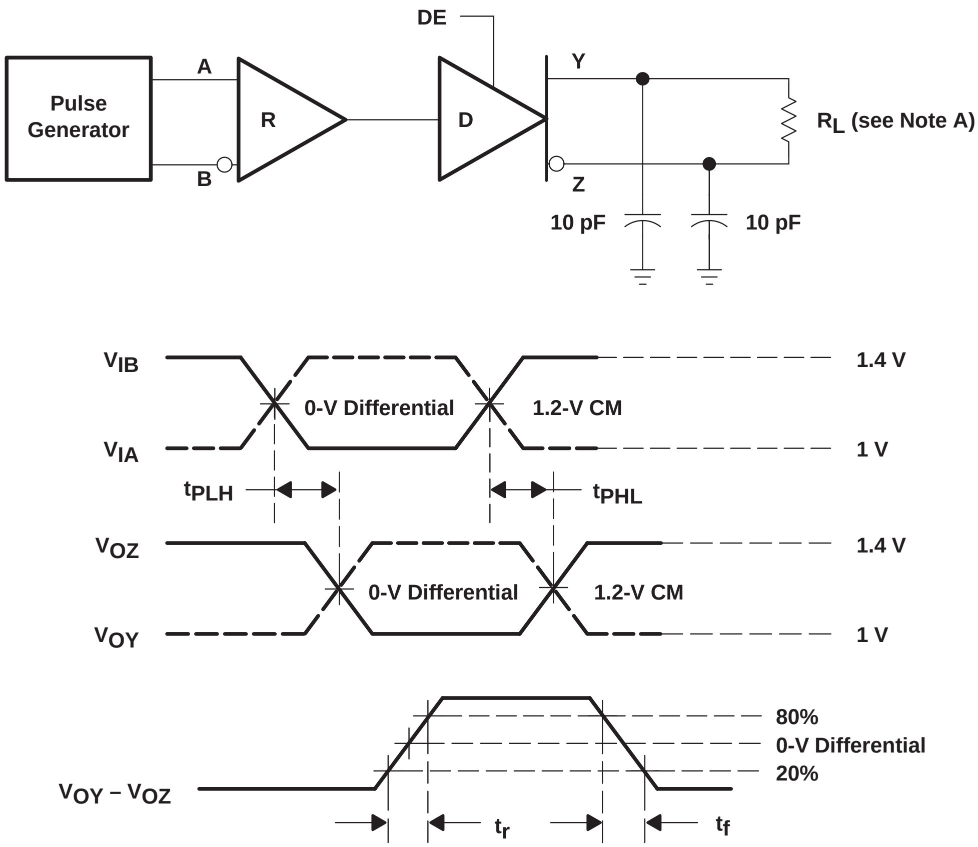
NOTES: B. $R_L$ = 100 Ω or 50 Ω ±1%

C. $C_L$ includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

D. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

**Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage**

## PARAMETER MEASUREMENT INFORMATION

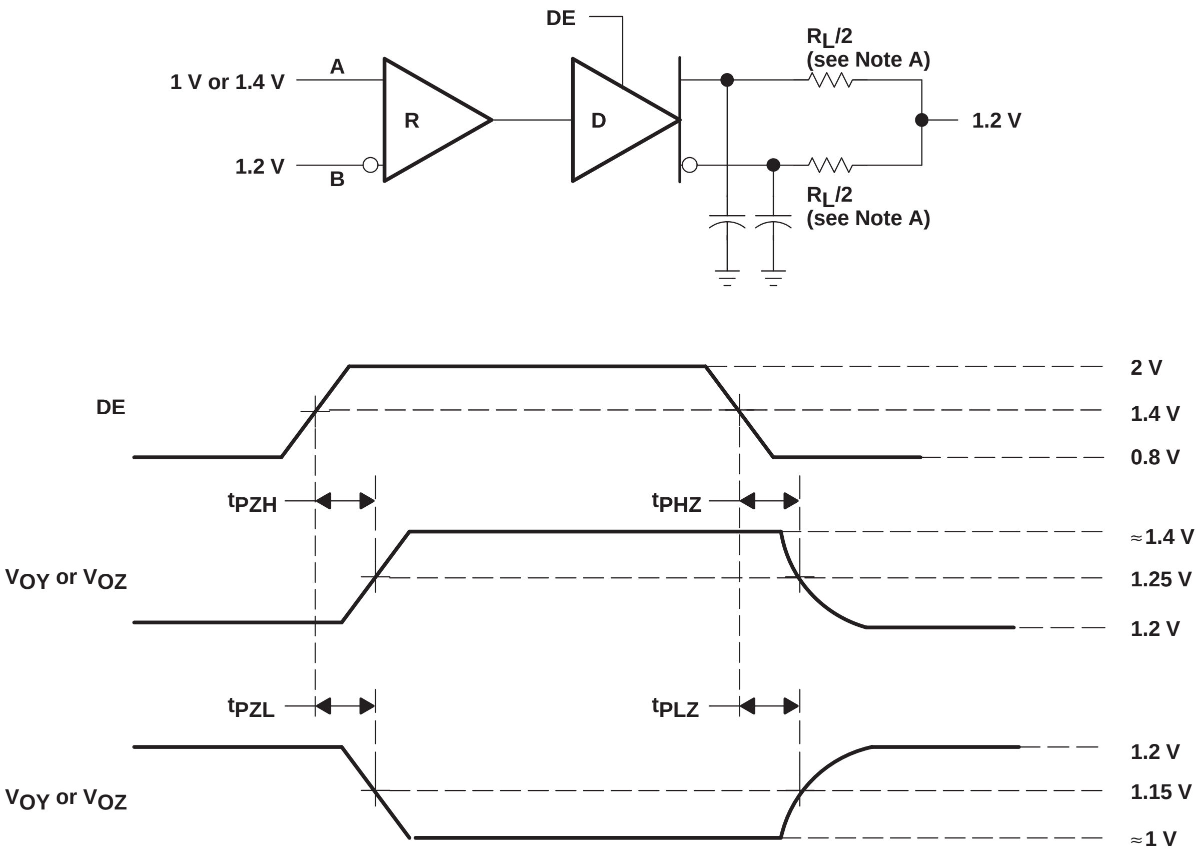



NOTES: A. $R_L$ = 100 Ω or 50 Ω ±1%

B. All input pulses are supplied by a generator having the following characteristics: pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.

**Figure 4. Differential Receiver to Driver Propagation Delay and Driver Transition Time Waveforms**

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $R_L$ = 100 Ω or 50 Ω ±1%

B. All input pulses are supplied by a generator having the following characteristics: pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.

**Figure 5. Enable and Disable Timing Circuit**

## TYPICAL CHARACTERISTICS

**SN65LVDS22**
**HIGH-LEVEL OUTPUT VOLTAGE**
**vs**
**HIGH-LEVEL OUTPUT CURRENT**

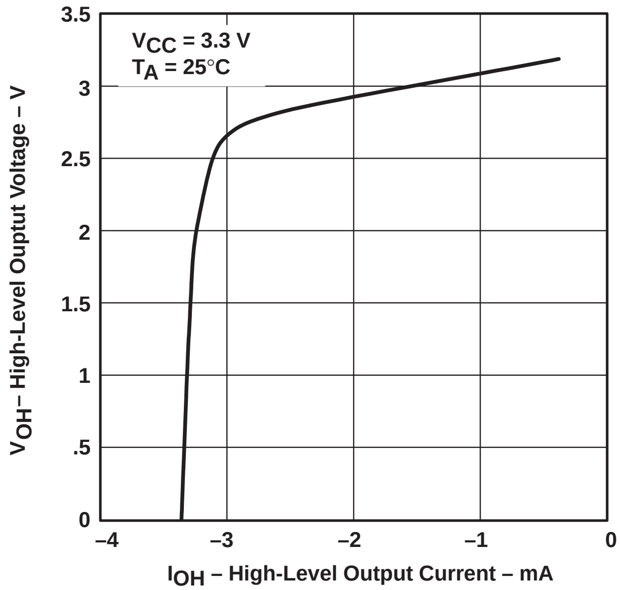



**Figure 6**

**SN65LVDS22**
**LOW-LEVEL OUTPUT VOLTAGE**
**vs**
**LOW-LEVEL OUTPUT CURRENT**

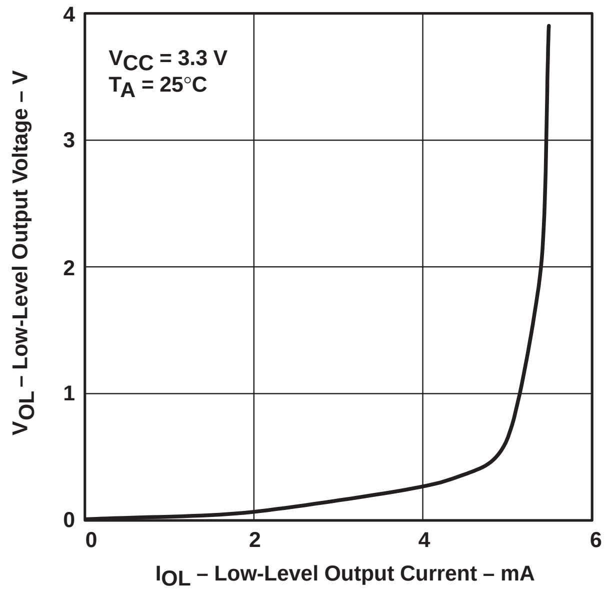



**Figure 7**

**SN65LVDM22**
**HIGH-LEVEL OUTPUT VOLTAGE**
**vs**
**HIGH-LEVEL OUTPUT CURRENT**

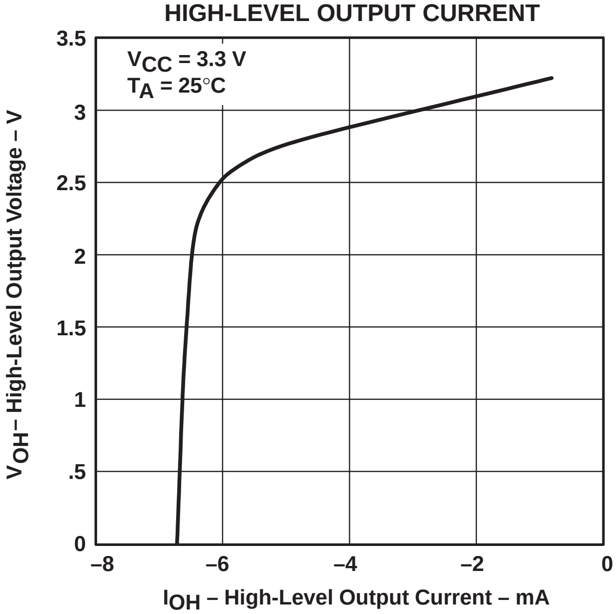



**Figure 8**

**SN65LVDM22**
**LOW-LEVEL OUTPUT VOLTAGE**
**vs**
**LOW-LEVEL OUTPUT CURRENT**

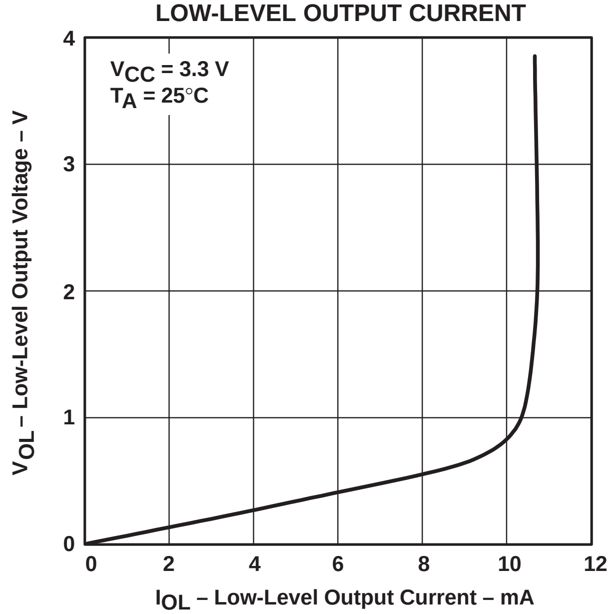



**Figure 9**

## APPLICATION INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission. Ground differences are less than 1 V with a low common–mode output and balanced interface for very low noise emissions. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/Receivers maintain ECL speeds without the power and dual supply requirements.

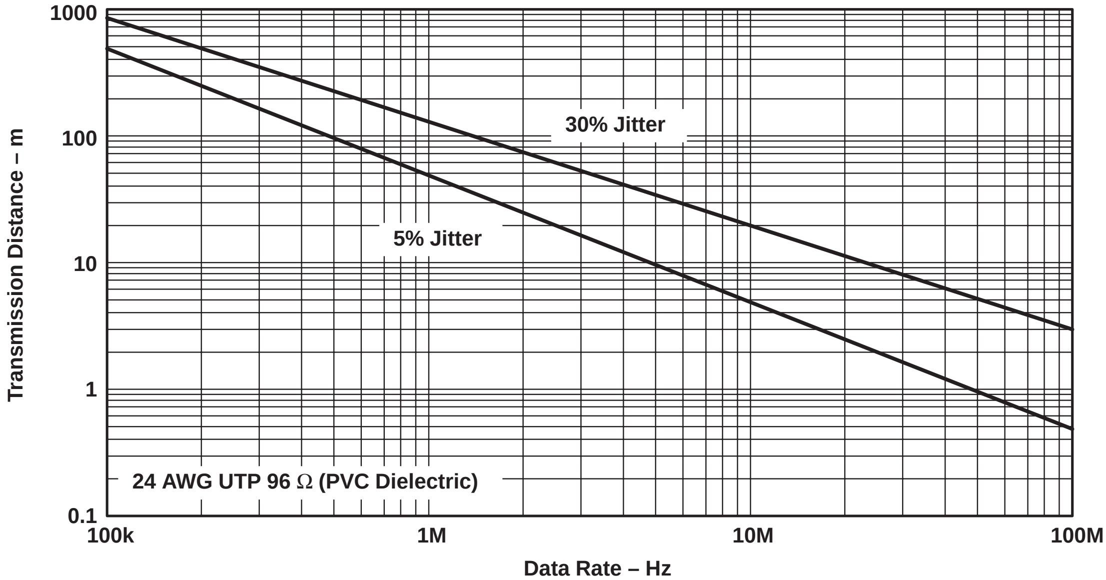



**Figure 10. Data Transmission Distance Versus Rate**

## APPLICATION INFORMATION

### fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near $V_{CC}$ through 300-kΩ resistors as shown in Figure 11. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

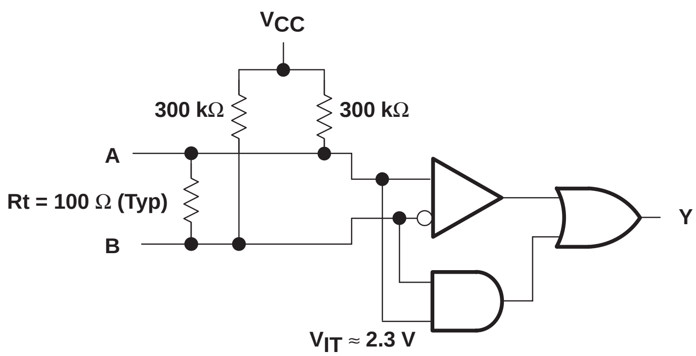


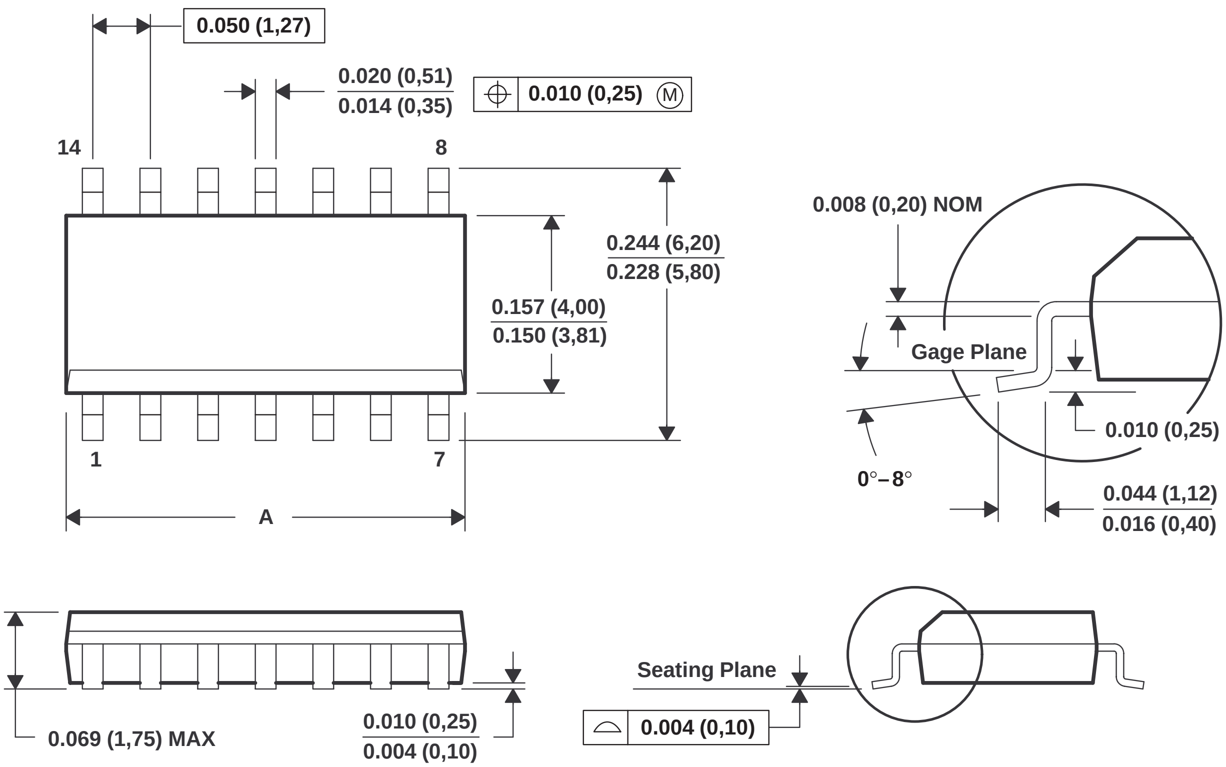

**Figure 11. Open-Circuit Fail Safe of the LVDS Receiver**

It is only under these conditions that the output of the receiver will be valid with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pull-up currents from the receiver and the fail-safe feature.

## MECHANICAL DATA

**D (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PIN SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 |
|---|---|---|---|
| A MAX | 0.197 (5,00) | 0.344 (8,75) | 0.394 (10,00) |
| A MIN | 0.189 (4,80) | 0.337 (8,55) | 0.386 (9,80) |

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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