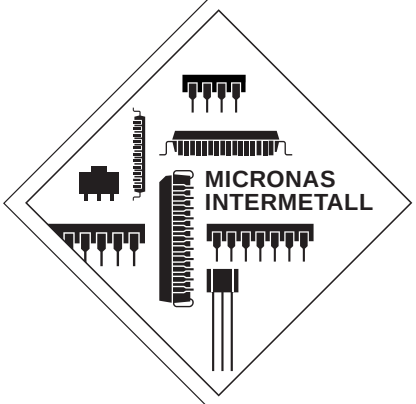


ADVANCE INFORMATION

VDP 3108
Single-Chip
Video Processor

Edition Oct. 12, 1994
6251-352-3AI

MICRONAS
INTERMETALL

Contents

Single-Chip Video Processor

1. Introduction

The entire video processing and controlling for a color TV has been developed on a single chip in 0.8µ CMOS technology. Modular design and submicron technology allow the economic integration of features in all classes of TV sets.

Open architecture is the key word to the new DSP generation. Flexible standard building blocks have been defined that offer continuity and transparency of the entire system.

One IC contains the entire video and deflection processing and builds the heart of a modern color TV. Its performance and complexity allow the user to standardize his product development. Hardware and software applications can profit from the modularity as well as manufacturing, system support or maintenance. The main features are:

– low cost, high performance

– all digital video processing

– multi-standard color decoder PAL/NTSC/SECAM

– 3 composite, 1 S–VHS input

– integrated high-quality AD/DA converters

– sync and deflection processing

– luminance and chrominance features, e.g. peaking, color transient improvement

– programmable RGB matrix

– various digital interfaces

– embedded RISC controller (80 MIPS)

– one crystal, few external components

– single power supply 5 V

– 0.8µ CMOS Technology

– 68-pin PLCC or 64-pin Shrink DIL Package

1.1. System Architecture

Two main modules have been defined:

Video Processor and

Display Processor.

They are designed as silicon building blocks. Their partitioning permits a variety of IC configurations with the aim to satisfy the particular requirements of different applications. Both, analog and digital interfaces, support state of the art TV receivers as well as other environments. Fig. 1–1 shows the block diagram of the single-chip Video Processor which consists of both modules.

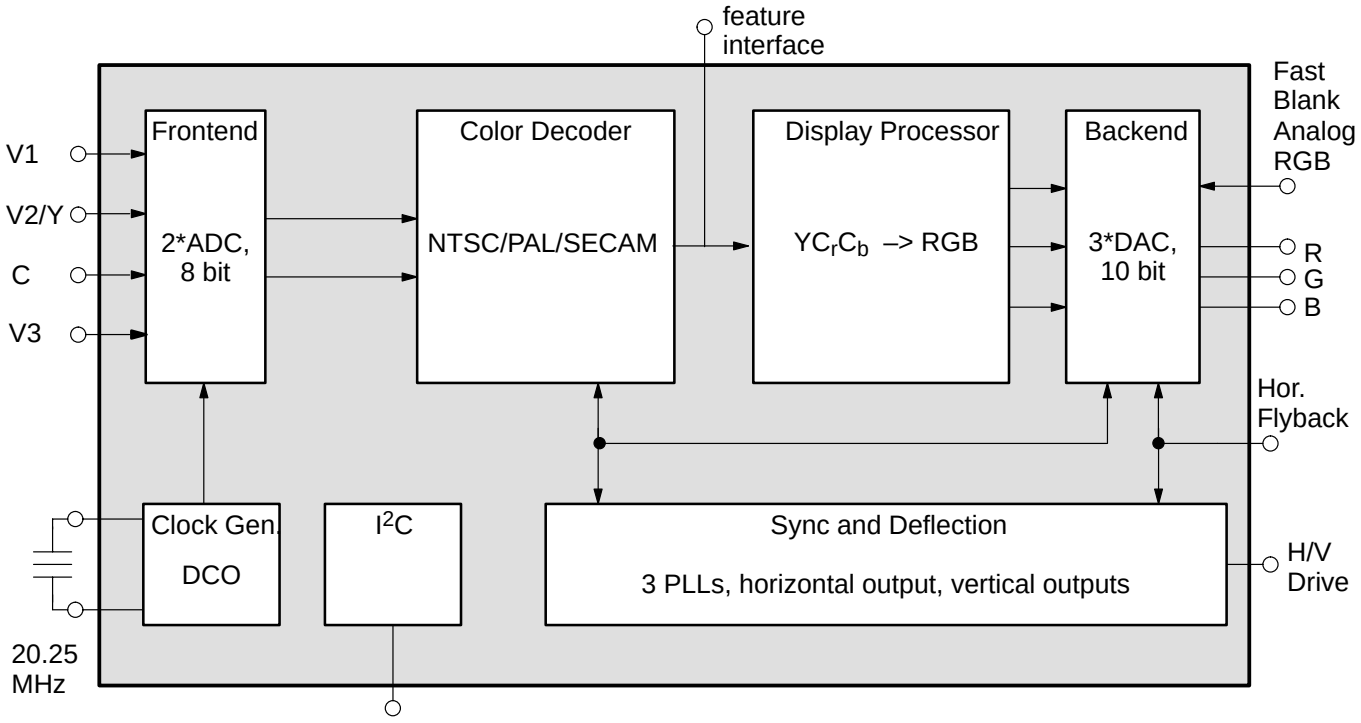


Fig. 1–1: VDP block diagram

2. Functional Description

2.1. Analog Front End

This block provides the analog interfaces to all video inputs and mainly carries out analog-to digital conversion for the following digital video processing. A block diagram is given in figure 2–1.

Most of the functional blocks in the front end are digitally controlled (clamping, AGC and clock-DCO). The control loops are closed by the Fast Processor ('FP') embedded in the decoder.

2.1.1. Input Selector

Up to four analog inputs can be connected. Three inputs are for input of composite video or S–VHS luma signal. These inputs are clamped to the sync back porch and are amplified by a variable gain amplifier. One input is for connection of S–VHS carrier–chrominance signal. This input is internally biased and has a fixed gain amplifier.

2.1.2. Clamping

The composite video input signals are AC coupled to the IC. The clamping voltage is stored on the coupling capacitors and is generated by digitally controlled current sources. The clamping level is the back porch of the video signal. S-VHS chroma is also AC coupled. The input pin is internally biased to the center of the ADC input range.

2.1.3. Automatic Gain Control

A digitally working automatic gain control adjusts the magnitude of the selected baseband by +6/–4.5 dB in 64 logarithmic steps to the optimal range of the ADC .

The gain of the video input stage including the ADC is 213 steps/V for all three standards (PAL/NTSC/SECAM/Y/C), with the AGC set to 0 dB.

2.1.4. Analog-to-Digital Converters

Two ADCs are provided to digitize the input signals. Each converter runs with 20.25 MHz and has 8 bit resolution. An integrated bandgap circuit generates the required reference voltages for the converters.

The two ADCs are of a 2-stage subranging type.

2.1.5. ADC Range

The ADC input range for the various input signals and the digital representation is given in table 2–1 and figure 2–2.

2.1.6. Digitally Controlled Clock Oscillator

The clock generation is also a part of the analog front end. The crystal oscillator is controlled digitally by the control processor; the clock frequency can be adjusted within ±150 ppm.

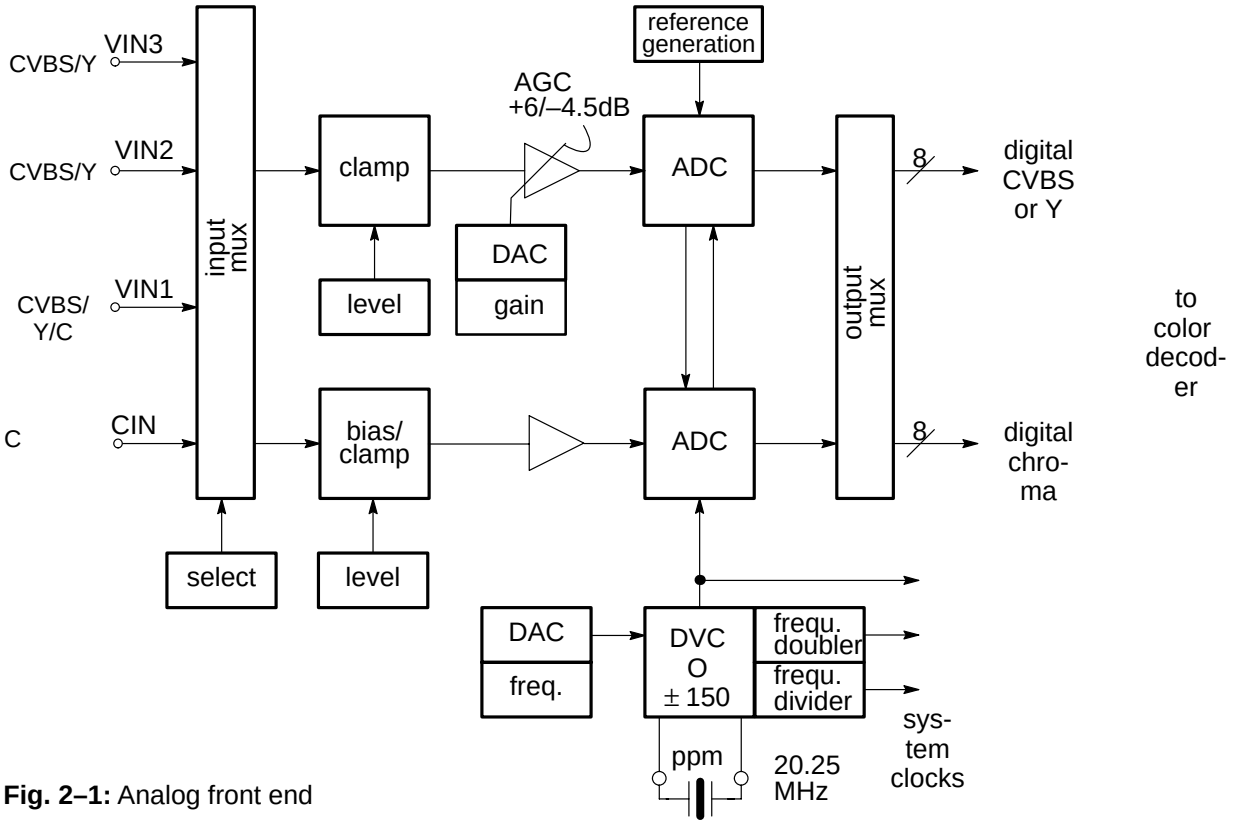


Fig. 2–1: Analog front end

Table 2–1: ADC input range for PAL input Signal

Signal		ADC Range [steps]	Input Level [mV_{pp}]		
			–6 dB	0 dB	+4.5 dB
CVBS	100% CVBS	252 (clipped at 125 IRE)	667	1333	2238
	75% CVBS	213	500	1000	1679
	video (luma)	149	350	700	1175
	sync	64 (AGC reference)	150	300	504
	clamp level	68			
Chroma	burst	64		300	
	100% Chroma	190		890	
	75% Chroma	143		670	
	bias level	128			

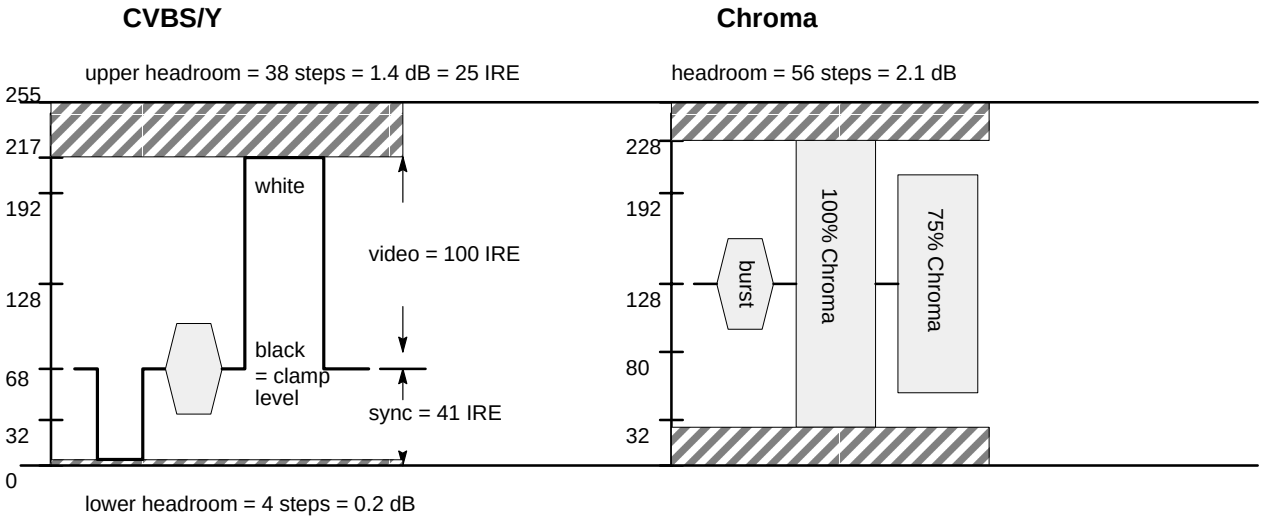


Fig. 2–2: ADC ranges for CVBS/Luma and Chroma, PAL input signal

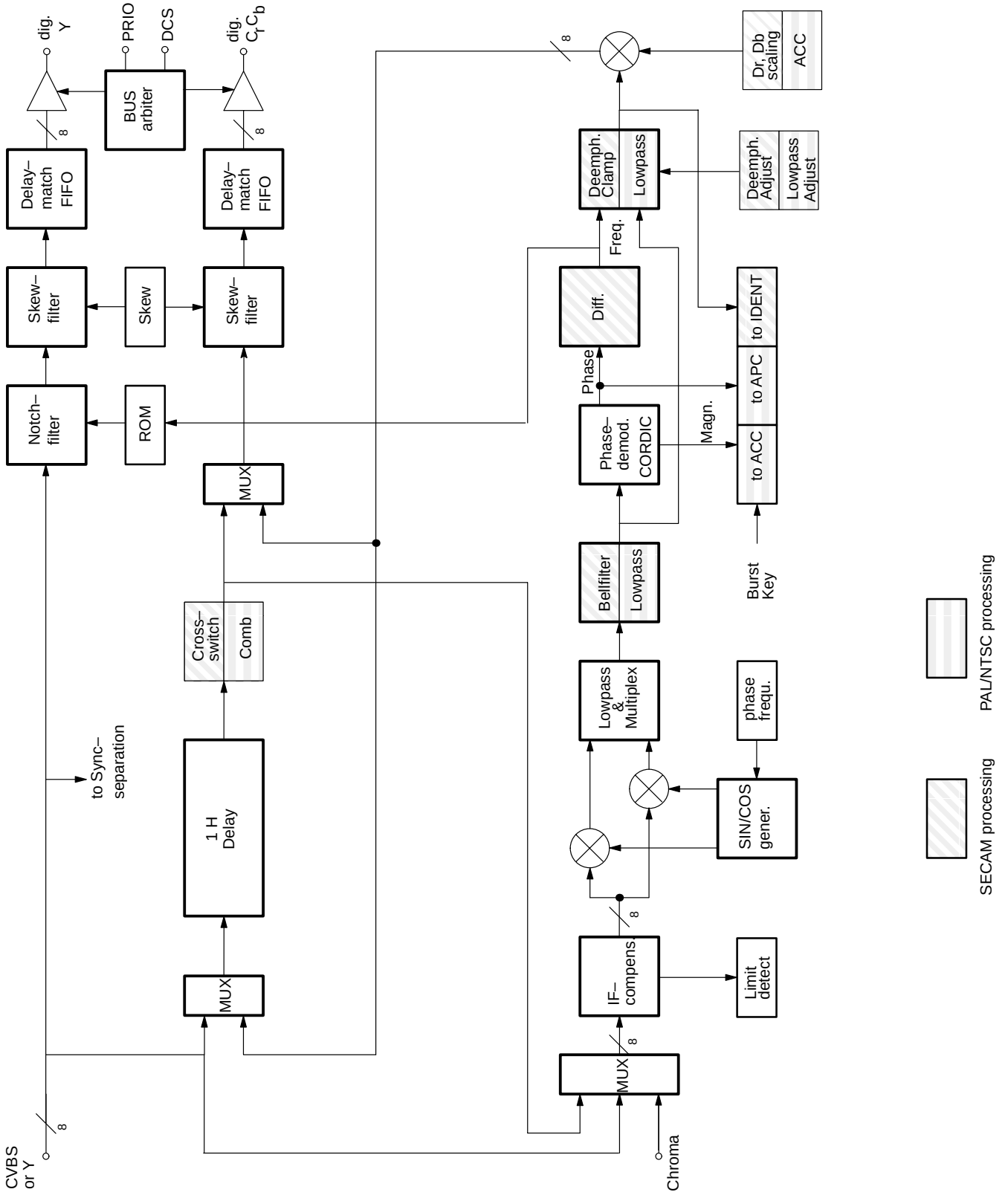


Fig. 2–3: Color decoder

2.2. Color Decoder

In this block the entire luma/chroma separation and multi standard color demodulation is carried out. The color demodulation uses an asynchronous clock, thus allowing a unified architecture for all color standards.

Both luma and chroma are processed to an orthogonal sampling raster. Luma and Chroma delays are matched. The total delay of the decoder is adjustable by a FIFO memory. Thus, including the delay of the display processing, exactly 64 µsec processing delay can be obtained.

The output of color decoder is YC_rC_b in a 4:2:2 format.

2.2.1. IF-Compensation

With off-air or mistuned reception any attenuation at higher frequencies or asymmetry around the color subcarrier is compensated. Three different settings of the IF-compensation are possible:

flat (no compensation)
6 dB /octave
12 dB /octave

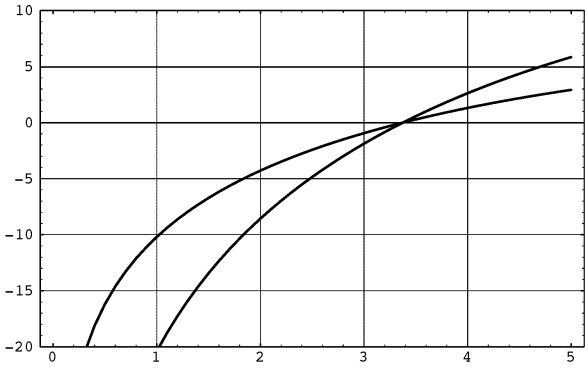


Fig. 2–4: Frequency response of chroma IF-compensation

2.2.2. Demodulator

The entire signal (which might still contain luma) is now quadrature-mixed to the baseband. The mixing frequency is equal to the subcarrier for PAL and NTSC, thus achieving the chroma demodulation. For SECAM, the mixing frequency is 4.286 MHz giving the quadrature baseband components of the FM modulated chroma. After the mixer, a lowpass filter selects the chroma components; a downsampling stage converts the color difference signals to a multiplexed half rate data stream.

The subcarrier frequency in the demodulator is generated by direct digital synthesis; therefore substandards such as PAL 3.58 or NTSC 4.43 can also be demodulated.

2.2.3. Chrominance Filter

The demodulation is followed by a lowpass filter for the color difference signals for PAL/NTSC. SECAM requires a modified lowpass function with bell-filter characteristic. At the output of the lowpass filter all luma information is eliminated.

The lowpass filters are calculated in time multiplex for the two color signals. Three bandwidth settings (narrow, normal, broad) are available for each standard. The filter passband can be shaped with an extra peaking term at 1.25 MHz.

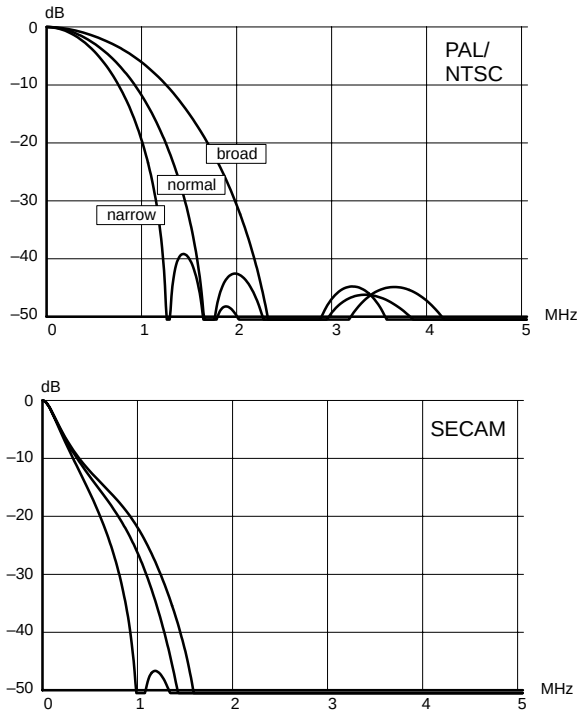


Fig. 2–5: Frequency response of chroma filters

2.2.4. Frequency Demodulator

The frequency demodulator for demodulating the SECAM signal is implemented as a CORDIC-structure. It calculates the phase and magnitude of the quadrature components by coordinate rotation.

The phase output of the CORDIC processor is differentiated to obtain the demodulated frequency. After a programmable deemphasis filter the Dr and Db signals are scaled to standard C_rC_b amplitudes and fed to the cross-over-switch.

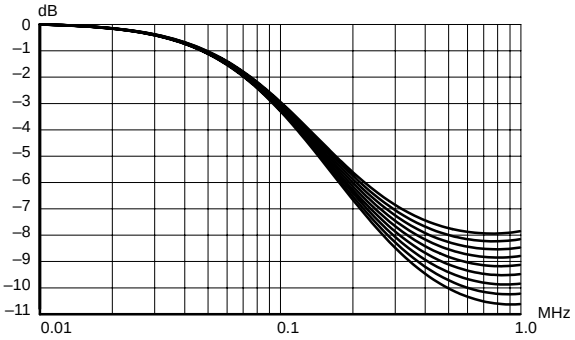


Fig. 2–6: Frequency response of SECAM deemphasis

2.2.5. Burst Detection

In the PAL/NTSC-system the burst is the reference for the color signal. The phase and magnitude outputs of the CORDIC are gated with the color key and used for controlling the phase-lock-loop (APC) of the demodulator and the automatic color control (ACC) in PAL/NTSC.

The ACC has a control range of +30 ... –6 dB.

For SECAM decoding, the frequency of the burst is measured. Thus, the current chroma carrier frequency can be identified and is used to control the SECAM processing. The burst measurements also control the color killer operation; they can be used for automatic standard detection as well.

2.2.6. Color Killer Operation

The color killer uses the burst–phase, –frequency measurement to identify a PAL/NTSC or SECAM color signal. For PAL/NTSC the color is switched off (killed) as long as the color subcarrier PLL is not locked. For SECAM the killer is controlled by the toggle of the burst frequency. The burst amplitude measurement is used to switch–off the color if the burst amplitude is below a programmable threshold. Thus color will be killed for very noisy signals. The color amplitude killer has a programmable hysteresis.

2.2.7. Delay Line / Comb Filter

The color decoder uses one fully integrated delay line. Only active video is stored.

The delay line application depends on the color standard:

NTSC:	combfilter **or** color compensation
PAL:	color compensation
SECAM:	crossover-switch

In the NTSC compensated mode, Fig. 2–7 c), the color signal is averaged for two adjacent lines. Thus cross–color distortion and chroma noise is reduced. In the NTSC combfilter mode, Fig. 2–7 d), the delay line is in the composite signal path, thus allowing reduction of cross-color components as well as cross-luminance. The loss of vertical resolution in the luminance channel is compensated by adding the vertical detail signal with removed color information.

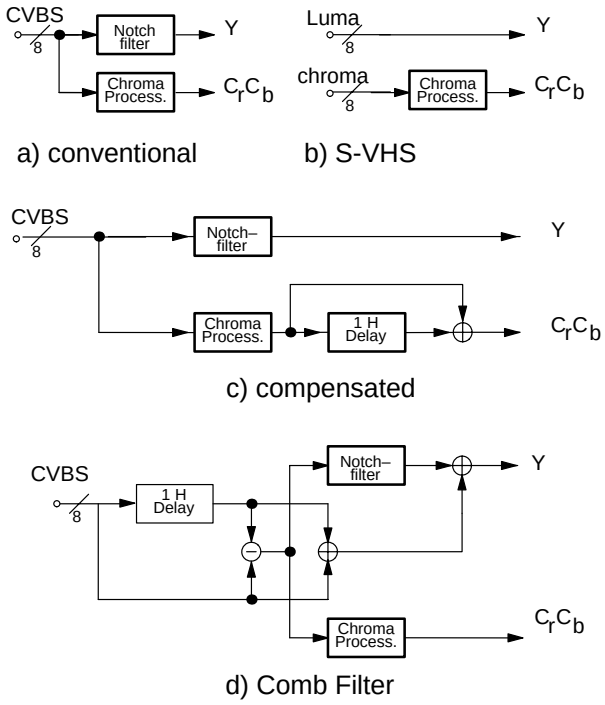


Fig. 2–7: NTSC color decoding options

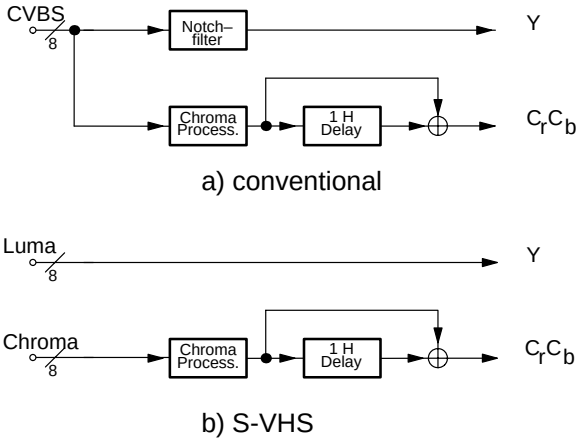


Fig. 2–8: PAL color decoding options

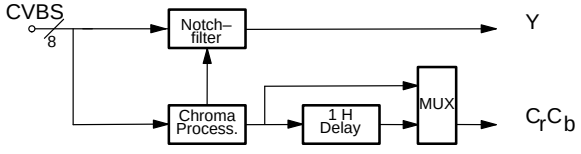
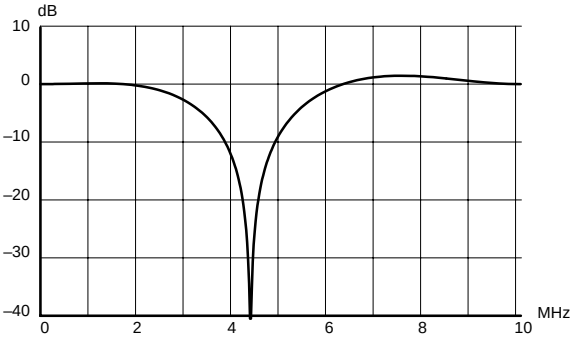
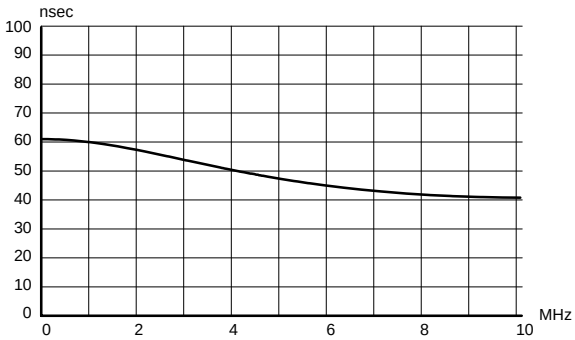


Fig. 2–9: SECAM color decoding

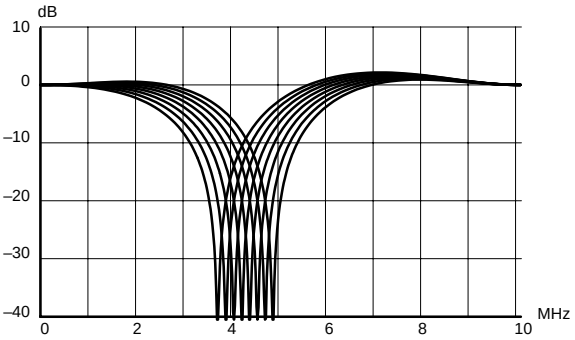
2.2.8. Luminance Notch Filter

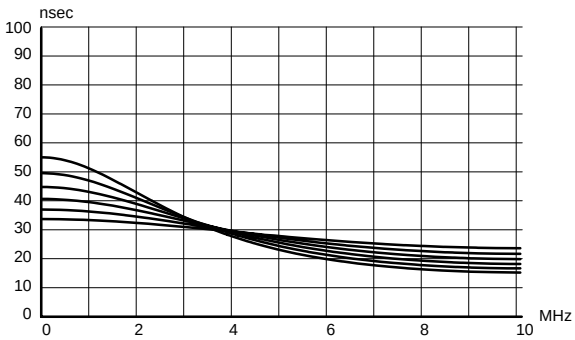
If a composite video signal is applied, the color information is suppressed by a programmable notch filter. The position of the filter center frequency depends on the subcarrier frequency for PAL/NTSC. For SECAM, the notch is directly controlled by the chroma carrier frequency. This considerably reduces the cross-luminance. The frequency responses and the delay characteristics of all three systems are shown below.



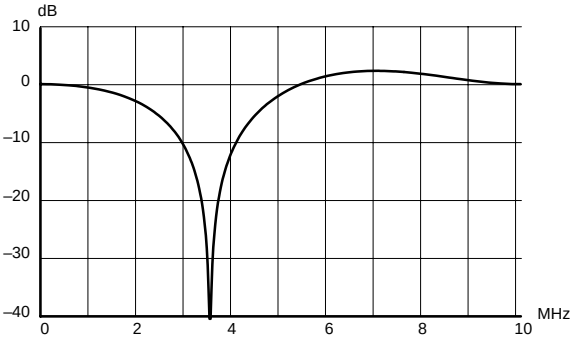


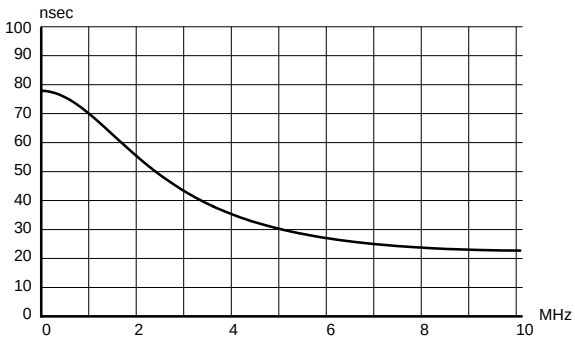
PAL notch filter





SECAM notch filter





NTSC notch filter

Fig. 2–10: Frequency Responses and Time Delay Characteristics for PAL, SECAM, NTSC

2.2.9. Skew Filter

The system clock is free running and not locked to the TV line frequency. Therefore, the ADC sampling pattern is not orthogonal. The decoded YC_rC_b signals are converted to an orthogonal sampling raster by skew filter block at the output of the color decoder.
The skew filters are controlled by a skew parameter and allow to apply a group delay to the input signals without introducing waveform of frequency response distortion.

The amount of phase shift of this filter is controlled by the horizontal PLL1. The accuracy of the filters is 1/32 clocks for luminance and 1/4 clocks for chroma. Thus the output of the color decoder is in an orthogonal pixel format even in the case of nonstandard input signals such as VCR.

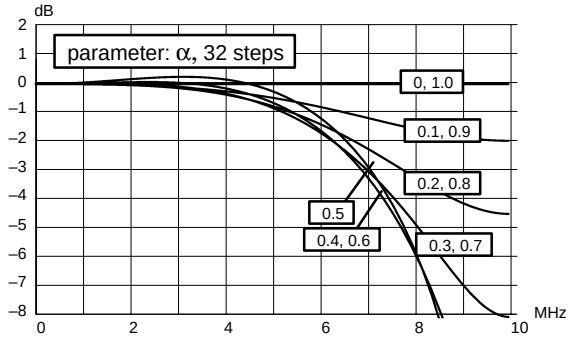


Fig. 2–11: Luminance, Chrominance skew filter magnitude frequency response

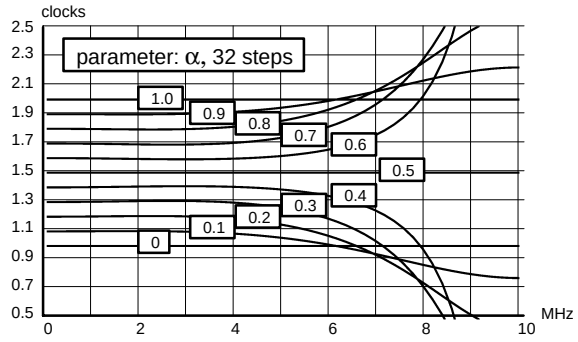


Fig. 2–12: Luminance, chrominance skew filter group delay characteristics

2.2.10. Picture Bus Color Space

Output of the color decoder block is YC_rC_b with 20.25 Msamples/s. Only active video is transferred. The number of active samples is 1068 per line for all standards (525 lines and 625 lines).

The following equations explain the data formats. The R,G,B source signals are already gamma-weighted. The transform matrix from R,G,B to color difference signals is given by:

$$\begin{pmatrix} Y \\ R-Y \\ B-Y \end{pmatrix} = \begin{pmatrix} 0.299 & 0.587 & 0.114 \\ 0.701 & -0.587 & -0.114 \\ -0.299 & -0.587 & 0.886 \end{pmatrix} \begin{pmatrix} R \\ G \\ B \end{pmatrix}$$

In each TV broadcast standard different weighting factors for (R–Y) and (B–Y) are used:

PAL: $V = 0.877*(R-Y)$, $U = 0.493*(B-Y)$

NTSC: $I = V*\cos 33^\circ - U*\sin 33^\circ$, $Q = V*\sin 33^\circ + U*\cos 33^\circ$

SECAM: $Dr = -1.9*(R-Y)$, $Db = 1.5*(B-Y)$

MAC: $Vm = 0.927*(R-Y)$, $Um = 0.733*(B-Y)$

Studio (CCIR 601): $C_r = 0.713*(R-Y)$, $C_b = 0.564*(B-Y)$

In the color decoder the weighting for both color difference signals is adjusted individually. The default format will have the following specification:

$Y = 224*Y + 16$ (pure binary),
$C_r = 224*(0.713*(R-Y)) + 128$ (offset binary),
$C_b = 224*(0.564*(B-Y)) + 128$ (offset binary).

Optionally the picture bus format of the chrominance components C_r, C_b can be switched to two's complement format.

The YC_rC_b FIFO memories allow an adjustable delay for the video processing e.g. one TV line. The memories are controlled by the horizontal sync information available in the front end and the display processor. Using the front end sync, a window for the active video is generated. Only active video data are written to the FIFO memories. The display processor generates the main sync signal from the display timing and data is read from the FIFOs using the main sync signal. This allows an adjustable delay as well as a variable delay, e.g. for VCR timebase correction.

2.3. Digital Video Interfaces

The digital video interface allows insertion of digital data in YC_rC_b format on the internal YC_rC_b data bus. The orthogonal data structure of this bus is the ideal interface point to external data sources and sinks. On top of this, a host of formats are supported, e.g. support of level-2 teletext or the priority pixel bus concept.

Figure 2–13 shows all available digital interfaces:

YC_rC_b 16 bit 4:2:2
RBG 5 bit 4:4:4
PRIO 3 bit, source selection

The YCrCb bus is used for video insertion. The RGB interface is used for insertion of a Teletext or OSD picture. The priority bus allows to mix up to 8 sources on the YC_rC_b / RGB bus.

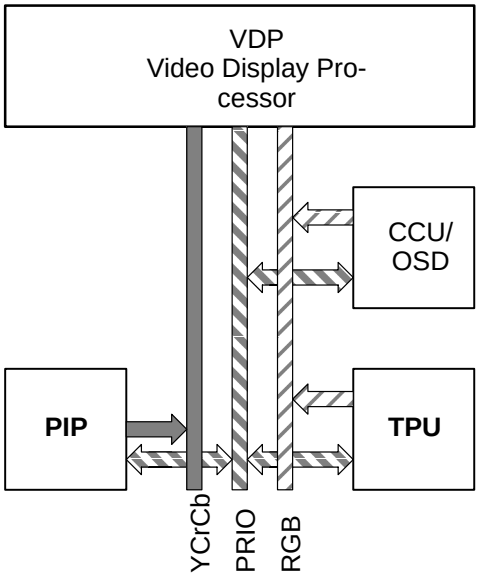


Fig. 2–13: VDP video interfaces

2.3.1. Picture Bus Interface

The picture bus format between all DIGIT3000 ICs is YCrCb with 20.25 Msamples/s. Only active video is transferred, synchronized by the system main sync signal (MSY) which indicates the start of valid data for each scan line. The number of active samples per line is 1068 for all standards (525 and 625).

Via the MSY line, serial data is transferred which contains information about the main picture such as current line number, odd/even field etc.). It is generated by the deflection circuitry and represents the orthogonal timebase for the entire system.

Feature ICs (e.g. PIP) will be synchronized to the main YC_rC_b bus. Digital insertion (boxing) is controlled by a priority system.

2.3.2. Digital RGB Interface

Digital RGB from text or on-screen-display is connected via the Picture bus. The RGB signal is 5 bits wide. The RGB signals are not subject to any post-filtering. The RGB signal provides 3–bit RGB (one bit per color), the 4th bit allows to display half contrast colors. Bit 5 enables a programmable color–look–up table with 16 entries and 4 bit resolution per color. This allows the support of a World System Teletext level-2 color display. Display contrast for RGB data can be adjusted separately by three contrast multipliers.

2.3.3. Priority Codec

Up to eight digital YC_rC_b or RGB sources (main decoder, PIP, OSD, Text, etc.) may be selected in real-time by means of a 3-bit priority bus. Thus a pixelwise bus arbitration and source switching is possible. It is essential that all YC_rC_b-sources are synchronous and orthogonal.

In general each source (= master) has its own YC_rC_b bus request. This bus request may either be software or hardware-controlled, i.e. a fast blank signal. Data collision is avoided by a bus arbiter that provides the individual bus acknowledge in accordance to a user defined priority.

Each master sends a bus request with his individual priority ID onto the PRIO-bus and immediately reads back the bus status. Only in case of positive arbitration (send-PRIO-ID = read-PRIO-ID) the bus acknowledge becomes active and the data is sent.

This treatment has many features that have impact on the appearance of a TV picture:

real-time bus arbitration (PIP, OSD, ...)
priorities are software configurable
different coefficients for different sources

2.4. Display Processor

In the display processor the conversion from digital YC_rC_b to analog RGB is carried out. A block diagram is shown in figure 2–18. In the luminance processing path contrast and brightness adjustments and variety of features such as black level expansion, dynamic peaking and soft limiting are provided. In the chrominance path, the C_rC_b signals are converted to 20.25 MHz sampling rate and filtered by a color transient improvement circuit. The YC_rC_b signals are converted by a programmable matrix to RGB color space.

The signals inserted via the YC_rC_b bus are identified by their respective priority. The display processor provides separate control settings for two pictures, i.e. different coefficients for a 'main' and a 'side' picture.

The digital RGB insertion circuit allows the insertion of a 5 bit RGB signal. The color space for this signal is controlled by a programmable color look up table (CLUT) and contrast adjustment.

The RGB signals and the display clock are synchronized to the horizontal flyback. For the display clock a gate delay phase shifter is used. The RGB signals are synchronized by a FIFO. In the analog back-end, three 10-bit digital-to-analog converters provide the analog output signals.

2.4.1. Contrast Adjustment

The 8 bit luminance input is multiplied by a factor of 0 ... 2 in 64 steps. A 2-bit noise shaping on the result is used to increase the resolution of the luma signal. Contrast adjustment is separate for main and side picture.

2.4.2. Black Level Expander

The black level expander enhances the contrast of the picture. Therefore the luminance signal is modified with an adjustable, nonlinear function. Dark areas of the picture are changed to black, while bright areas remain unchanged. The advantage of this black level expander is that the black expansion is performed only if there is a large dynamic range in the video signal and when it will be most noticeable to the viewer.

The black level expander works adaptively. Depending on the measured amplitudes 'L_{min}' and 'L_{max}' of the low-pass-filtered luminance and an adjustable coefficient BTLT, a tilt point 'L_t' is being established by

$$L_t = L_{min} + BTLT\ (L_{max} - L_{min}).$$

Above this value there is no expansion, while all luminance values below this point are expanded according to:

$$L_{out} = L_{in} + BAM\ (L_{in} - L_t)$$

A second threshold, L_{tr}, can be programmed, above which there is no expansion. The characteristics of the black level expander are shown in Fig. 2–14 and Fig. 2–15.

The tilt point L_t is a function of the dynamic range of the video signal. Thus, the black level expansion is only performed when the video signal has a large dynamic range. Otherwise, the expansion to black is zero. This allows the correction of the characteristics of the picture tube.

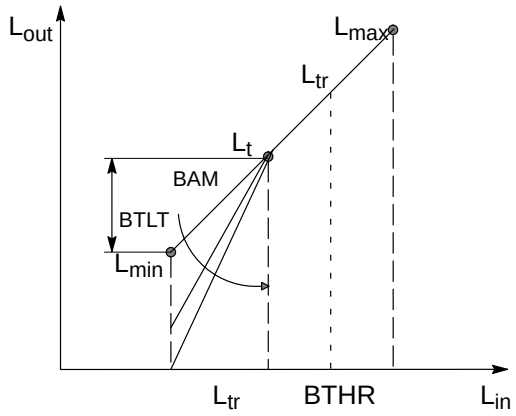


Fig. 2–14: Characteristics of the black level expander

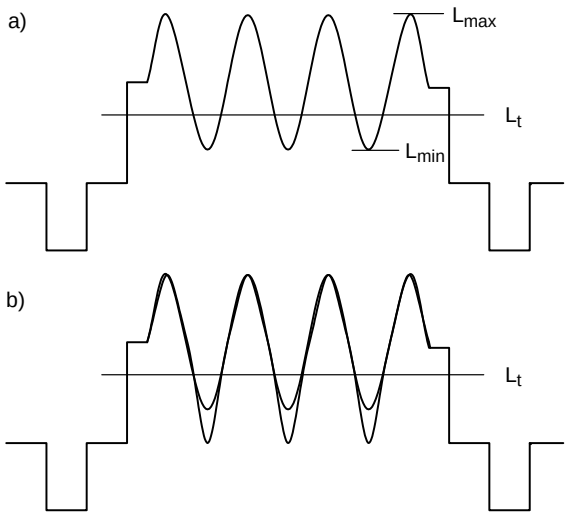


Fig. 2–15: Black-level-expansion
a) luminance input
b) luminance output

2.4.3. Dynamic Peaking

Especially with composite input signals and notch filter luminance separation, it is necessary to improve the luminance frequency characteristics.

In DIGIT3000 the luma response is improved by 'dynamic' peaking. The algorithm has been optimized regarding step and frequency response. It adapts to the amplitude of the high frequency part. Small amplitudes are enhanced while large amplitudes stay nearly unmodified.

The dynamic range can be adjusted to 0 ... +14 dB for small high frequency signals. Adjustment is separate for signal overshoot and for signal undershoot. For large signals the dynamic range is limited by a nonlinear function that does not create any visible alias components.

The center frequency of the peaking filter is switchable from 2.5 MHz to 3.2 MHz. For S-VHS and for notch filter color decoding, the total system frequency responses for PAL and NTSC are shown in figure 2–17.

Transients, produced by the dynamic peaking when switching video source signals, can be suppressed via the priority bus.

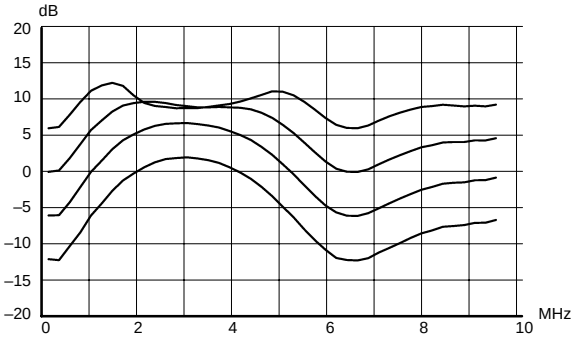


Fig. 2–16: Dynamic peaking frequency response

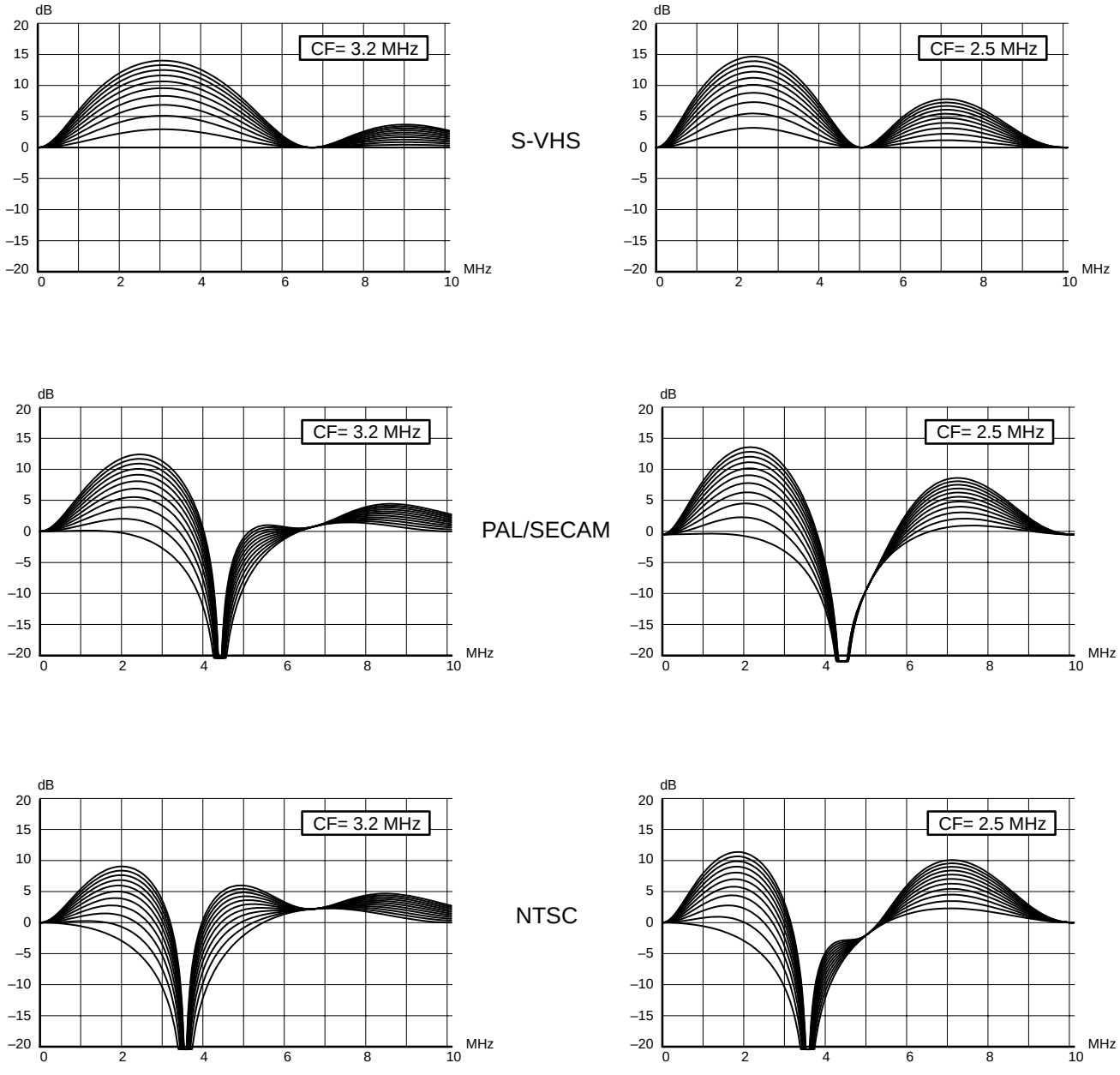


Fig. 2–17: Total frequency response for peaking filter and S-VHS, PAL, NTSC

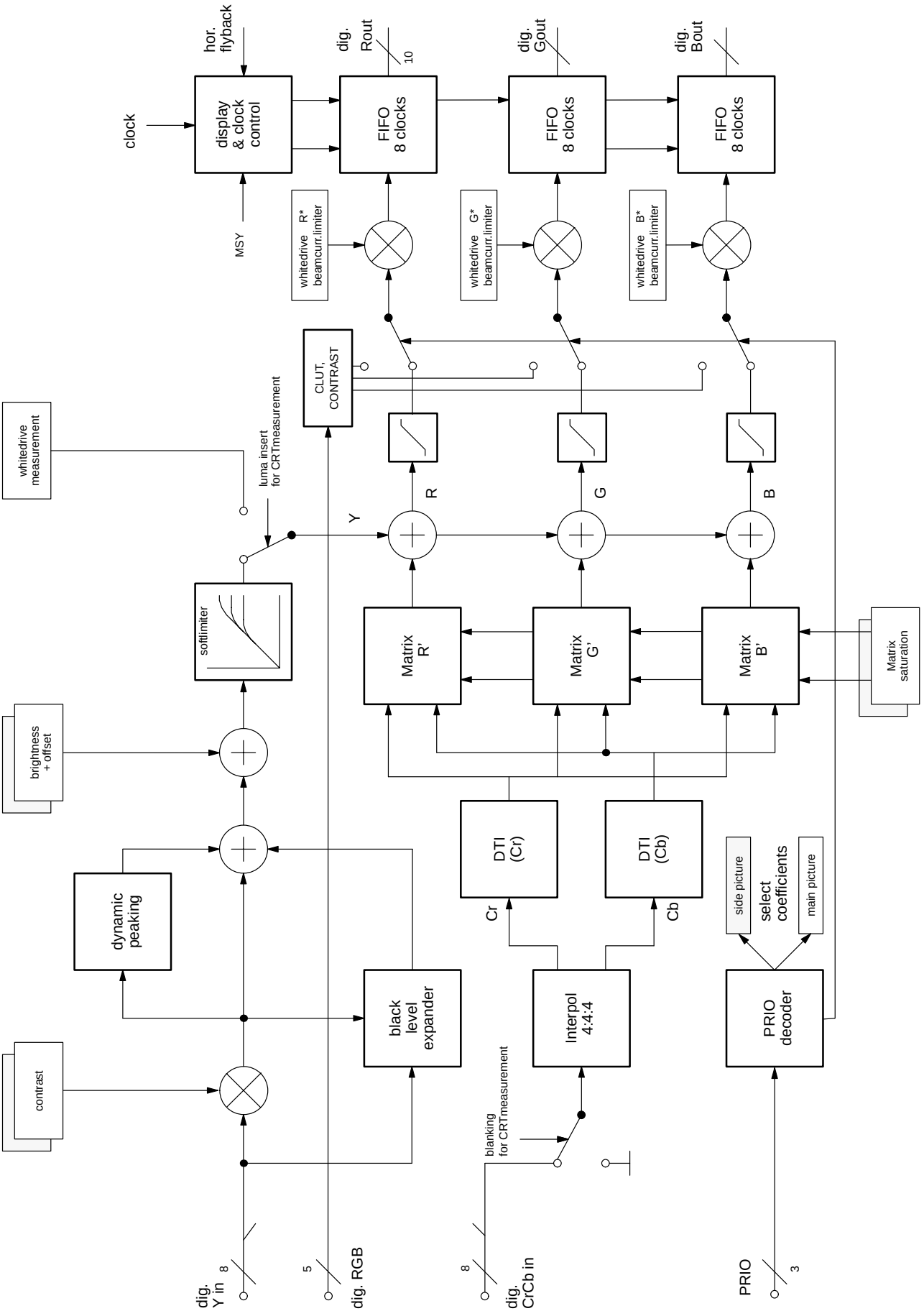


Fig. 2–18: Display processor

2.4.4. Brightness Adjustment

The DC-level of the luminance signal can be adjusted by –30 ... +100 % with 8 bit resolution. It is desirable to keep a small offset with the signal to prevent undershoots from the peaking from being cut. The brightness adjustment is separate for main and side picture.

2.4.5. Soft Limiter

The dynamic range of the processed luma signal must be limited to prevent the CRT from overload. An appropriate headroom for contrast, peaking and brightness can be adjusted by the manufacturer according to the CRT-characteristic. All signals higher than above this limit will be 'soft'-clipped. The soft limiter can support or even replace an analog beam current limiter. Aliasing due to signal limitation is avoided by using a filterbank with individual limiter circuits.

A block diagram of the soft limiter is shown in figure 2–19. The signal is split into high and low frequency bands. The low frequency part represents the average picture level; if the average level is too high the picture tube will overheat and produce coloration. The high frequency part represents the peak picture level which can be considerably higher than the average picture level. Due to this characteristic of the picture tube, both components are treated individually and are later recombined. For the low frequency band a limiter with adjustable threshold is used. The high frequency components produced in the limiter are below the nyquist frequency, therefore no disturbing alias frequencies are generated. For the high frequency band, the limiting is done by a variable gain notch filter, effectively bounding the peak to peak amplitude of the signal. In this way the signal is limited without generating unwanted aliasing.

When the high and low frequency bands are added together again a second limiter sets the exact signal amplitude range. The state of this limiter is used to control the attenuation of the variable notch filter.

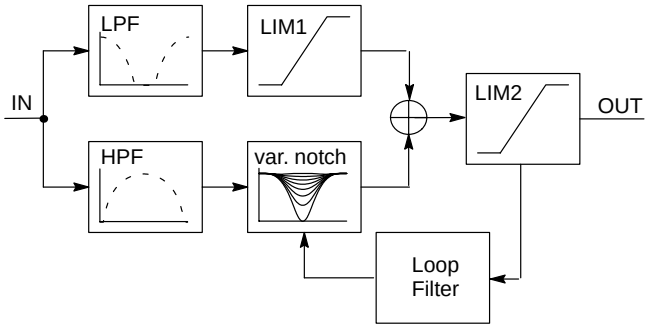


Fig. 2–19: Block diagram of the soft limiter

2.4.6. Chroma Interpolation

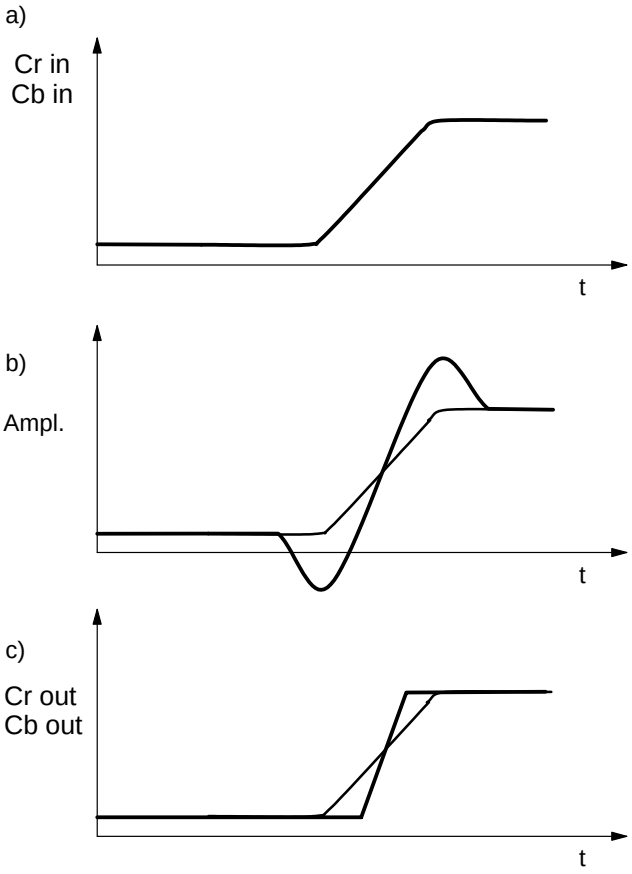
A linear phase interpolator is used to convert the chroma sampling rate from 10.125 MHz (4:2:2) to 20.25 MHz (4:4:4). The frequency response of the interpolator is shown in fig. 2–20. All further processing is carried out at the full sampling rate.

Fig. 2–20: Frequency response of the chroma interpolation filter

2.4.7. Chroma Transient Improvement

The intention of this block is to enhance the chroma resolution. A correction signal is calculated by differentiation of the color difference signals. The differentiation can be adjusted according to the signal bandwidth, e.g. for PAL/NTSC/SECAM or digital component signals respectively. The amplitude of the correction signal is adjustable independently for the Cr/Cb signals. Small

noise amplitudes in the correction signal are suppressed by an adjustable coring circuit. To eliminate 'wrong colors' , which are caused by over and undershoots at the chroma transition, the sharpened chroma signals are limited to a proper value automatically.



a) Cr Cb input of DTI
b) Cr Cb input + Correction signal
c) sharpened and limited Cr Cb

Fig. 2–21: Digital Color Transient Improvement

2.4.8. Dematrix

A 6-multiplier matrix transcodes the Cr and Cb signals to R–Y, B–Y and G–Y. The multipliers are also used to adjust color saturation in the range of 0 ... 2. The coefficients are signed and have a resolution of 9 bits. The matrix coefficients are separate for main and side picture. The matrix computes:

R–Y = MR1*Cb + MR2*Cr
G–Y = MG1*Cb + MG2*Cr
B–Y = MB1*Cb + MB2*Cr

The initialization values for the matrix are computed from the standard ITUR matrix:

$$\begin{pmatrix} R \\ G \\ B \end{pmatrix} = \begin{pmatrix} 1 & 0 & 1.402 \\ 1 & -0.345 & -0.713 \\ 1 & 1.773 & 0 \end{pmatrix} \begin{pmatrix} Y \\ Cb \\ Cr \end{pmatrix}$$

For a contrast setting of CTM=32 the matrix values are scaled by a factor of 64, see also table 3–1.

2.4.9. RGB Processing

After adding the post processed luma, the digital RGBs are limited to 10 bits. Three multipliers are used to digitally adjust the whitedrive. Using the same multipliers an average beam current limiter is implemented. See also paragraph 'CRT control'.

2.4.10. FIFO Display Buffer

A FIFO is used to buffer the phase differences between the video source and the flyback signal. By using the described clock system, this 'phase-buffer' is working with sub-pixel accuracy. It has a range of 8 clocks which is equivalent to +/– 200 ns @ 20.25 MHz.

2.5. Analog Back End

The digital RGB signals are converted to analog RGBs using three video digital to analog converters (DAC) with 10 bit resolution. An analog brightness value is provided by three additional DACs. The adjustment range is 40% of the full RGB range.

The back end allows insertion of an external analog RGB signal. The RGB signal is key-clamped and inserted into the main RGB by the fast blank switch. The external RGB signals are virtually handled as priority bus signals. Thus they can be overlaid or underlaid to the digital picture. The external RGB signals can be independently adjusted in DC-level (brightness) and magnitude (contrast).

The controls for the whitedrive / analog brightness and also for the external contrast and brightness adjustments are via the Fast Processor. The controls for the cutoff DACs are via I^2C bus registers.

Finally cutoff and blanking values are added to the RGB signals. Cutoff (dark current) is provided by three 9-bit DACs. The adjustment range is 60% of full scale RGB range.

The analog RGB-outputs are current outputs with current-sink characteristics. The maximum current drawn by the output stage is obtained with peak white RGB.

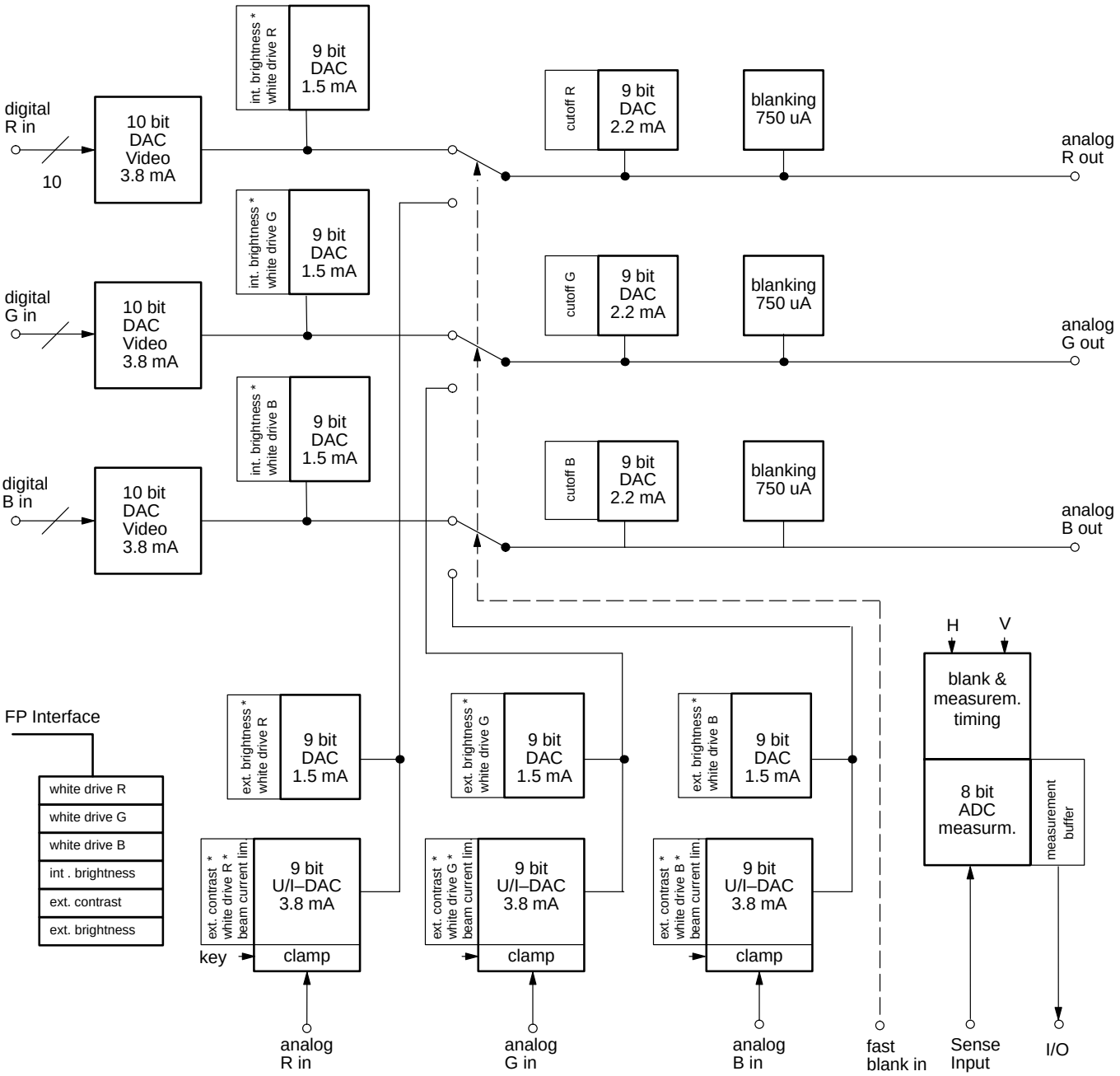


Fig. 2–22: Analog back end

2.5.1. CRT Measurement and Control

The display processor is equipped with an 8 bit PDM-ADC for all measuring purposes. The ADC is connected to the Sense input pin, the input range is 0...1.5V. The bandwidth of the PDM filter can be selected; the measurement window is 19/9.5 µs for small/large bandwidth setting. The input impedance is more than 1 MΩ.

Cutoff and white drive current measurement is carried out during the vertical blanking interval. It is always using the small bandwidth setting. The current range for the cutoff measurement is set by connecting a sense resistor to then MADC input. For the whitedrive measurement, the range is set by using a sense resistor and the range select switch 2 output pin. During the active picture the minimum and maximum beam current is measured. The measurement range can be set by using the range select switch pin. The timing window of this measurement is programmable. The intention is to automatically detect letterbox transmission or to measure the actual beam current. All control loops are closed via the external control microprocessor.

In each field two sets of measurements can be taken:
a) The picture tube measurement returns results for

cutoff R
cutoff G
cutoff B
white drive R or G or B (sequentially).

b) The picture measurement returns
active picture maximum current
active picture minimum current.

The tube measurement is automatically started when the cutoff blue result register is read. Cutoff control for RGB requires one field only while a complete white-drive control requires three fields. If the measurement mode is set to 'offset check' a measurement cycle is run with the cutoff / whitedrive signals set to zero. This allows to compensate the MADC offset as well as input the leakage currents. During cutoff and whitedrive measurements, the average beam current limiter function (ref. 2.5.2.) is switched of and a programmable value is used for the brightness setting. The start line of the tube measurement can be programmed via I^2C bus, the first line used for the measurement, i.e. measurement of cutoff red, is 2 lines after the programmed start line.

The picture measurement must be enabled by the control microprocessor after reading the min./max. result registers. The measurement is always started at the beginning of active video.

The vertical timing for the picture measurement is programmable, and may even be a single line. Also the signal bandwidth is switchable for the picture measurement.

Two horizontal windows are available for the picture measurement. The large window is active for the entire active line. Tube measurement is always carried out with the small window. Measurement windows for picture and tube measurement are shown in figure 2–23.

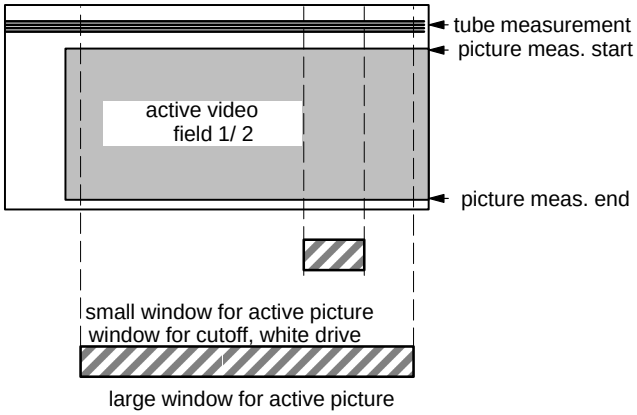


Fig. 2–23: Windows for tube and picture measurement

2.5.2. Average Beam Current Limiter

The average beam current limiter (BCL) uses the sense input for the beam current measurement. The BCL uses a different filter to average the beam current during the active picture. The filter bandwidth is approximately 2 kHz. The beam current limiter has an automatic offset adjust that is active two lines before the first cutoff measurement line.

The beam current limiter allows to set a threshold current. If the beam current is above the threshold, the excess current is low pass filtered and used to attenuate the RGB outputs by adjusting the white drive multipliers for the internal (digital) RGB signals and the analog contrast multipliers for the analog RGB inputs respectively. The lower limit of the attenuator is programmable, thus a minimum contrast can always be set. During the tube measurement the ABL attenuation is switched off. After the whitedrive measurement line it takes 3 lines to switch back to BCL limited drives and brightness.

Typical characteristics of the ABL for different loop gains are shown in Fig. 2–24; for this example the tube has been assumed to have a square law characteristic.

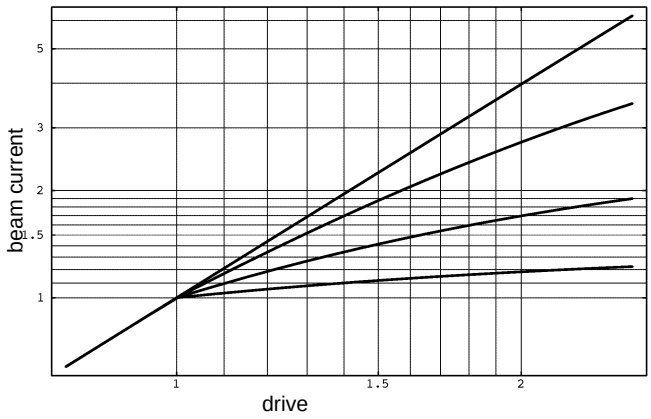


Fig. 2–24: Beam current limiter characteristics:
beam current output vs. drive
BCL threshold: 1

2.6. Synchronization and Deflection

The synchronization and deflection processing is distributed over front end and back end. The video clamping, horizontal and vertical sync separation and all video related timing information are processed in the front end. Most of the processing that runs at the horizontal frequency is programmed on the internal Fast Processor (FP). Also the values for vertical & East-West deflection are calculated by the FP software.

The display related synchronization, i.e. generation of horizontal and vertical drive and synchronization of horizontal and vertical drive to the video timing extracted in the front end, are implemented in hardware.

2.6.1. Video Sync Processing

Fig. 2–25 shows a block diagram of the front end sync processing. To extract the sync information from the video signal, a linear phase lowpass filter eliminates all noise and video contents above one MHz. The sync is separated by a slicer, the sync phase is measured. A variable window can be selected to improve the noise immunity of the slicer. The phase comparator measures the falling edge of sync as well as the integrated sync pulse.

The sync phase error is filtered by a phase locked loop that is computed by the FP. All timing in the front end is derived from a counter that is part of this PLL and it thus counts synchronously to the video signal.

A separate hardware block measures the signal back porch and also allows to gather maximum/minimum of the video signal. This information is processed by the FP and used for of gain control and clamping.

For vertical sync separation the sliced video signal is integrated. The FP uses the integrator value to derive vertical sync and field information.

The information extracted by the video sync processing is multiplexed onto the hardware front sync signal (FSY) and is distributed to the rest of the video processing system. The format of the front sync signal is given in fig. 2–26.

The data for the vertical deflection, the sawtooth and the East-West correction signal is calculated by the FP. The data is buffered in a FIFO and transferred to the back end by a single wire interface.

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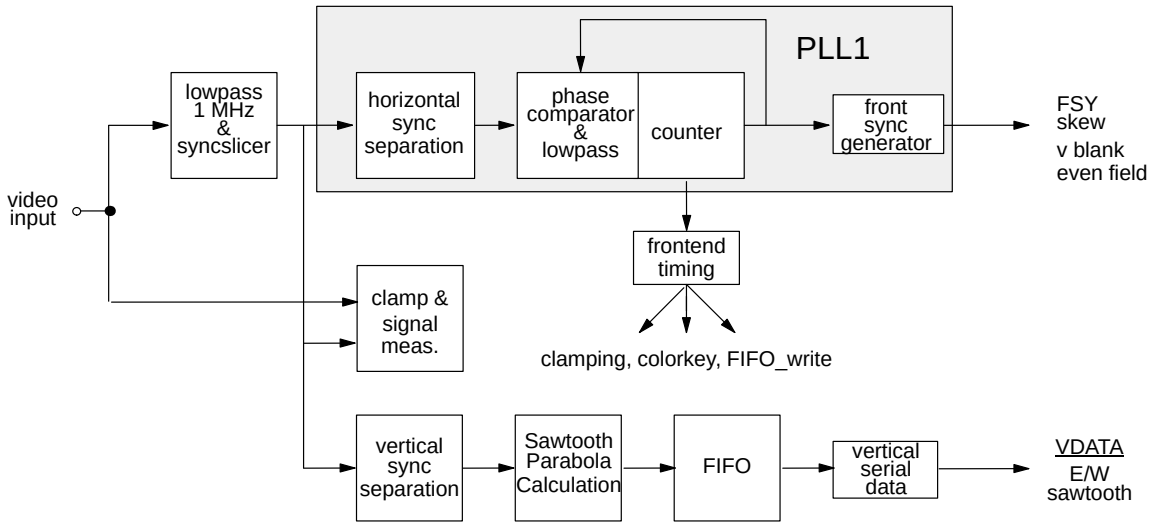


Fig. 2–25: Sync separation block diagram

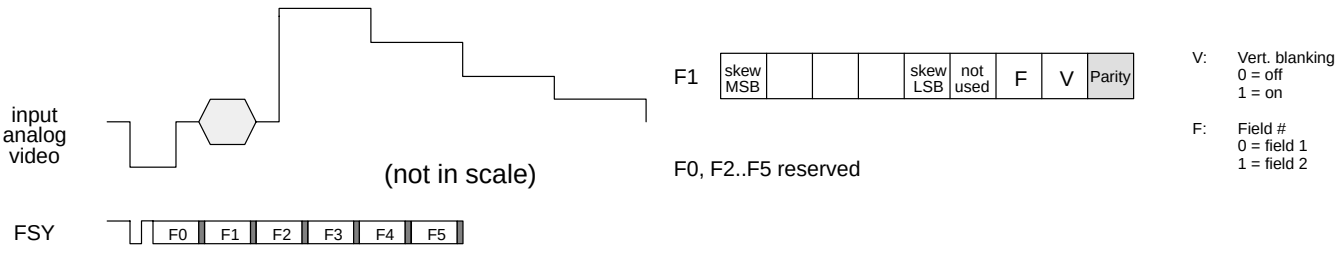


Fig. 2–26: Front sync format

2.6.2. Deflection Processing

The deflection processing generates the signals for the horizontal and vertical drive (fig. 2–27). This block contains two phase-locked loops:

– PLL2 generates the horizontal and vertical timing. Phase and frequency are synchronized by the front sync signal. The Main Sync (MSY) signal that is generated from PLL2 is a multiplex of all display related data (fig. 2–28). This signal is intended for use by other processors, e.g. a PIP processor can use this signal to adjust to a certain display position.

– PLL3 adjusts the phase of the horizontal drive pulse and compensates for the delay of the horizontal output stage.

The horizontal drive circuitry uses a digital sine wave generator to produce the exact (subclock) timing for the drive pulse. The generator runs at 1 MHz; in the output stage the frequency is divided down to give drive-pulse period and width. In standby mode, the output stage is driven from an internal 1 MHz clock that is derived from the 20 MHz main clock oscillator and a fixed drive pulse width is used. When the circuit is switched out of standby operation the drive pulse width is programmable. The horizontal drive uses a high voltage (8V) open drain output transistor.

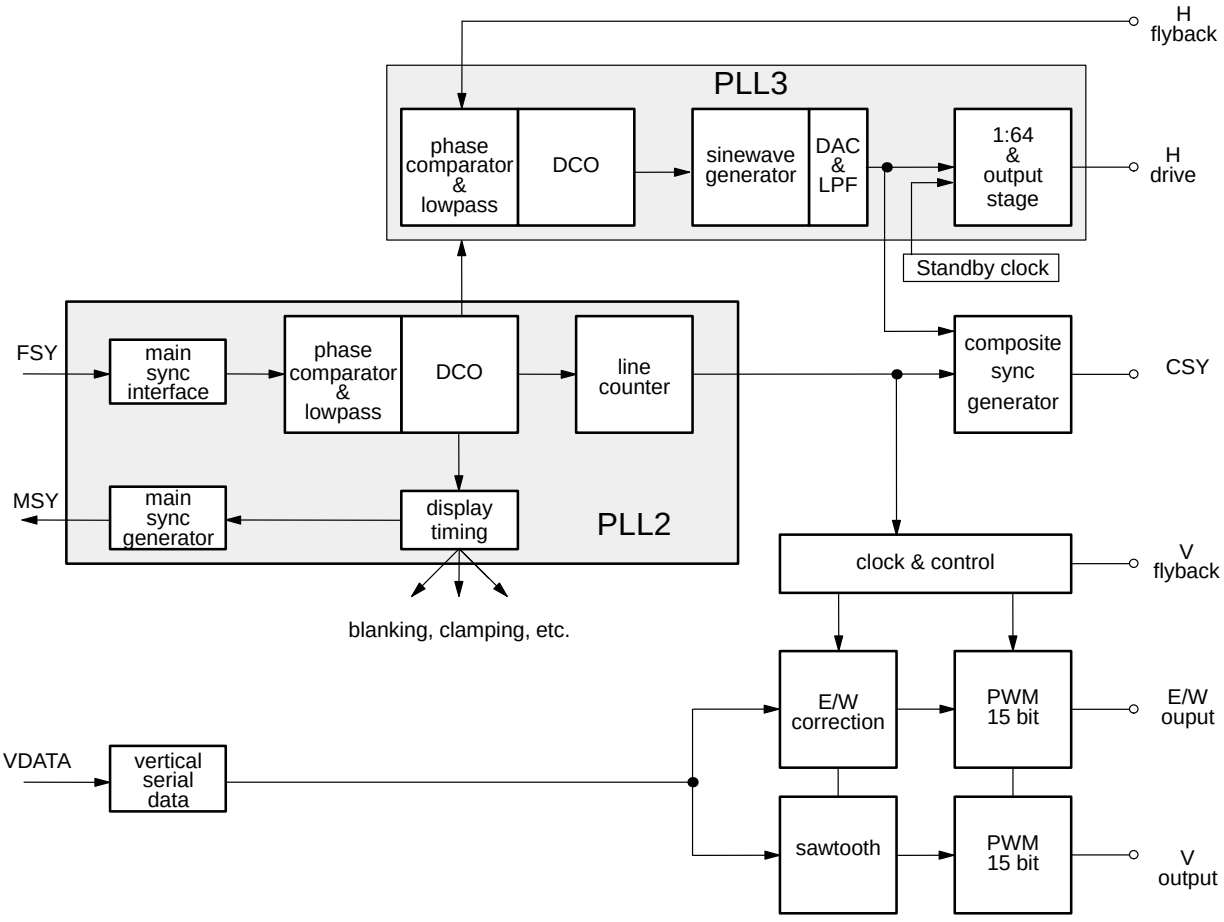


Fig. 2–27: Deflection processing block diagram

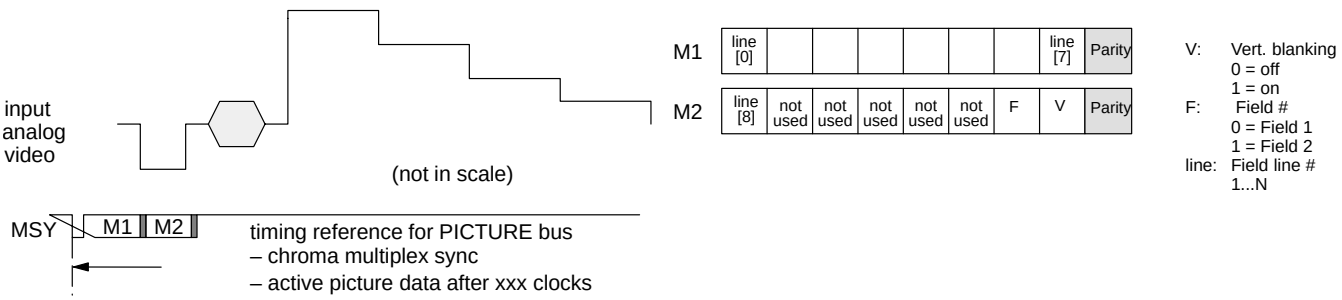


Fig. 2–28: Main sync format

2.6.3. Vertical, East–West Deflection

The calculations of the vertical and east–west deflection waveforms are done by the fast processor. The algorithm is using a chain of accumulators to generate the required polynomial waveforms. To produce the deflection waveforms, the accumulators are initialized at the beginning of each field. The initialization values must be computed by the control processor and are written once to the fast processor of the VDP3108. The waveforms are described as polynomials in x, where x varies from 0 to 1 for one field.

$P: a + b(x–0.5) + c(x–0.5)^2 + d(x–0.5)^3 + e(x–0.5)^4$

The initialization values for the accumulators a0..a3 for vertical deflection and a0..a4 for east–west deflection are 12 bit values. The coefficients that should be used to calculate the initialization values for different field frequencies are given is section 3.

The vertical waveform can be scaled according the average beam current. This is used to compensate the effects of electric high tension changing due to beam current variations. In order to get a faster vertical retrace timing, the output impedance of the vertical DA converter can be reduced by 50% during the retrace.

Fig. 2–29 shows some vertical and east–west deflection waveforms. The polynomial coefficients are given in the figure.

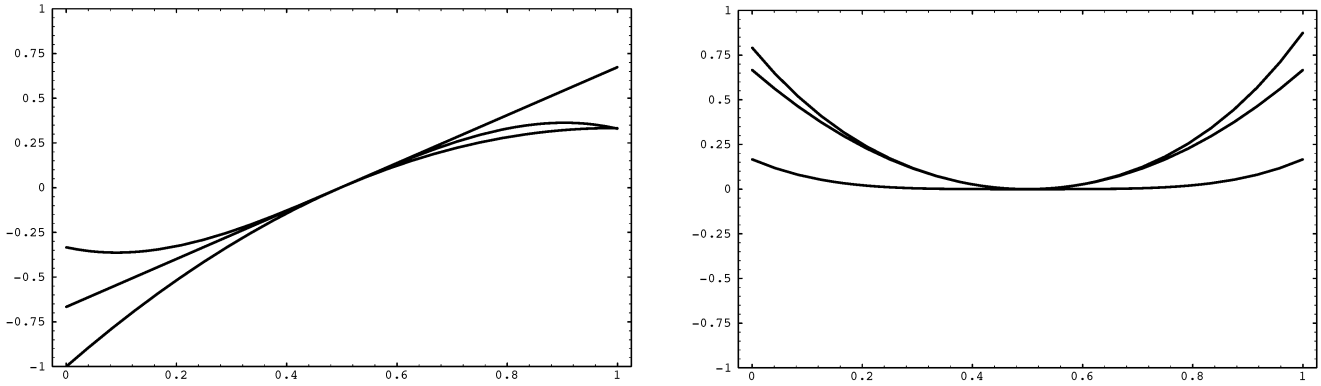


Fig. 2–29: Vertical and East–West Deflection Waveforms

vertical: a,b,c,d	0,1,0,0	east–west: a,b,c,d,e	0,0,1,0,0
	0,1,1,0		0,0,0,0,1
	0,1,0,1		0,0,1,1,1

2.6.4. Protection Circuitry

Picture tube and drive stage protection is provided through the following measures:

– vertical flyback safety input: this pin looks for a negative edge in every field, otherwise the RGB drive signals are blanked.

– drive shutoff during flyback: this feature can be selected by software.

– safety input pin: this pin has two thresholds; at the lower threshold the RGB signals are blanked, at the higher threshold the horizontal drive is shut off.

– The main oscillator and the horizontal drive circuitry are run from a separate (standby) power supply and are already active while the TV set is powering up.

2.7. Reset and Standby Functions

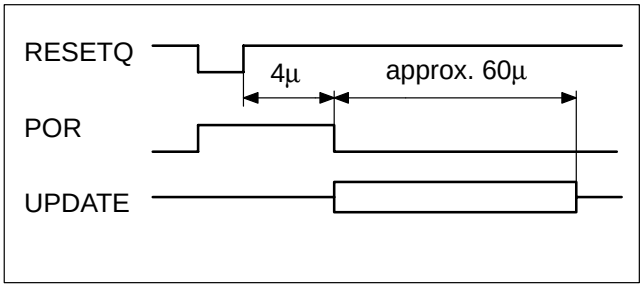
Reset of most functions (exceptions see below) is performed by a reset pin. When this pin becomes active then all the internal registers and counters are set to zero. When this pin is released, the internal reset is still active for 4us. After that time all the internal registers are loaded with the values defined in the defaults ROM. All the registers which are updated with the vertical sync get these values with the next vertical sync. During this initialization procedure (approx. 60 µs) it is not possible to access the VDP via the serial interface (I^2C). Access to other ICs via the serial bus is possible during that time. The same initialization procedure is started when the internal clock supervision detects that there is no clock (in the video processing part).

Exceptions for initialization :

– CCU clock divider (5MHz), not initialized by reset

– standby clock divider (1MHz), not initialized by reset, but clock selector switched to standby clock

During standby, only the horizontal drive pulse (see also 2.6.2.) and the 5 MHz clock output for the control microprocessor are active. The standby circuitry is reset when the standby supply voltage is applied.


RESETQ
4µ
approx. 60µ
POR
UPDATE

3. Serial Interface

3.1. I²C Bus Interface

Communication between the VDP and the external controller is done via I²C bus. The VDP has an I²C bus slave interface and uses I²C clock synchronization to slow down the interface if required. The I²C bus interface uses one level of subaddress: one I²C bus address is used to address the IC and a subaddress selects one of the internal registers. The I²C bus chip address is given below:

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	0	1	0/1

The registers of the VDP have 8 or 16 bit data size; 16 bit registers are accessed by reading/writing two 8 bit data words.

Figure 3–1 shows I²C bus protocols for read and write operations of the interface; the read operation requires an extra start condition and repetition of the chip address with read command set.

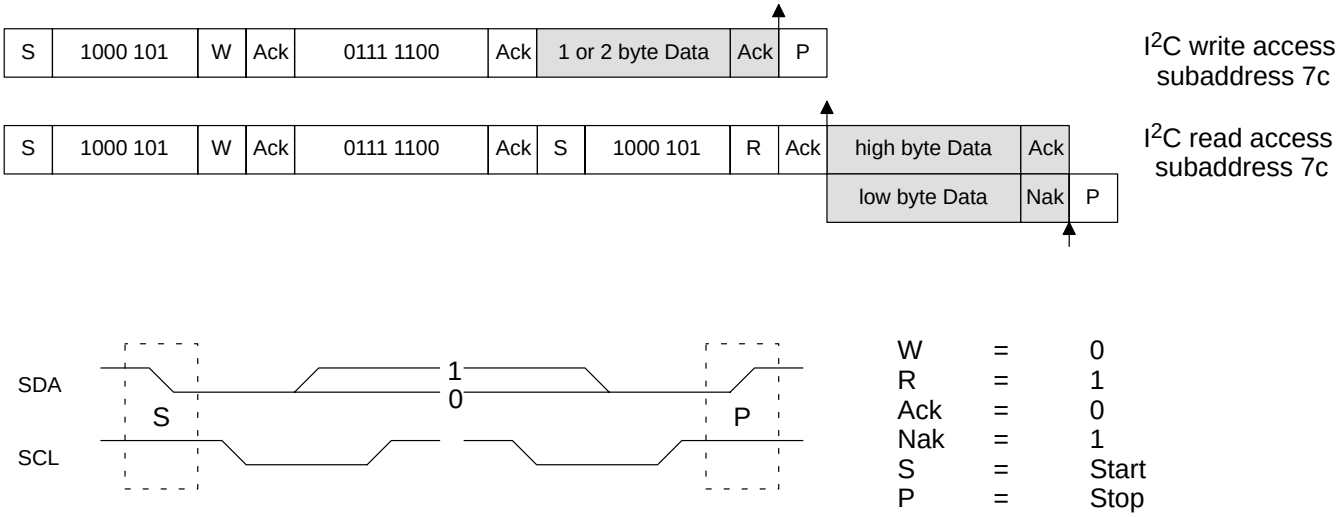


Fig. 3–1: I²C Bus Protocols

3.2. Control and Status Registers

Table 3–1 gives definitions of the VDP control and status registers. The number of bits indicated for each register in the table is the number of bits implemented in hardware, i.e. a 9-bit register must always be accessed using two data bytes but the 7 MSB will be don't care on write operations and 0 on read operations. Write registers that can be read back are indicated in the following table.

Functions implemented by software in the on-chip control microprocessor (FP) are explained elsewhere.

A hardware reset initializes all control registers to 0. The automatic chip initialization loads a selected set of registers with the default values given in Table 3–1.

The register modes given in Table 3–1 are:

w	write only register
w/r	write/read data register
r	read data from VDP
v	register is latched with vertical sync

The mnemonics used in the Intermetall VDP demo software are given in the last column.

Table 3–1: Control and status registers

I^2C Sub address	Number of bits	Mode	Function	Default	Name
	FP INTERFACE				
26	16	w	FP read address		FPRD
27	16	w	FP write address		FPWR
28	16	w/r	FP data		FPDAT
29	8	r	FP status bit [0] write request bit [1] read request bit [2] busy		FPSTA
	FRONTEND				
33	8	w/r	input selector luma adc: bit [1:0] 00 VIN3 01 VIN2 10 VIN1 11 reserved input selector, chroma adc: bit [2] 0/1 select VIN1/CIN clamping modes: bit [3] 0/1 clamp on/off for chroma ad converter bit [4] 0/1 internal/external clamp enable (luma adc) bit [7:5] reserved		VIS CS DCLC DCLY
	CHROMA PROCESSING				
20	8	w/r	IF compensation: bit [1:0] 0 12 dB 2 6 dB/oct 3 0 dB/oct bit [7:2] reserved	3	IFC
22	8	w/r	SECAM deemphasis or PAL lowpass peaking filter (1.25 MHz): bit [4:0] 0...31, PAL/NTSC: 8 SECAM: 24 bit [5] reserved chroma bandwidth select: luma delay adjust (LDY) PAL/NTSC SECAM bit [7:6] 00 narrow 0 25 01 normal 3 28 10 broad 6 31 11 reserved	8 1	DEEM CBW
	LUMA PROCESSING				
30	8	w/r	luma notch frequency bit [5:0] 0..63/64 YNF = 128 · cos (2π f_f/f_S) PAL/SECAM: 25 NTSC: 57 bit [6] 0/1 1: disable adaptive notch filter for SECAM must be set to 0 in PAL/NTSC bit [7] reserved	25 0	YNF YNMD
31	8	w/r	luma / chroma matching delay: bit [4:0] 0..31 delay in clocks (+19) bit [7:5] reserved	3	LDF

I²C Sub address	Number of bits	Mode	Function	Default	Name
34	8	w/r	standard select: bit [2:0] 000 SECAM 100 SECAM–SVHS 001 PAL, NTSC compensated 101 PAL–SVHS, NTSC compensated–SVHS 010 NTSC, simple PAL 110 NTSC–SVHS, simple PAL–SVHS 011 NTSC comb filter mode 111 reserved bit [3] 0/1 chroma polarity signed/offset-binary bit [7:4] reserved	9	STS
	PRIORITY BUS – FRONTEND				
23	8	w/r	priority bus overwrite register bit [7:0] 8 bit mask, bit[x] = 1 : overwrite priority x	64	PIOV
24	8	w/r	priority bus ID register and enable bit [2:0] 0..7 priority ID, 0 highest bit [4:3] 0..3 pad driver strength, number of pull-down transistors 1..4 bit [6:5] reserved bit [7] 0/1 disable/enable priority	0 0 1	PID PIDD PIDE
	PRIORITY BUS – BACKEND				
			priority mask register, if bit[x] is set to 1 then the function is active for the respective signal priority		
75	9	w v	bit [7:0] bit [x] 0/1: select main/side picture contrast/brightness/matrix		PBCT
71	9	w v	bit [7:0] bit [x] 0/1: select main/external (via CLUT) RGB		PBERGB
7d	9	w v	bit [7:0] bit [x] 0/1: disable/enable black level expander		PBBLE
79	9	w v	bit [7:0] bit [x] 0/1: disable/enable peaking transient suppression when signal is switched		PBPK
53	9	w v	bit [7:0] bit [x] 0/1: disable/enable analog fast blank input		PBFB
	DISPLAY PROCESSOR – LUMA				
61	9	w v	bit [5:0] 0..63/32 main picture contrast	32	CTM
65	9	w v	bit [5:0] 0..63/32 side picture contrast	32	CTS
51	9	w v	bit [8:0] –256..255 main picture brightness	0	BRM
55	9	w v	bit [8:0] –256..255 side picture brightness		BRS
2a	16	w/r	bit [10:0] reserved bit [11] 0/1 disable/enable luma input –16	1	EY16
59	9	w v	black level expander: bit [3:0] 0..15 tilt coefficient (k2) bit [8:4] 0...31 amount (k1)	6 4	BTLT BAM
5d	9	w v	black level expander: bit [8:0] 0..511 disable expansion, threshold value	120	BTHR

I²C Sub address	Number of bits	Mode	Function	Default	Name
69	9	w v	luma peaking filter, the gain at high frequencies and small signal amplitudes is: 1 + (k1+k2)/8 bit [3:0] 0..15 k1: peaking level undershoot bit [7:4] 0..15 k2: peaking level overshoot	 4 4	 PKUN PKOV
6d	9	w v	luma peaking filter, coring bit [5:0] 0..31 coring level bit[7:6] reserved bit[8] 0/1 peaking filter CF 2.5/3.2 MHz	 1 0	 COR PFS
4d	9	w v	luma soft limiter bit[7:0] 0..255 maximum limit for low frequency comp.	 255	 SLDC
49	9	w v	luma soft limiter bit[7:0] 0..255 maximum limit for output signal	 255	 SLO
41	9	w v	luma soft limiter bit[4:0] 0..31 loop filter gain bit[5] 0/1 enable/disable noise reduction		 SFG DNO
45	9	w v	luma soft limiter bit[4:0] 0..31 notch filter gain (for manual notch) bit[5] 0/1 automatic/manual notch		 SFGM SLM
	DISPLAY PROCESSOR – CHROMA				
14	8	w/r v	luma / chroma matching delay bit [2:0] –2...2 variable chroma delay bit [3] 0/1 chroma polarity signed/offset binary	 0 1	 LDB COB
72	9	w v	digital transient improvement bit [4:0] 0..31 transient gain Cr bit [8:5] 0..15 coring level for Cr, Cb	 31 3	 CPKV CCOR
7a	9	w v	digital transient improvement bit [4:0] 0..31 transient gain Cb bit [7:5] reserved bit [8] 0/1 filter characteristic broad/narrow	 31 1	 CPKU CFS
	DISPLAY PROCESSOR – MATRIX				
7c/74	9	w v	main picture matrix coefficient R–Y = MR1M*Cb + MR2M*Cr bit[9:0] –256 ... 255/128	0 86	MR1M, MR2M
6c/64	9	w v	main picture matrix coefficient G–Y = MG1M*Cb + MG2M*Cr bit[9:0] –256 ... 255/128	–22 –44	MG1M, MG2M
5c/54	9	w v	main picture matrix coefficient B–Y = MB1M*Cb + MB2M*Cr bit[9:0] –256 ... 255 /128	113 0	MB1M, MB2M
78/70	9	w v	side picture matrix coefficient R–Y = MR1S*Cb + MR2S*Cr bit[9:0] –256 ... 255/128	0 73	MR1S, MR2S
68/60	9	w v	side picture matrix coefficient G–Y = MG1S*Cb + MG2S*Cr bit[9:0] –256 ... 255/128	–19 –37	MG1S, MG2S
	DISPLAY PROCESSOR – COLOR LOOK-UP TABLE				
58/50	9	w v	side picture matrix coefficient B–Y = MB1S*Cb+ MB2S*Cr bit[9:0] –256 ... 255/128	97 0	MB1S, MB2S

I²C Sub address	Number of bits	Mode	Function	Default	Name
00–0f	16	w v	color look-up table: 16 entries, 12 bit wide, The CLUT registers are initialized at power-up bit [3:0] 0..15 blue amplitude bit [7:4] 0..15 green amplitude bit [11:8] 0..15 red amplitude		 CLUT0 ... CLUT15
4c/48/ 44	9	w v	digital RGB insertion contrast for R/G/B bit [3:0] 0..13 RGB amplitude is CLUT*(4+x), RGB amplitude range is from 0 to 255 14,15 invalid	 8 8 8	 DRCT DGCT DBCT
	DISPLAY PROCESSOR – DISPLAY CONTROLS				
6e 6a 66	9	w v	cutoff R/G/B		CR CG CB
	DISPLAY PROCESSOR – TUBE AND PICTURE MEASUREMENT				
7b	9	w v	picture measurement start bit [8:0] 0..511 first line of picture measurement	23	PMST
77	9	w v	picture measurement stop bit [8:0] 0..511 last line of picture measurement	308	PMSO
7f	9	w v	tube measurement line bit [8:0] 0..511 line for tube measurement	15	TML
25	8	w/r	tube and picture measurement control bit [0] 0/1 disable/enable tube measurement bit [1] 0/1 80/40 kHz bandwidth for picture measurement bit [2] 0/1 enable picture measurement start bit [3] 0/1 large/small picture measurement window bit [4] 0/1 measure / offset check for adc bit [7:5] reserved		PMC
13	16	w/r	white drive measurement control bit [9:0] 0..1023 white drive value for measurement bit [10] reserved bit [11] 0/1 white drive measurement disabled/enabled	 512 0	 WDRV EWDM
18–1d 18 19 1a 1b 1c 1d	8	r	measurement result registers minimum maximum white drive cutoff/leakage blue, read pulse starts tube measurement cutoff/leakage green cutoff/leakage red	–	 MRMIN MRMAX MRWDR MRCB MRCG MRCR

I²C Sub address	Number of bits	Mode	Function	Default	Name
1e	8	r	measurement adc status and fast blank input status measurement status register bit [0] 0/1 tube measurement active / complete bit [2:1] white drive measurement cycle 00 red 01 green 10 blue 11 reserved bit [3] 0/1 picture measurement active / complete bit [4] 0/1 fast blank input low / high (static) bit [5] 1 fast blank input negative transition (reset at read) bit [7:6] reserved	–	PMS
32	8	w	fast blank interface mode bit [0] 0 fast blank from FBLIN pin 1 force internal fast blank signal to high bit [1] 0/1 fast blank active high/low bit [2] 0 clmpref 1 bit [7:3] reserved	–	FBMD
	DISPLAY PROCESSOR – TIMING				
6f	9	w v	vertical blanking start bit [8:0] 0..511 first line of vertical blanking	305	VBST
73	9	w v	vertical blanking stop bit [8:0] 0..511 last line of vertical blanking	25	VBSO
6b	9	w v	start of active video bit [8:0] 0..511 first line of active video	30	AVST
	DISPLAY PROCESSOR – HORIZONTAL DEFLECTION				
67	9	w v	adjustable delay from front sync to PLL2 adjust analog and digital RGB bit [8:0] –256..+255 +/– 8 µsec	–141	POFS2
63	9	w v	adjustable delay from fly back to PLL2 adjust horizontal position for analog RGB picture bit [8:0] –256..+255 +/– 8 µsec	0	POFS3
7e	9	w v	adjustable delay from fly back to main sync adjust horizontal position for digital picture bit [8:0] allowed values ?	120	HPOS
17	8	w/r	start of horizontal blanking bit [7:0] 0..255 0..t_h	1	HBST
16	8	w/r	end of horizontal blanking bit [7:0] 0..255 0..t_h	48	HBSO

I²C Sub address	Number of bits	Mode	Function	Default	Name
57 5b 5f	9	w v	PLL2/3 filter coefficients, refer to section ‘horizontal deflection’	2 2 2	PKP3 PKP2 PKI2
15	16	w/r d	horizontal drive control register bit [5:0] 0..63 horizontal drive pulse duration in µsec bit [6] 0/1 disable/enable horizontal pll loops bit [7] 0/1 1: gate HOUT off during flyback bit [8] 0 bit [9] 0/1 enable/disable ultra black blanking bit [10] 0/1 force/enable blanking after reset bit [11] 0/1 enable/disable analog RGB clamping bit [12] 0/1 disable/enable composite sync(ref.bit[15]) bit [13] 0/1 enable/disable vertical protection bit [14] 0/1 bypass/active display clock skew bit [15,12] function of CSIO pin 00 composite sync signal output 01 25 Hz output (field1/field2 signal) 10 no interlace (field 2), output = 0 11 1 MHz h–drive clock	32	HDRV EHPLL EFLB DUBL EBL DCRGB DVPR CSKEW CSYNC
TEST REGISTER					
39	8	w/r	Main Test Register		
3f	8	w/r	Front End, Luma1		
3e	8	w/r	Front End, Luma2		
3d	8	w/r	Front End, Luma3		
2f	8	w/r	Front End, Chroma1		
2e	8	w/r	Front End, Chroma2		
2a	16	w/r	Display 1		
2b	16	w/r	Display 2		
2c	8	w/r	Display 3		
3a	8	w/r	FP		
3b	16	w/r	Display Processor Control		
2d	16	w/r	Deflection		
3c	8	w/r	Analog Backend		

Table 3–2: Control Registers of the Fast Processor

– default values are initialized at reset
– * indicates that register is initialized according to the current standard when SDT register is changed.

FP Sub address	Function	Default	Name
	Standard Selection		
h'1b	Standard select: 0 PAL B,G,H,I (50 Hz) 4.433618 1 NTSC M (60 Hz) 3.579545 2 SECAM (50 Hz) 4.286 3 NTSC44 (60 Hz) 4.433618 4 PAL M (60 Hz) 3.575611 5 PAL N (50 Hz) 3.582056 6 PAL 60 (60 Hz) 4.433618 7 NTSC COMB (60 Hz) 3.579545 The activated routine will set up several blocks for the selected standard. Option bits: (OR for the new selected standard) h'100 no hpll setup h'200 no vertical setup h'400 no acc setup Note: After FP has switched to a new standard, the MSB of SDT is set to 1 to indicate operation complete.	0	SDT
	Color Processing		
h'1c	NTSC tint angle, $\pm 512 = \pm \pi/4$	0	TINT
h'a0	ACC reference level to adjust C_r, C_b levels on picture bus. (use main matrix) ACCREF = 0: ACC function is disabled, chroma gain can be adjusted via ACCb / ACCr register ACC reference level for increased color saturation. (use side matrix)	P/N: 2070* S: 0* P/N: 2263	ACCREF
h'a3	ACC multiplier value for SECAM Dr chroma component to adjust C_r level on picture bus. (use main matrix) b[10:0] eeemmmmmmmm m * 2^–e ACC multiplier value for SECAM Dr chroma component for increased color saturation (use side matrix)	S: 1496* S:1532	ACCr
h'a4	ACC multiplier value for SECAM Db chroma component to adjust C_b level on picture bus. (use main matrix) b[10:0] eeemmmmmmmm m * 2^–e ACC multiplier value for SECAM Dr chroma component for increased color saturation (use side matrix)	S: 1155* S: 1177	ACCb
h'a8	amplitude color killer level (0:killer disabled)	30	KILVL
h'a9	amplitude color killer hysteresis	10	KILHY

FP Sub address	Function	Default	Name
	Vertical Standard Select		
h'e7	vertical standard select if LSB is set to one, lock to standard signal is enabled	50Hz: 625* 60Hz: 525*	VSDT
	AGC – DVCO		
h'b2	sync amplitude reference (0: AGC disabled). Write 0 to register h'b5 after writing 0 to AGCREF to disable the AGC	768	AGCREF
h'be	start value for AGC gain while vertical lock or AGC is inactive	27	SGAIN
h'20	AGC gain value (read only if AGC is enabled)	read only	GAIN
h'58	crystal oscillator center frequency adjust, –2048..2047	0	DVCO
h'59	crystal oscillator center frequency adjustment value for line lock mode. true adjust value is DVCO – ADJUST. For factory crystal alignment: set DVCO=0, set lock mode, read crystal offset from ADJUST register and use negative value for initial center frequency adjustment via DVCO.	read only	ADJUST
h'26	line locked mode lock command/status write: 100 enable lock 0 disable lock read: 4095/0 locked / unlocked	0	XLG
	FP Status Register		
'53	automatic standard recognition status bit0 1 vertical sync detected bit1 2 horizontally locked bit2 4 reserved bit3 8 color killer active bit5 32 ident killer active	–	ASR
h'eb	number of lines per field, P/S: 312, N: 262	read only	NLPF
h'41	measured sync amplitude value, nominal: 768	read only	SAMPL
h'a5	measured burst amplitude	read only	BAMPL
h'50	software version number: 2105	read only	–
h'5f	software release: 1001	read only	–
	FP Display Control Register		
h'f0	White Drive Red (0...1023)	700	WDR [1)]
h'f1	White Drive Green (0...1023)	700	WDG [1)]
h'f2	White Drive Blue (0...1023)	700	WDB [1)]
h'f9	Internal Brightness, Picture (0...511)	256	IBR
h'fc	Internal Brightness, Measurement (0...511)	384	IBRM
h'fa	Analog Brightness for external RGB (0...511)	256	ABR
h'fb	Analog Contrast for external RGB (0...511)	350	ACT

FP Sub address	Function	Default	Name
FP Display Control Register, BCL			
h'd4	BCL threshold current, 0..2047 (max ADC output ~1152)	1000	BCLTHR
h'd2	BCL time constant. 0..15 —> 0.5 .. 100msec	15	BCLTM
h'd3	BCL loop gain. 0..1023. Bit 11 must be always set to 1.	0	BCLG
h'd5	BCL minimum contrast. 0..1023	307	BCLMIN
h'75	Test register for BCL/EHT comp. function, register value: 1 stop ADC offset compensation x>1 use x in place of input from Measurement ADC	0	BCLTST
FP Display Control Register, Deflection			
h'73	interlace offset, –2048..2047 this value is added to the SAWTOOTH output during one field	0	INTLC
h'72	discharge sample count for deflection retrace, SAWTOOTH DAC output impedance is reduced for DSCC lines after vertical retrace.	7	DSCC
h'8f	vertical discharge value, SAWTOOTH output value during discharge operation, typically same as A0 init value for sawtooth	–1365	DSCV
h'7b	EHT (electronic high tension) compensation coefficient. 0..1023	0	EHT
h'7a	EHT time constant. 0..15 —> 0.5 .. 100msec	15	EHTTM
FP Display Control Register, Vertical Sawtooth			
h'80	DC offset of SAWTOOTH output, this offset is independent of EHT compensation.	0	OFS
h'8b	accu0 init value	–1365	A0
h'8c	accu1 init value	900	A1
h'8d	accu2 init value	0	A2
h'8e	accu3 init value	0	A3
FP Display Control Register, East–West Parabola			
h'9b	accu0 init value	–1121	A0
h'9c	accu1 init value	219	A1
h'9d	accu2 init value	479	A2
h'9e	accu3 init value	–1416	A3
h'9f	accu4 init value	1052	A4

[1)] The white drive values will become active only after writing the blue value WDB, latching of new values is indicated by setting the MSB of WDB.

Table 3–3: Tables for the Calculation of Initialization values for Vertical Sawtooth and East–West Parabola

Vertical Deflection 50 Hz				
	a	b	c	d
a0	1	–1365.3	+682.7	–682.7
a1		899.6	–904.3	+1363.4
a2			296.4	898.4
a3				585.9

Vertical Deflection 60 Hz				
	a	b	c	d
a0	1	–1365.3	682.7	–682.7
a1		1083.5	–1090.2	1645.5
a2			429.9	–1305.8
a3				1023.5

East–West Deflection 50 Hz					
	a	b	c	d	e
a0	1	–341.3	1365.3	–85.3	341.3
a1		111.9	–899.6	84.8	–454.5
a2			586.8	111.1	898.3
a3				72.1	–1171.7
a4					756.5

East–West Deflection 60 Hz					
	a	b	c	d	e
a0	1	–341.3	1365.3	–85.3	341.3
a1		134.6	–1083.5	102.2	–548.5
a2			849.3	–161.2	1305.5
a3				125.6	–2046.6
a4					1584.8

4. Specifications

4.1. Outline Dimensions

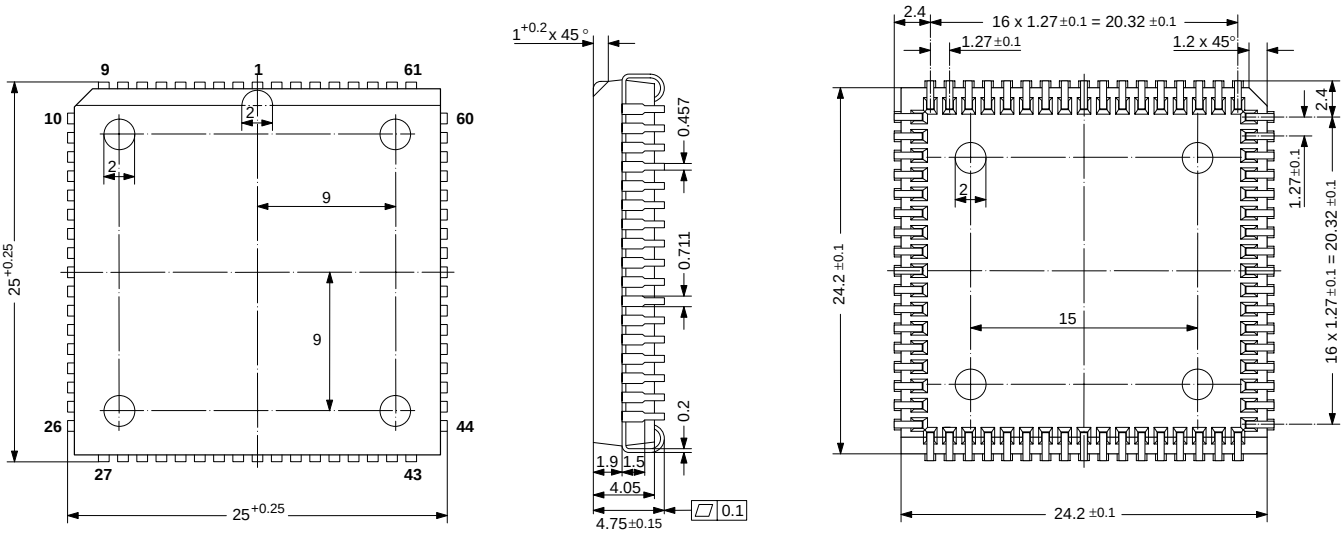


Fig. 4–1: VDP 3108 in 68-pin PLCC package
Weight approx. 4.8 g Dimensions in mm

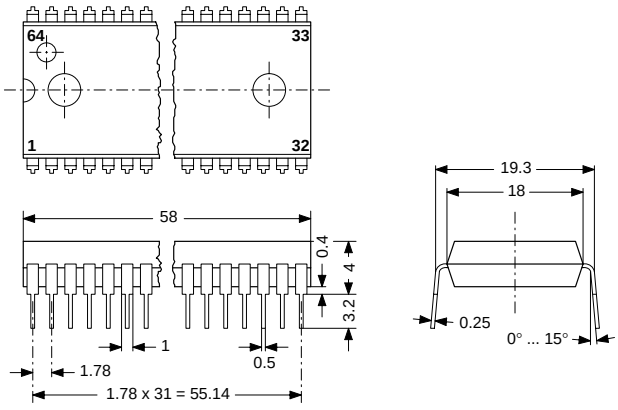


Fig. 4–2: VDP 3108 in 64-Pin S-DIL Plastic Package
Weight approx. 9.0 g Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram

Pin No. PLCC 68-pin	Pin No. SDIL 64-pin	Connection (if not used)	Pin Name	Type	Short Description
1	32	LV	MSY		Main Sync
2	31	X	$\overline{RES}$		Reset Input
3	30	GND_D	TEST		Test Pin

Pin No. PLCC 68-pin	Pin No. SDIL 64-pin	Connection (if not used)	Pin Name	Type	Short Description
4	29	LV	CSY		Composite Sync Output
5	–	GND_D	Y7		Picture Bus Luma (MSB)
6	–	GND_D	Y6		Picture Bus Luma
7	–	GND_D	Y5		Picture Bus Luma
8	28	X	V_{STBY}		Stand-By Supply Voltage
9	27	X	HOUT		Horizontal Drive Output
10	23	LV	CLK5		5 MHz Clock
11	–	GND_D	Y4		Picture Bus Luma
12	–	GND_D	Y3		Picture Bus Luma
13	21	GND_D	Y2		Picture Bus Luma
14	20	GND_D	Y1		Picture Bus Luma
15	19	GND_D	Y0		Picture Bus Luma (LSB)
16	18	X	GND_D		Ground, Digital Circuitry
17	17	X	XTAL2		Crystal (out)
18	16	X	XTAL1		Crystal (in)
19	15	X	V_{SUPD}		Supply Voltage, Digital Circuitry
20	14	X	SDA		I^2C Bus Data
21	13	GND_D	C0		Picture Bus Chroma (LSB)
22	12	GND_D	C1		Picture Bus Chroma
23	–	GND_D	C2		Picture Bus Chroma
24	–	GND_D	C3		Picture Bus Chroma
25	–	GND_D	C4		Picture Bus Chroma
26	10	X	SCL		I^2C Bus Clock
27	–	GND_D	C5		Picture Bus Chroma
28	–	GND_D	C6		Picture Bus Chroma
29	–	GND_D	C7		Picture Bus Chroma (MSB)
30	4	GND_D	PR0		Picture Bus Priority (LSB)
31	3	GND_D	PR1		Picture Bus Priority
32	2	GND_D	PR2		Picture Bus Priority (MSB)
–	1	X	VSUB		Substrate
33	6	LV	VERT		Vertical Sawtooth Output

Pin No. PLCC 68-pin	Pin No. SDIL 64-pin	Connection (if not used)	Pin Name	Type	Short Description
34	64	GND_O	RIN		Analog Red Input
35	5	LV	EW		Vertical Parabola
36	63	GND_O	GIN		Analog Green Input
37	62	X	VRD/BCS		DAC Reference/Beam Current Safety
38	61	GND_O	BIN		Analog Blue Input
39	60	X	V_{SUPO}		Supply Voltage, Analog Backend
40	59	V_{SUPO}	ROUT		Analog Output Red
41	58	X	GND_O		Ground, Analog Backend
42	57	V_{SUPO}	GOUT		Analog Output Green
43	56	GND_O	FBLIN		Fast Blank Input
44	55	V_{SUPO}	BOUT		Analog Output Blue
45	54	GND_D	NC		Not connected
46	53	GND_O	SENSE		Sense ADC Input
47	52	X	GND_O		Ground, Analog Backend
48	51	GND_O	RSW		Range Switch for Measurement ADC
49	50	GND_O	RSW2		Range Switch2 for Measurement ADC
50	49	X	GND_O		Ground, Analog Backend
51	48	GND_D	NC		Not connected
52	–	GND_D	NC		Not connected
53	–	GND_D	NC		Not connected
54	47	X	V_{SUPB}		Supply Voltage, CLK20 Buffer
55	46	LV	CLK20		20 MHz System Clock Output
56	45	X	V_{SUPF}		Supply Voltage, Analog Frontend
57	44	VRT	CIN		Chroma/Video 4 Analog Input
58	43	X	GND_F		Ground, Analog Frontend
59	42	VRT	VIN1		Video 1 Analog Input
60	–	X	$VSUB/GND_B$		Substrate/Ground CLK20 Buffer
–	41	X	GND_B		Ground CLK20 Buffer
61	40	VRT	VIN2		Video 2 Analog Input
62	39	X	VRT		Reference Voltage Top
63	38	VRT	VIN3		Video 3 Analog Input

Pin No. PLCC 68-pin	Pin No. SDIL 64-pin	Connection (if not used)	Pin Name	Type	Short Description
64	37	GND_F	ISGND		Signal Ground for Analog Input
65	36	H_{OUT}	HFLB		Horizontal Flyback Input
66	35	GND_O	SAFETY		Safety Input
67	34	GND_O	VPROT		Vertical Protection Input
68	33	LV	FSY		Front Sync

4.3. Pin Descriptions (pin numbers for 68–PLCC)

Pin 1 – Main Sync Pulse MSY (Fig. 4–8)
This pin supplies the main sync information.

Pin 2 – Reset Input RES (Fig. 4–5)
A low level on this pin resets the VDP3108.

Pin 3 – Test Input TEST (Fig. 4–5)
This pin enables factory test modes. For normal operation it must be connected to ground.

Pin 4 – Composite Sync Output CSY (Fig. 4–6)
This output supplies a standard composite sync signal that is compatible to the analog RGB output signals.

Pin 5–7, 11–15 Picture Bus Luma L7 – L0 (Fig. 4–8)
The Picture Bus Luma lines carry the digital luminance data. The data are sampled at 20.25 MHz.
In 5-bit RGB mode the 3 LSB L0,L1,L2 are the 1-bit R,G,B color signals.

Pin 8 – Standby Supply Voltage V_{STDBY}
In standby mode, only the clock oscillator and the horizontal drive circuitry are active.

Pin 9 – Horizontal Drive HOUT (Fig. 4–9)
This open drain output supplies the the drive pulse for the horizontal output stage. The polarity and gating with the flyback pulse are selectable by software.

Pin 10 – CCU 5 MHz Clock Output Clk5 (Fig. 4–6)
This pin provides a clock frequency for the TV microcontroller, e.g. a CCU3000 controller.

Pin 16 – Ground, Digital Circuitry GND_D

Pin 17,18 – XTAL1 Crystal Input and XTAL2 Crystal Output (Fig. 4–10)
These pins are connected to an 20.25 MHz crystal oscillator is digitally tuned by integrated shunt capacitances. The Clk20 and Clk5 clock signals are derived from this oscillator. An external clock can be fed into XTAL1. In this case clock frequency adjustment must be switched off.

Pin 19 – Supply Voltage, Digital Circuitry V_{SUPD}

Pin 20 – I^2C Data SDA (Fig. 4–18)
This pin connects to the I^2C bus data line.

Pin 21–25, 27–29 – Picture Bus Chroma C0–C7 (Fig. 4–8)
The Picture Bus Chroma lines carry the digital UV chrominance data. The data are sampled at 10.125 MHz and multiplexed. The UV multiplex is reset for each TV line.

In 5-bit RGB mode the two LSB UV0,UV1 are the C0,C1 bits of the 5-bit RGB signal. If C1 is 0 the RGB signals are displayed in half contrast mode; if C1 is 1 the 4 bits C0, R, G, B address one of the 16 entries of the color map.

Pin 26 – I^2C Clock SCL (Fig. 4–18)
This pin connects to the I^2C bus clock line.

Pin 30–32 – Picture Bus Priority PR0–PR2 (Fig. 4–8)
The Picture Bus Priority lines carry the digital priority selection signals. The priority interface allows digital switching of up to 8 sources to the backend processor. Switching for different sources is prioritized and can be on a per pixel basis.

Pin 33 – Vertical Sawtooth Output VERT (Fig. 4–11)
This pin supplies the drive signal for the vertical output stage. The drive signal is generated with 15-bit precision by the internal Fast Processor. The analog voltage is generated with a 4 bit R-DAC and uses digital noise shaping.

Pin 34,36,38 – Analog RGB Input RIN, GIN, BIN (Fig. 4–12)
These pins are used to insert an external analog RGB signal, e.g. from a SCART connector, to the analog RGB outputs. The analog backend provides separate brightness and contrast settings for the external analog RGB signals.

Pin 35 – East–West Parabola Output EW (Fig. 4–11)
This pin supplies the parabola signal for the East-West correction. The drive signal is generated with 15 bit precision by the internal Fast Processor. The analog volt-

age is generated by a 4 bit R-DAC and uses digital noise shaping.

Pin 37 – DAC Reference Decoupling/Beam Current Safety VRD/BCS (Fig. 4–13)
Via this pin the DAC reference voltage is decoupled by an external capacitance. The DAC output currents depend on this voltage, therefore a pulldown transistor can be used to shut off all beam currents. A decoupling capacitor of 3.3µF//100nF is required.

Pin 39 – Supply Voltage, Analog Backend V_{SUPO}

Pin 40, 42, 44 – Analog RGB Output ROUT, GOUT, BOUT (Fig. 4–14)
This are the analog Red/Green/Blue outputs of the backend. The outputs sink a current of max. 8mA.

Pin 41, 47, 50 – Ground, Analog Backend GND_O

Pin 43 – Fast Blank Input FBLIN (Fig. 4–12)
This pin is used to switch the RGB outputs to the external analog RGB inputs.

Pin 45, 51–53 – not connected

Pin 46 – Measurement ADC Input SENSE (Fig. 4–12)
This is the input of the analog digital converter for the picture and tube measurement.

Pin 48,49 – Range Switch for Meas. ADC, RSW, RSW2 (Fig. 4–9)
These pins are open drain pulldown outputs. RSW is switched off during cutoff and whitedrive measurement. RSW2 is switched off during cutoff measurement only.

Pin 54, 60 – Supply Voltage, Clk20 Output V_{SUPB}, Ground Clk20 Output GND_B.

Pin 55 – Main Clock Output Clk20 (Fig. 4–7)
This is the 20.25 main system clock, that is used by all circuits in a high-end VDP system. All external timing is derived from this clock.

Pin 56 – Supply Voltage, Analog Frontend V_{SUPI}

Pin 57 – Chroma Input CIN (Fig. 4–15)
This pin is connected to the S-VHS chroma signal. A resistive divider is used to bias the input signal to the middle of the converter input range. CIN can only be connected to the chroma (Video 2) AD converter. The signal must be AC-coupled.

Pin 58 – Ground, Analog Frontend GND_F

Pin 59,61,63 – Video Input 1–3 VIN1,VIN2,VIN3 (Fig. 4–16)
These are the analog video inputs. A CVBS or S-VHS luma signal is converted using the luma (Video 1) AD converter. The VIN1 input can also be switched to the chroma (Video 2) ADC. The input signal must be AC-coupled.

Pin 60 – Ground, Clock 20 Buffer, GND_B

Pin 62 – Reference Voltage Top VRT (Fig. 4–17)
Via this pin, the reference voltage for the AD converters is decoupled. The pin is connected with 10 µF//47 nF to the Signal Ground Pin.

Pin 64 – Signal Ground for Analog Input ISGND
This is the high quality ground reference for the video input signals.

Pin 65 – Horizontal Flyback Input HFLB (Fig. 4–12)
This pin is connected to the horizontal flyback pulse from the horizontal deflection stage. This flyback pulse is used for synchronization of the display processor and for generation of the display clock.

Pin 66 – Safety Input SAFETY (Fig. 4–12)

Pin 67 – Vertical Protection Input VPROT (Fig. 4–12)
The vertical protection circuitry prevents the picture tube from burn-in in the event of a malfunction of the vertical deflection stage. During vertical blanking, a signal level of 2.5V is sensed. If a negative edge cannot be detected, the RGB output signals are blanked.

Pin 68 – Front Sync Pulse FSY (Fig. 4–8)
This pin supplies the front sync information.

4.4. Pin Configuration

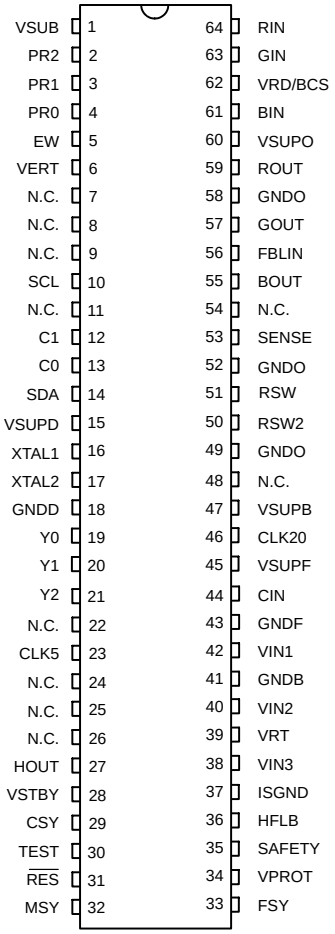


Fig. 4–3: VDP 3108 in 64-pin Shrink DIL package

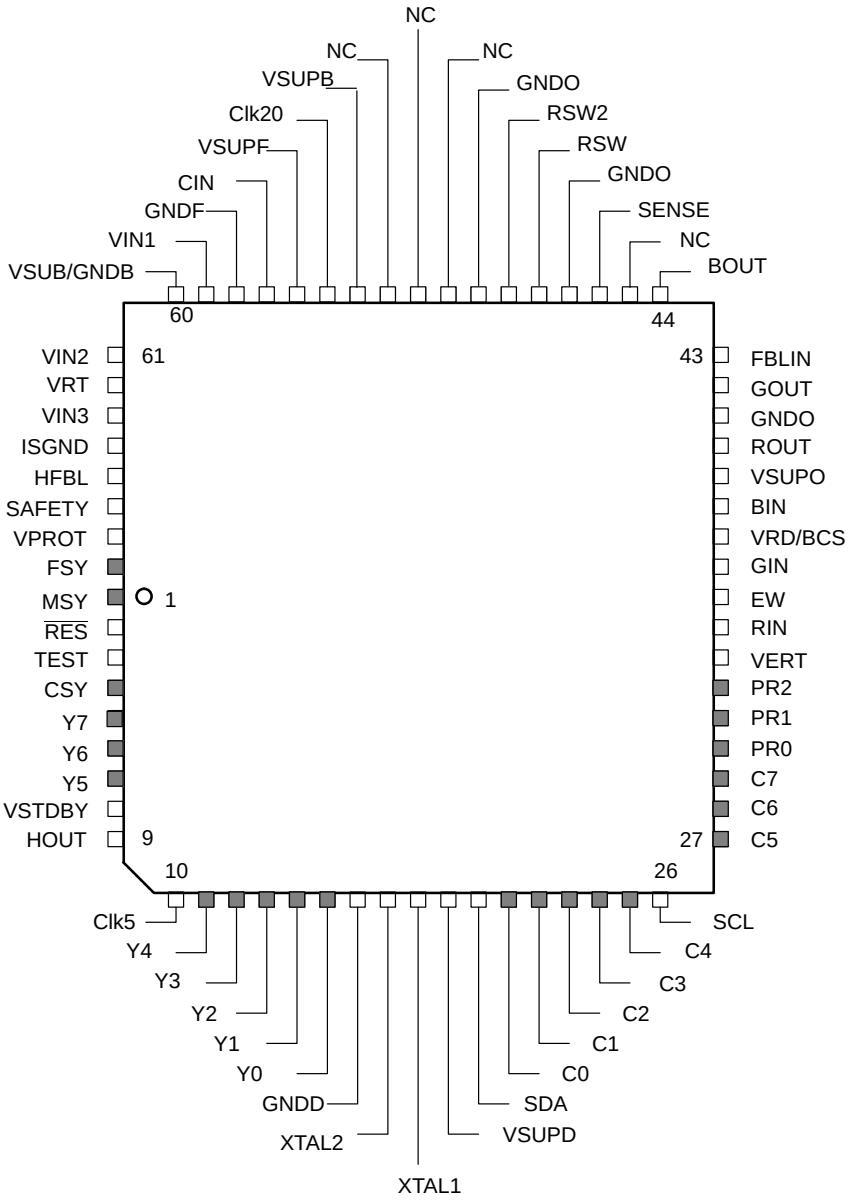


Fig. 4–4: VDP 3108 in 68-pin PLCC package

4.5. Pin Circuits

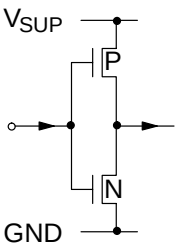


Fig. 4–5: Input pins 2, 3

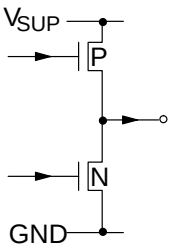


Fig. 4–6: Output pin 4, 10

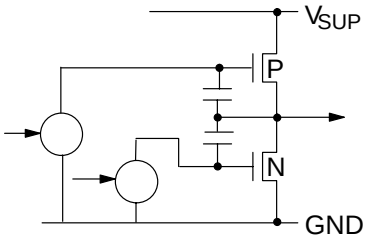


Fig. 4–7: Output pin 55

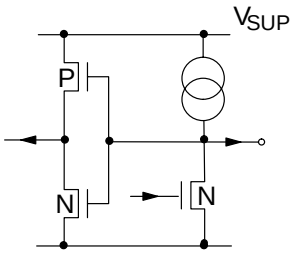


Fig. 4–8: I/O pins 1, 5, 6, 7, 11–15, 21–25, 27–32, 68

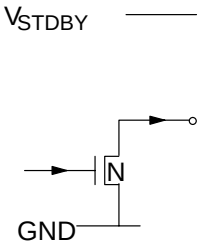


Fig. 4–9: Output pin 9, 48, 49

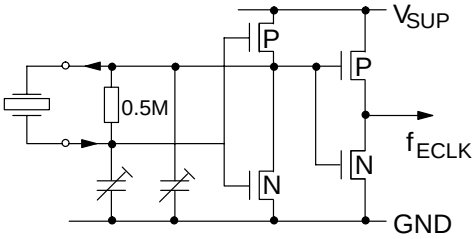


Fig. 4–10: Input pins 17, 18

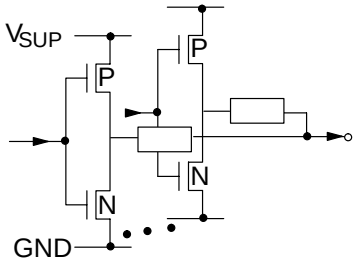


Fig. 4–11: Output pins 33, 35

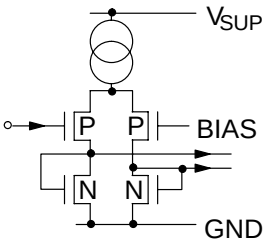


Fig. 4–12: Input pins 34, 36, 38, 65, 66, 67

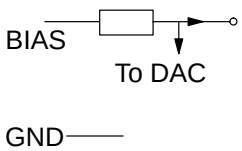


Fig. 4–13: Output pins 37

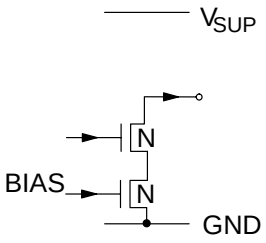


Fig. 4–14: Output pins 40, 42, 44

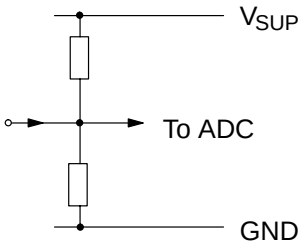


Fig. 4–15: Chroma input pin 57

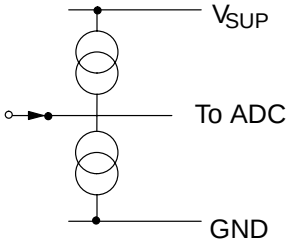


Fig. 4–16: Input pin 59, 61, 63

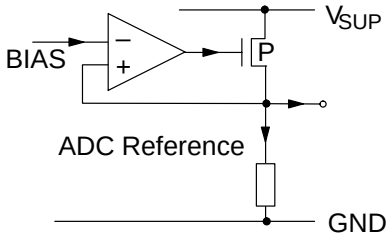


Fig. 4–17: Pin 62

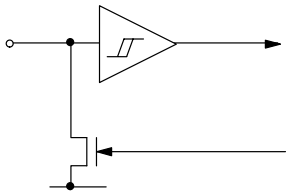


Fig. 4–18: Pins 20, 26,

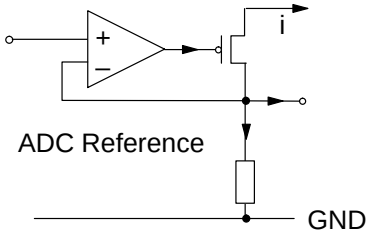


Fig. 4–19: Pin 46

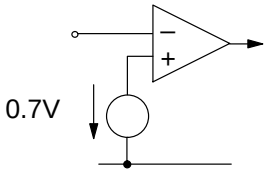


Fig. 4–20: Pin 43

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin No.	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	° C
T_S	Storage Temperature	–	–40	125	° C
V_{SUP}	Supply Voltage, all Supply Inputs		–0.3	6	V
V_I	Input Voltage, all Inputs		–0.3	V_{SUP}+0.3	V
V_O	Output Voltage, all Outputs		–0.3	V_{SUP}+0.3	V

4.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	–	65	5C
V_{SUP}	Supply Voltages, all Supply Pins		4.75	5.0	5.25	V
f_{XTAL}	Clock Frequency	XTAL1, XTAL2		20.25		MHz

4.6.3. Characteristics

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit
I_{VSUPB}	Current Consumption Backend	V_{SUPB}	58	70	85	mA
I_{VSUPF}	Current Consumption	V_{SUPF}		40		mA
I_{VSUPD}	Current Consumption	V_{SUPD}		140		mA
I_{VSUPO}	Current Consumption	V_{SUPO}		5		mA
I_{VSTDBY}	Current Consumption	V_{STDBY}		3		mA
P_{TOT}	Total Power Dissipation			1.3		W

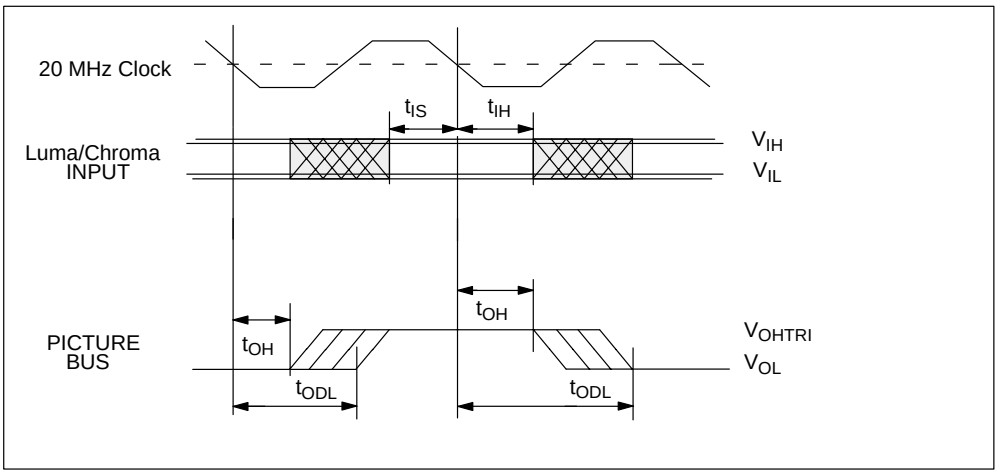
4.6.4. Recommended Crystal Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Ambient Temperature	0	–	65	° C
f_P	Parallel Resonance Frequency with Load Capacitance C_L=10pF	–	20.250000	–	MHz
$\Delta f_P/f_P$	Accuracy of Adjustment	–	–	+/– 20	ppm
$\Delta f_P/f_P$	Frequency Temperature Drift	–	–	+/– 30	ppm
C_0	Shunt Capacitance	3	–	6	pF

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_1	Motional Capacitance	13	–	20	fF
R_r	Series Resistance			40	W

Characteristics, Priority Bus: Luma, Chroma, Priority, FSync, MSync

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	Y[7..0] C[7..0] PR[2:0] MSY FSY	–	0.25	0.5	V	I_{OL} = 8 mA, strength 3 I_{OL} = 6 mA, strength 2 I_{OL} = 4 mA, strength 1 I_{OL} = 2 mA, strength 0
V_{OH}	Output High Voltage		1.8	2.0	–	V	$-I_{OL}$ = 10 µA C_{LOAD} = 71pF
t_{OH}	Output Hold Time		5	14	TBD	ns	C_{LOAD} = 71pF I_{PL} = 8.4 mA
t_{ODL}	Output Delay Time		–	–	35	ns	C_{LOAD} = 71pF I_{PL} = 8.4 mA
I_{PL}	Output Pull-up Current		1.2	1.5	1.8	mA	V_{OL} = 0V
V_{IL}	Input Low Voltage		–	–	0.8	V	
V_{IH}	Input High Voltage		1.5	–	–	V	
t_{IS}	Input Setup Time		10	–	–	ns	
t_{IH}	Input Hold Time		0	–	–	ns	



Characteristics, Combined Sync Output, 5 MHz Clock Output

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	CSY Clk5	–	–	0.4	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage		4.0	–	VSUP	V	$-I_{OL}$ = 1.6 mA
t_{OT}	Output Transition Time	Clk5	–	50		ns	C_{LOAD} = 30pF
t_{OT}	Output Transition Time	CSY	–	10	20	ns	C_{LOAD} = 30pF

Characteristics, Horizontal Drive Output

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	HOUT	–	–	0.4	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (Open Drain Stage)		–	–	8	V	external pull-up resistor
t_{OF}	Output Fall Time		–	8	20	ns	C_{LOAD} = 30pF

Characteristics, Reset Input, Test Input

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	$\overline{\text{RES}}$ TEST	–	–	2.0	V	
V_{IH}	Input High Voltage		3.1	–	–	V	

Characteristics, 20 MHz Clock Input/Output, External Clock Input (XTAL1), V_R = (spec value/V_{SUP}) x 5V

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{DCAV}	DC Average	Clk20	$V_R/2$ – 0.3	$V_R/2$	$V_R/2$ + 0.3	V	C_{LOAD} = 30pF
V_{PP}	V_{OUT} Peak to Peak		1.3	1.6	–	V_R	C_{LOAD} = 30pF
t_{OT}	Output Transition Time		–	–	18	ns	C_{LOAD} = 30pF
V_{IT}	Input Trigger Level		2.1	2.5	2.9	V	only for test purposes
V_I	Clock Input Voltage	XTAL 1	1.3	–	–	V_{PP}	capacitive coupling used XTAL2 open

Characteristics, I²C Bus Interface

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	SDA, SCL	–	–	1.5	V	
V_{IH}	Input High Voltage		3.0	–	–	V	
V_{OL}	Output Low Voltage		–	–	0.4 0.6	V V	I_I = 3mA I_I = 6mA
V_{IH}	Input Capacitance		–	–	TBD	pF	
II	Input Leakage Current		–1	–	1	µA	
t_F	Signal Fall Time		–	–	300	ns	C_L = 400 pF
t_R	Signal Rise Time		–	–	300	ns	C_L = 400 pF
f_{SCL}	Clock Frequency	SCL	0	–	400	kHz	
t_{LOW}	Low Period of SCL			–	–	ns	
t_{HIGH}	High Period of SCL			–	–	ns	
$t_{SU\ Data}$	Data Set Up Time to SCL high	SDA		–	–	ns	
$t_{HD\ Data}$	DATA Hold Time to SCL low		0	–	–	ns	

Characteristics, Sense ADC Input

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_I	Input Voltage Range	SENSE	0	–	V_{sup}	V	
V_{I255}	Input Voltage for code 255 output		1.4	1.54	1.7	V	read cutoff blue register
C_0	Digital Output for 0 Input				16	LSB	offset check, read cutoff blue register
R_I	Input Impedance		1	–	–	MΩ	

Characteristics, Range Switch Outputs

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
R_{ON}	Output On Resistance	RSW RSW2	–	–	50	W	I_{OL} = 10 mA
I_{Max}	Maximum Current		–	–	15	mA	
I_{LEAK}	Leakage Current		–	–	600	nA	RSW High Impedance
C_{IN}	Input Capacitance		–	–		pF	

Characteristics, Horizontal Flyback Input

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	HFLB	–	–	1.8	V	
V_{IH}	Input High Voltage		2.6	–	–	V	
V_{IHST}	Input Hysteresis		0.1	–	–	V	
$PSRR_{HF}$	Power Supply Rejection Ratio of Trigger Level		0			dB	F = 20 MHz
$PSRR_{MF}$	Power Supply Rejection Ratio of Trigger Level		–20			dB	F < 15 kHz
$PSRR_{LF}$	Power Supply Rejection Ratio of Trigger Level		–40			dB	F < 100 Hz
t_{PID}	Internal Delay				12	ns	slew rate 500mV / ns swing $1V_{PP}$

Characteristics, Vertical Protection Input

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	VPROT	–	–	1.8	V	
V_{IH}	Input High Voltage		2.6	–	–	V	
V_{IHST}	Input Hysteresis		0.1	–	–	V	

Characteristics, Vertical Safety Input

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{ILA}	Input Low Voltage	SAFE-TY	–	–	1.8	V	
V_{IHA}	Input High Voltage		2.6	–	–	V	
V_{ILA}	Input Low Voltage		–	–	3.1	V	
V_{IHA}	Input High Voltage		3.9	–	–	V	
V_{IHST}	Input Hysteresis A and B		0.1	–	–	V	
t_{PID}	Internal Delay				100	ns	

Characteristics, Vertical, East–West Drive Output

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_O	Output Voltage Range	EW VERT	0.1		4.9	V	
PSSR	Power Supply Rejection Ratio			0		dB	
R^{dacn}	R–DAC Output Resistance		1.0	1.25	1.7	kΩ	
R_{dacd}	R–DAC Output Resistance discharge		0.47	0.65	0.8	kΩ	

Characteristics, DAC Reference, BEAM Current Safety Output

at T_A = 0 to 65 °C, V_{SUPO} = 4.75 to 5.25 V, f = 20.25 MHz for min./max.–values
at T_C = 60 °C, V_{SUPO} = 5 V, f = 20.25 MHz for typical values

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{DACREF}	DAC–Ref. Voltage	VRD/ BCS	2.38	2.52	2.67	V	
	DAC–Ref.–Output resistance	VRD/ BCS	18	25	32	kΩ	

Characteristics, R,G,B D/A Converters, External Analog RGB Voltage/Current DA Converters
at T_A = 0 to 65 °C, V_{SUPO} = 4.75 to 5.25 V, f = 20.25 MHz for min./max.–values
at T_C = 60 °C, V_{SUPO} = 5 V, f = 20.25 MHz for typical values

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
	RGB–DACs Resolution			10		bits	
I_{OUT}	Full Scale Output Current	ROUT, GOUT, BOUT	3.1	3.75	4.5	mA	
I_{OUT}	Differential Nonlinearity				0.5	LSB	
I_{OUT}	Integral Nonlinearity				1	LSB	
I_{OUT}	Glitch Pulse			0.5		pAsec	Ramp, line is terminated on both ends with 50Ohms
I_{OUT}	Rise and Fall Time			3		nsec	10% to 90%, 90% to 10%
I_{OUT}	Intermodulation				–50	dB	2/2.5MHz Full Scale
I_{OUT}	Signal to Noise		+50			dB	Signal: 1MHz Full Scale Bandwidth: 10MHz
I_{OUT}	Match R–G, R–B, G–B		–2		2	%	
	R/B/G Crosstalk one channel talks two channels talk				–46	dB	passive channel I_{OUT} =1.88mA Crosstalk–Signal: 1.25MHz 3.75mApp
	RGB Input Crosstalk from external RGB one channel talks two channels talk three channels talk				–50	dB	passive channel I_{OUT} =1.88mA Crosstalk–Signal: 1.25MHz 3.75mApp

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
	Brightness–DACs Resolution			9		bits	
I_{BR}	Full Scale Output Current	ROUT, GOUT, BOUT	39.2	40	40.8	%	ref to max. digital RGB
I_{BR}	Full Scale Output Current typical			1.5		mA_{pp}	
I_{BR}	differential nonlinearity				0.5	LSB	
I_{BR}	integral nonlinearity				1	LSB	
I_{BR}	Match R–G, R–B, G–B		–2		2	%	
I_{BR}	Match to digital RGB R–R, G–G, B–B		–2		2	%	
	Cutoff–DACs Resolution			9		bits	
I_{CUT}	Full Scale Output Current	ROUT, GOUT, BOUT	58.8	60	61.2	%	ref to max. digital RGB
I_{CUT}	Full Scale Output Current typical			2.25		mA_{pp}	
I_{CUT}	differential nonlinearity				0.5	LSB	
I_{CUT}	integral nonlinearity				1	LSB	
I_{CUT}	Match to digital RGB R–R, G–G, B–B		–2		2	%	
	Ultrablack–DACs Resolution			1		bits	
I_{UB}	Full Scale Output Current	ROUT, GOUT, BOUT	19.6	20	20.4	%	ref to max. digital RGB
	Full Scale Output Current typical			0.75		mA	
	Match to digital RGB R–R, G–G, B–B		–2		2	%	

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
	Ext. RGB Brightn. DACs Resolution			9		bits	
I_{EXBR}	Full Scale Output Current of Ex. Brightness DACs	ROUT, GOUT, BOUT	39.2	40	40.8	%	ref to max. Digital RGB
	Full Scale Output Current of Ex. Brightness DACs typical			1.5		mA	
	differential nonlinearity				0.5	LSB	
	integral nonlinearity				1	LSB	
	Match R–G, R–B, G–B		–2		2	%	
	Match to digital RGB R–R, G–G, B–B		–2		2	%	
	Ext. RGB V/I–DACs Resolution			9		bits	
I_{EXOUT}	Full Scale Output Current	ROUT GOUT BOUT	96	100	104	%	ref to max. Digital RGB V_{IN}=0.7 contrast = 323
	Full Scale Output Current typical			3.75		mA	same as Digital RGB
CR	Contrast adjust Range			16:511			
	Gain Match R–G, R–B, G–B		–2		2	%	measured at RGB Outputs V_{IN} = 0.7 V Contrast=323
	Gain Match to RGB–DACs R–R, G–G, B–B		–4		4	%	
	R/B/G Input Crosstalk one channel talks two channels talk	ROUT GOUT BOUT			–46	dB	passive channel: V_{IN} = 0.7V contrast =323. Crosstalk Signal: 1.25MHz 3.75mApp
	RGB Input Crosstalk from internal RGB one channel talks two channels talk tree channels talk	ROUT GOUT BOUT			–50	dB	

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
	RGB Input Noise & Distortion	ROUT GOUT BOUT			–50	dB	V_{IN}=0.7Vpp 1MHz contrast = 323 Bandwidth: 10MHz
	RGB Input Bandwidth –3dB		10	15	–	MHz	V_{IN} = 0.7Vpp contrast =323
	RGB Input THD		–50 –40			dB dB	Input signal 1 MHz Input signal 6 MHz V_{IN} = 0.7Vpp contrast =323
	differential nonlinearity of Contrast Adjust				1.0	LSB	V_{IN} = 0.44V
	integral nonlinearity of Contrast Adjust				7	LSB	
V_{RGBO}	R,G,B Output Voltage	ROUT GOUT BOUT	–1.0		0.3	V	referred to $VSUP_O$
	R,G,B Output Load Resistance				100	W	to $VSUP_O$
V_{OUTC}	RGB Output Compliance		–1.5	–1.3	–1.2	V	ref. to $VSUP_o$ Sum of max. Current of RGB–DACs and max. Current of Int.Brightness DACs is 2% degraded
	Ext. RGB Inputs						
V_{RGBIN}	External RGB Inputs Voltage Range	RIN, GIN, BIN	–0.3	–	1.1	V	
V_{RGBIN}	nominal RGB Input Voltage peak/peak		0.5	0.7	1.0	V_{PP}	SCART Spec: 0.7V ±3dB
V_{RGBIN}	RGB Inputs Voltage for maximum Output Current			0.44			contrast setting: 511
	RGB Inputs Voltage for maximum Output Current			0.7			contrast setting: 323
	RGB Inputs Voltage for maximum Output Current			1.1			contrast setting: 204

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
C_{RGBIN}	External RGB Input Coupling Capacitor	RIN, GIN, BIN		15		nF	
	Clamp Pulse Width		3.1			µsec	
C_{IN}	Input Capacitance		–	–	13	pF	
I_{IL}	Input Leakage Current		–0.5	–	0.5	µA	clamping OFF, V_{IN} –0.3..3V
V_{CLIP}	RGB Input Voltage for Clipping Current			2		V	
V_{CLAMP}	Clamp Level at Input		40	60	80	mV	clamping ON
V_{INOFF}	Offset Level at Input		–10		10	mV	extrapolated from V_{IN}= 100mV and 200mV
V_{INOFF}	Offset Level Match at Input		–10		10	mV	extrapolated from V_{IN}= 100mV and 200mV
R_{CLAMP}	Clamping On–Resistance				–	W	

Characteristics, Fast Blank Input

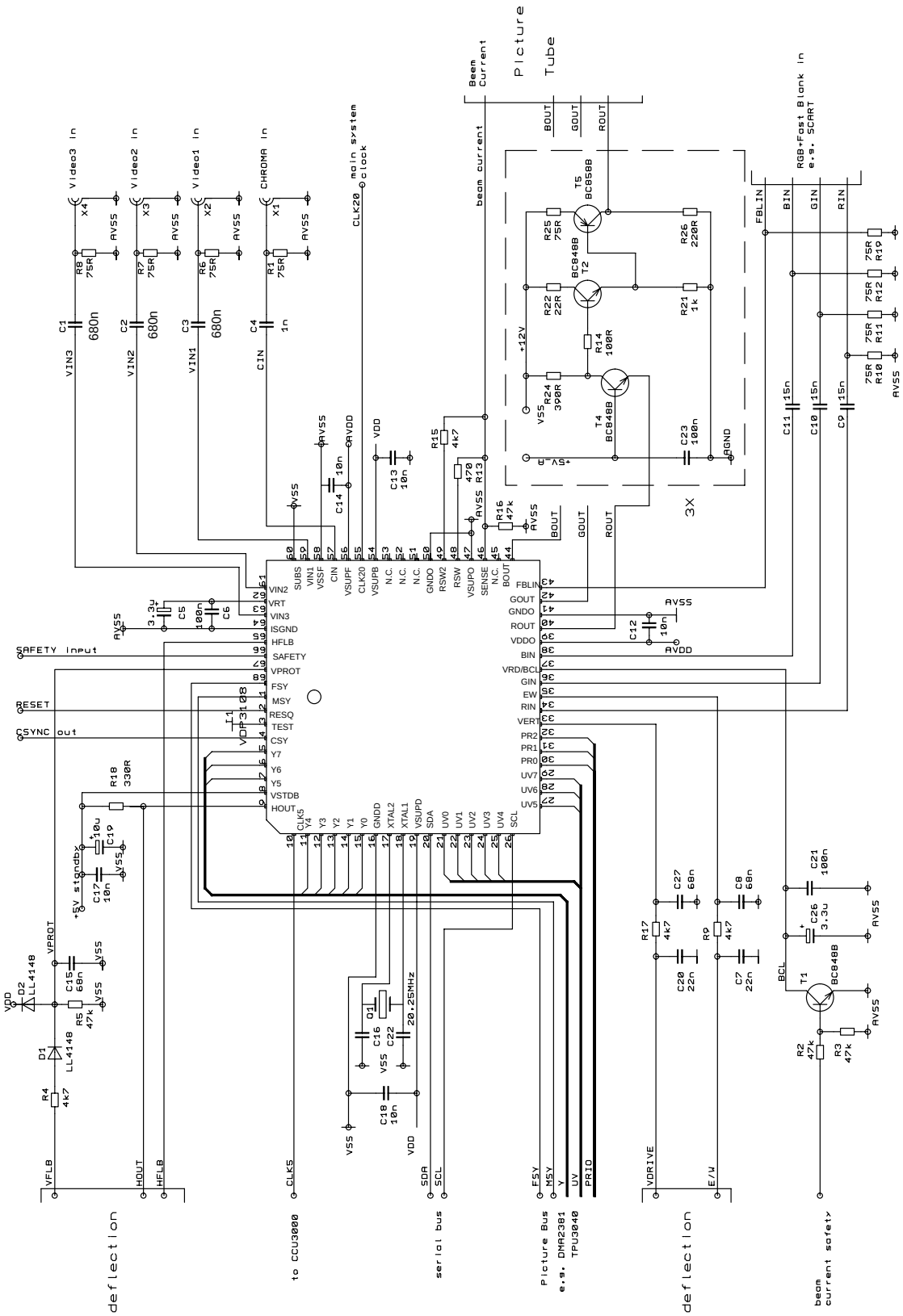
Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{FBLOFF}	FBLIN Low Level	FBLIN	–	–	0.5	V	
V_{FBLON}	FBLIN High Level		0.9	–	–	V	
$V_{FBLTRIG}$	Fast Blanking Trigger Level typical			0.7			
t_{PID}	Delay Fast Blanking to RGB_{OUT} from midst of FBLIN–transition to 90% of RGB_{OUT}– transition			8	15	ns	Int. RGB = 3.75mA Full Scale Int. Brightness = 0 ext. Brightness = 1.5mA (Full Scale) RGBin = 0 V_{FBLOFF}=0.4V V_{FBLON}=1.0V rise and fall time = 2ns
	Difference of Internal Delay to ext. RGBin Delay		–5		+5	ns	
	Switch–over–Glitch			0.5		pAsec	switch from 3.75mA (int) to 1.5mA (ext)

Characteristics, Analog Video Inputs

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{VIN}	Analog Input Voltage	VIN1 VIN2 VIN3 CIN	0		2.5	V	
C_{IN}	Input Capacitance				13	pF	V_{IN} = 1.5 V
C_{CP}	Input Coupling Capacitor Video Inputs	VIN1 VIN2 VIN3		680		nF	
C_{CP}	Input Coupling Capacitor Chroma Input	CIN		1		nF	

Characteristics, Analog Frontend and ADCs

Symbol	Parameter	Pin No.	Min.	Typ.	Max.	Unit	Test Conditions
V_{VIN}	Full Scale Input Voltage, Video 1	VIN1, VIN2, VIN3	1.8	2.0	2.2	V_{PP}	min. AGC Gain
V_{VIN}	Full Scale Input Voltage, Video 1		0.5	0.6	0.7	V_{PP}	max. AGC Gain
V_{VINCL}	Video 1 Input Clamping Level, CVBS			1.0		V	Binary Level = 68 LSB min. AGC Gain
V_{CIN}	Full Scale Input Voltage, Chroma	CIN, VIN1	1.08	1.2	1.32	V_{PP}	
V_{VINCL}	Video 2 Input Clamping Level, CVBS			1.2		V	Binary Level = 68 LSB
V_{CINB}	Video 2 Input Bias Level, SVHS Chroma		–	1.5	–	V	
R_{CIN}	Video 2 Input Resistance SVHS Chroma		1.6	2	2.4	kΩ	
	Binary Code for Open Chroma Input	VIN1 CIN		128			
Q_{CL}	Input Clamping Current resolution	VIN1–3, CIN	–16		15	steps	
I_{CL}	Input Clamping Current per step		0.7	1	1.3	µA	
V_{VRT}	Reference Voltage Top	VRT	2.5	2.6	2.8	V	10µF//10nF, 1GΩ Probe
	Video 1 Bandwidth			10		MHz	–3dB for full scale signal
	Video 2 Bandwidth			10		MHz	–3dB for full scale signal
	Crosstalk, any Two Video Inputs			–50		dB	at 1 MHz
THD	Distortion			–45	–42	dB	at 1 MHz, 5th harmonics
	Video Signal to Noise & Distortion	VIN1–3, CIN	41			dB	at 1 MHz
	Video Integral Non-Linearity, static	VIN1–3, CIN			± 1	LSB	Code Density
	Video Differential Non-Linearity,	VIN1–3, CIN			± 0.5	LSB	Code Density
	Video Differential Gain	VIN1–3, CIN			± 3	%	300 mV_{PP}, 4.4 MHz on ramp
	Video Differential Phase	VIN1–3, CIN		TBD		5	300 mV_{PP}, 4.4 MHz on ramp


Video3 In
Video2 In
Video1 In
CHROMA In
main system clock
Beam Current
Picture Tube
RGB+Fast Blank In
e.g. SCART
SAFETY Input
RESET
CSYNC out
VDP3108
deflection
to CCU3000
serial bus
Picture Bus
e.g. DNA2381
TPU3040
deflection
beam current safety

5. Data Sheet History

1. Advance Information: “VDP 3108 Single-Chip Video Processor”, Edition Feb. 7, 1994, 6251-352-1AI.
First release of the Advance Information.

2. Advance Information: “VDP 3108 Single-Chip Video Processor”, Edition May 3, 1994, 6251-352-2AI.
Second release of the Advance Information.

3. Advance Information: “VDP 3108 Single-Chip Video Processor”, Edition Oct. 12, 1994, 6251-352-3AI.
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