

# SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B SN65LVDT3486B, SN65LVDS9637B, SN65LVDT9637B HIGH-SPEED DIFFERENTIAL RECEIVERS

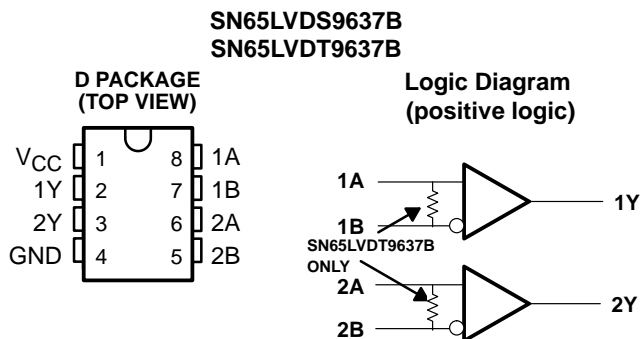
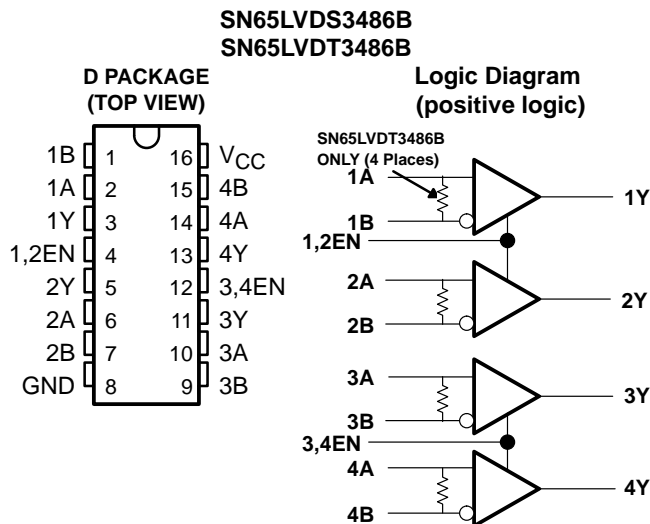
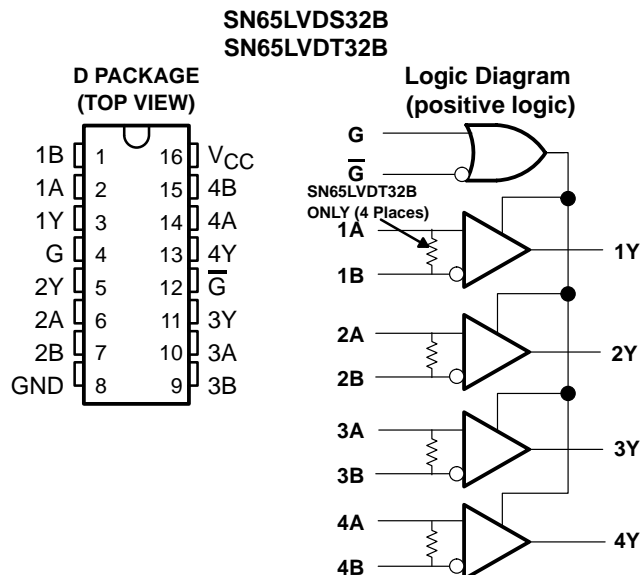
SLLS440A – OCTOBER 2000 – REVISED MAY 2001

- Meets or Exceeds the Requirements of ANSI EIA/TIA-644 Standard for Signaling Rates† up to 400 Mbps
- Operates With a Single 3.3-V Supply
- -2-V to 4.4-V Common-Mode Input Voltage Range
- Differential Input Thresholds <50 mV With 50 mV of Hysteresis Over Entire Common-Mode Input Voltage Range
- Integrated 110-Ω Line Termination Resistors Offered With the LVDT Series
- Propagation Delay Times 4 ns (typ)
- Active Fail Safe Assures a High-Level Output With No Input
- Bus-Pin ESD Protection Exceeds 15 kV HBM
- Inputs Remain High-Impedance on Power Down
- Recommended Maximum Parallel Rate of 200 M-Transfers/s
- Available in Small-Outline Package With 1,27 mm Terminal Pitch
- Pin-Compatible With the AM26LS32, MC3486, or  $\mu$ A9637

## description

This family of differential line receivers offers improved performance and features that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS is defined in the TIA/EIA-644 standard. This improved performance represents the second generation of receiver products for this standard, providing a better overall solution for the cabled environment. This generation of products is an extension to TI's overall product portfolio and is not necessarily a replacement for older LVDS receivers.

Improved features include an input common-mode voltage range 2 V wider than the minimum required by the standard. This will allow longer cable lengths by tripling the allowable ground noise tolerance to 3 V between a driver and receiver. TI has additionally introduced an even wider input common-mode voltage range of -4 to 5 V in their SN65LVDS/T33 and SN65LVDS/T34.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Signaling rate, 1/t, where t is the minimum unit interval and is expressed in the units bits/s (bits per second)

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated

# SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B SN65LVDT3486B, SN65LVDS9637B, SN65LVDT9637B HIGH-SPEED DIFFERENTIAL RECEIVERS

SLLS440A – OCTOBER 2000 – REVISED MAY 2001

## description (continued)

Precise control of the differential input voltage thresholds now allows for inclusion of 50 mV of input voltage hysteresis to improve noise rejection on slowly changing input signals. The input thresholds are still no more than  $\pm 50$  mV over the full input common-mode voltage range.

The high-speed switching of LVDS signals almost always necessitates the use of a line impedance matching resistor at the receiving-end of the cable or transmission media. The SN65LVDT series of receivers eliminates this external resistor by integrating it with the receiver. The nonterminated SN65LVDS series is also available for multidrop or other termination circuits.

The receivers can withstand  $\pm 15$ -kV human-body model (HBM) and  $\pm 600$  V-machine model (MM) electrostatic discharges to the receiver input pins with respect to ground without damage. This provides reliability in cabled and other connections where potentially damaging noise is always a threat.

The receivers also include a (patent pending) fail-safe circuit that will provide a high-level output within 600 ns after loss of the input signal. The most common causes of signal loss are disconnected cables, shorted lines, or powered-down transmitters. This prevents noise from being received as valid data under these fault conditions. This feature may also be used for wired-OR bus signaling.

The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100  $\Omega$ . The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B, SN65LVDT3486B, SN65LVDS9637B, and SN65LVDT9637B are characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

### AVAILABLE OPTIONS

PART NUMBER†	NUMBER OF RECEIVERS	TERMINATION RESISTOR†	SYMBOLIZATION
SN65LVDS32BD	4	No	LVDS32B
SN65LVDT32BD	4	Yes	LVDT32B
SN65LVDS3486BD	4	No	LVDS3486
SN65LVDT3486BD	4	Yes	LVDT3486
SN65LVDS9637BD	2	No	DK637B
SN65LVDT9637BD	2	Yes	DR637B

† Add the suffix R for taped and reeled carrier.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

**SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B  
SN65LVDT3486B, SN65LVDS9637B, SN65LVDT9637B  
HIGH-SPEED DIFFERENTIAL RECEIVERS**

SLLS440A – OCTOBER 2000 – REVISED MAY 2001

**Function Tables**

**SN65LVDS32B and SN65LVDT32B**

DIFFERENTIAL INPUT	ENABLES		OUTPUT
A-B	G	$\overline{G}$	Y
$V_{ID} \geq -32 \text{ mV}$	H X	X L	H H
$-100 \text{ mV} < V_{ID} \leq -32 \text{ mV}$	H X	X L	? ?
$V_{ID} \leq -100 \text{ mV}$	H X	X L	L L
X	L	H	Z
Open	H X	X L	H H

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off), ? = indeterminate

**SN65LVDS3486B and SN65LVDT3486B**

DIFFERENTIAL INPUT	ENABLES	OUTPUT
A-B	EN	Y
$V_{ID} \geq -32 \text{ mV}$	H	H
$-100 \text{ mV} < V_{ID} \leq -32 \text{ mV}$	H	?
$V_{ID} \leq -100 \text{ mV}$	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant,  
Z = high impedance (off), ? = indeterminate

**SN65LVDS9637B and SN65LVDT9637B**

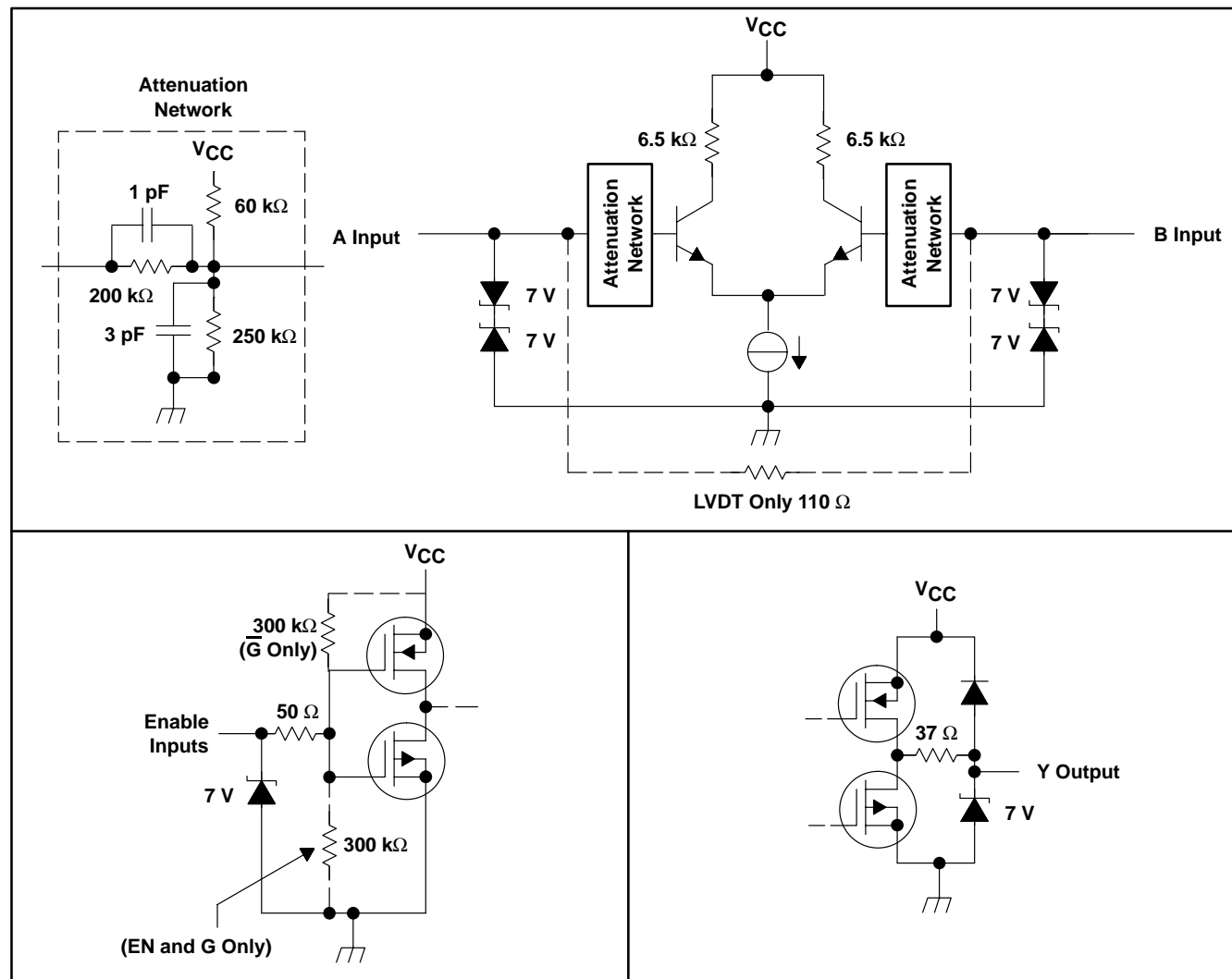
DIFFERENTIAL INPUT	OUTPUT
A-B	Y
$V_{ID} \geq -32 \text{ mV}$	H
$-100 \text{ mV} < V_{ID} \leq -32 \text{ mV}$	?
$V_{ID} \leq -100 \text{ mV}$	L
Open	H

H = high level, L = low level, ? = indeterminate

**SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B  
SN65LVDT3486B, SN65LVDS9637B, SN65LVDT9637B  
HIGH-SPEED DIFFERENTIAL RECEIVERS**

SLLS440A – OCTOBER 2000 – REVISED MAY 2001

**equivalent input and output schematic diagrams**



**SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B  
SN65LVDT3486B, SN65LVDS9637B, SN65LVDT9637B  
HIGH-SPEED DIFFERENTIAL RECEIVERS**

SLLS440A – OCTOBER 2000 – REVISED MAY 2001

**absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$ (see Note 1)	–0.5 V to 4 V
Voltage range: Enables or Y	–0.5 V to $V_{CC} + 3$ V
A or B	–4 V to 6 V
$ V_A - V_B $ (LVDT)	1 V
Electrostatic discharge: A, B, and GND (see Note 2)	Class 3, A: 15 kV, B: 600 V
Continuous power dissipation	See Dissipation Rating Table
Storage temperature range	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.  
2. Tested in accordance with MIL-STD-883C Method 3015.7.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	OPERATING FACTOR <sup>‡</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D8	725 mW	5.8 mW/°C	377 mW
D16	950 mW	7.6 mW/°C	494 mW

<sup>‡</sup> This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

**recommended operating conditions**

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		3	3.3	3.6	V
High-level input voltage, $V_{IH}$	Enables	2			V
Low-level input voltage, $V_{IL}$	Enables			0.8	V
Magnitude of differential input voltage, $ V_{ID} $	LVDS	0.1		3	V
	LVDT			0.8	V
Voltage at any bus terminal (separately or common-mode), $V_I$ or $V_{IC}$		–2		4.4	V
Operating free-air temperature, $T_A$		–40		85	°C



**SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B  
SN65LVDT3486B, SN65LVDS9637B, SN65LVDT9637B  
HIGH-SPEED DIFFERENTIAL RECEIVERS**

SLLS440A – OCTOBER 2000 – REVISED MAY 2001

**electrical characteristics over recommended operating conditions (unless otherwise noted)**

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>IT1</sub>	Positive-going differential input voltage threshold		V <sub>IB</sub> = −2 V or 4.4 V, See Figures 1 and 2			50	mV
V <sub>IT2</sub>	Negative-going differential input voltage threshold				−50		
V <sub>IT3</sub>	Differential input fail-safe voltage threshold		See Table 1 and Figure 5	−32		−100	mV
V <sub>ID(HYS)</sub>	Differential input voltage hysteresis, V <sub>IT1</sub> - V <sub>IT2</sub>				50		mV
V <sub>OH</sub>	High-level output voltage		I <sub>OH</sub> = −4 mA	2.4			V
V <sub>OL</sub>	Low-level output voltage		I <sub>OL</sub> = 4 mA			0.4	V
I <sub>CC</sub>	Supply current	'32B or '3486B	G or EN at V <sub>CC</sub> , No load, Steady-state		16	23	mA
			G or EN at GND		1.1	5	
		'9637B	No load, Steady-state		8	12	
I <sub>I</sub>	Input current (A or B inputs)	SN65LVDS	V <sub>I</sub> = 0 V, Other input open			±20	μA
			V <sub>I</sub> =2.4 V, Other input open			±20	
			V <sub>I</sub> = −2 V, Other input open			±40	
			V <sub>I</sub> = 4.4 V, Other input open			±40	
		SN65LVDT	V <sub>I</sub> = 0 V, Other input open			±40	μA
			V <sub>I</sub> =2.4 V, Other input open			±40	
			V <sub>I</sub> =−2 V, Other input open			±80	
			V <sub>I</sub> = 4.4 V, Other input open			±80	
I <sub>ID</sub>	Differential input current (I <sub>IA</sub> - I <sub>IB</sub> )	SN65LVDS	V <sub>ID</sub> = 100 mV, V <sub>IC</sub> = −2 V or 4.4 V, See Figure 1			±3	μA
		SN65LVDT	V <sub>ID</sub> = 0.2 V, V <sub>IC</sub> = −2 V or 4.4 V	1.55		2.22	mA
I <sub>I(OFF)</sub>	Power-off input current (A or B inputs)	SN65LVDS	V <sub>A</sub> or V <sub>B</sub> = 0 V or 2.4 V, V <sub>CC</sub> = 0 V			±20	μA
			V <sub>A</sub> or V <sub>B</sub> = −2 V or 4.4 V, V <sub>CC</sub> = 0 V			±35	
		SN65LVDT	V <sub>A</sub> or V <sub>B</sub> = 0 V or 2.4 V, V <sub>CC</sub> = 0 V			±30	
			V <sub>A</sub> or V <sub>B</sub> = −2 V or 4.4 V, V <sub>CC</sub> = 0 V			±50	
I <sub>IH</sub>	High-level input current (enables)		V <sub>IH</sub> = 2 V			10	μA
I <sub>IL</sub>	Low-level input current (enables)		V <sub>IL</sub> = 0.8 V			10	μA
I <sub>OZ</sub>	High-impedance output current					±10	μA
C <sub>I</sub>	Input capacitance, A or B input to GND		V <sub>I</sub> = 0.4 sin (4E6πt) + 0.5 V		5		pF

† All typical values are at 25°C and with a 3.3 V supply.



**SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B  
SN65LVDT3486B, SN65LVDS9637B, SN65LVDT9637B  
HIGH-SPEED DIFFERENTIAL RECEIVERS**

SLLS440A – OCTOBER 2000 – REVISED MAY 2001

**switching characteristics over recommended operating conditions (unless otherwise noted)**

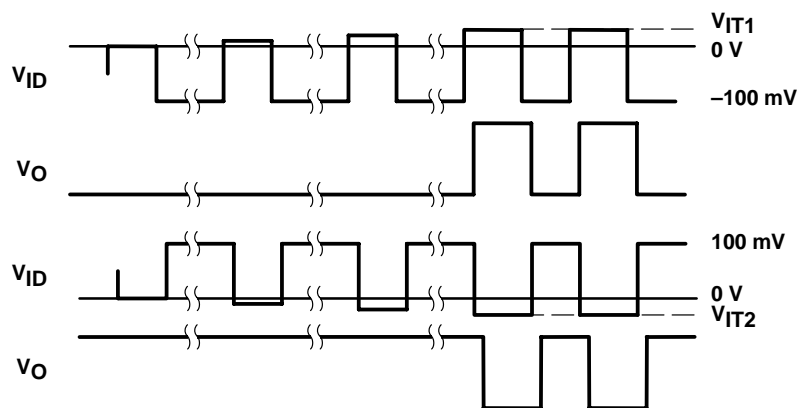
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t <sub>PLH</sub> Propagation delay time, low-to-high-level output	See Figure 3	2.5	4	6	ns
t <sub>PHL</sub> Propagation delay time, high-to-low-level output		2.5	4	6	ns
t <sub>d1</sub> Delay time, fail-safe deactivate time	See Figures 3 and 6			9	ns
t <sub>d2</sub> Delay time, fail-safe activate time		0.3		1.5	μs
t <sub>sk(p)</sub> Pulse skew ( t <sub>PHL1</sub> – t <sub>PLH1</sub>  )	C <sub>L</sub> = 10 pF, See Figure 3		200		ps
t <sub>sk(o)</sub> Output skew§			150		ps
t <sub>sk(pp)</sub> Part-to-part skew‡				1	ns
t <sub>r</sub> Output signal rise time			0.8		ns
t <sub>f</sub> Output signal fall time			0.8		ns
t <sub>PHZ</sub> Propagation delay time, high-level-to-high-impedance output	See Figure 4		5.5	9	ns
t <sub>PLZ</sub> Propagation delay time, low-level-to-high-impedance output			4.4	9	ns
t <sub>PZH</sub> Propagation delay time, high-impedance -to-high-level output			3.8	9	ns
t <sub>PZL</sub> Propagation delay time, high-impedance-to-low-level output			7	9	ns

† All typical values are at 25°C and with a 3.3-V supply.

‡ t<sub>sk(pp)</sub> is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

§ t<sub>sk(o)</sub> is the magnitude of the time difference between the t<sub>PLH</sub> or t<sub>PHL</sub> of all receivers of a single device with all of their inputs driven together.

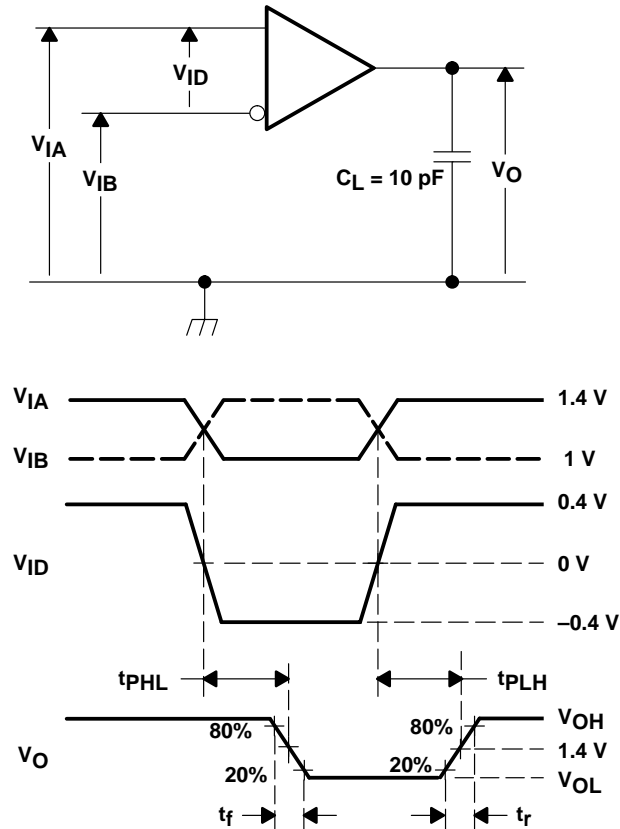
† Removed for testing the LVDT device



### Figure 2. $V_{IT1}$ and $V_{IT2}$ Input Voltage Threshold Test Circuit and Definitions



## PARAMETER MEASUREMENT INFORMATION



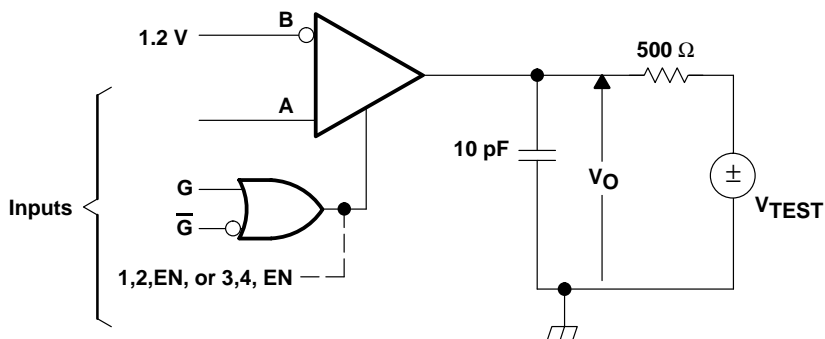
NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1 \text{ ns}$ , pulse repetition rate (PRR) = 50 Mpps, Pulswidth =  $10 \pm 0.2 \text{ ns}$ .  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

**Figure 3. Timing Test Circuit and Waveforms**

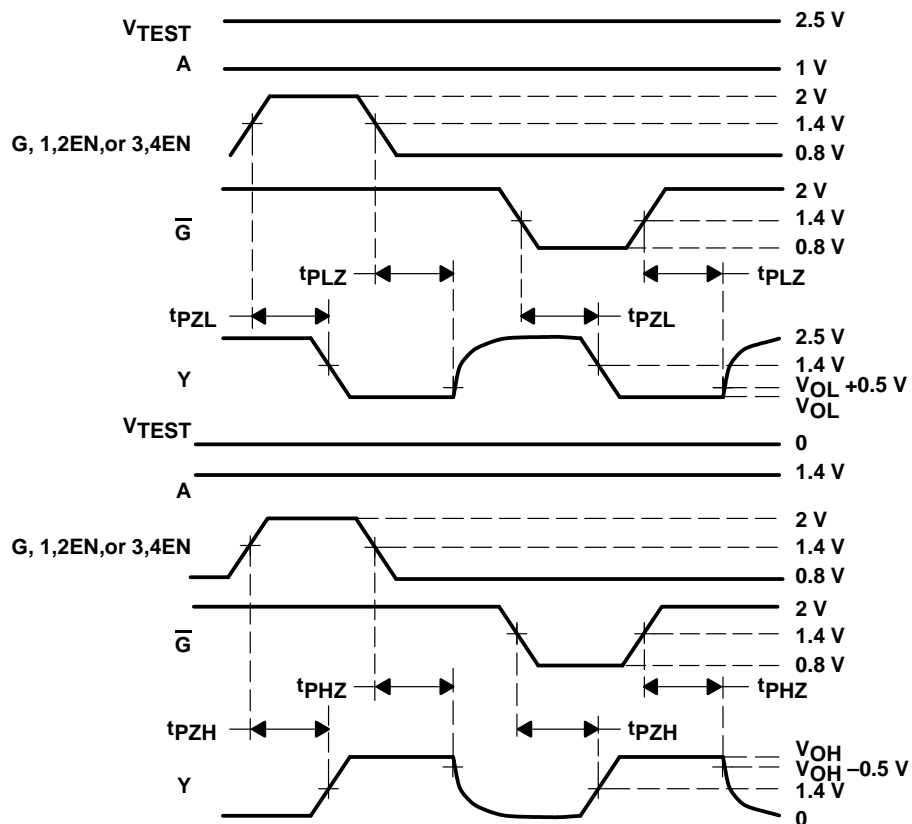
**SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B  
SN65LVDT3486B, SN65LVDS9637B, SN65LVDT9637B  
HIGH-SPEED DIFFERENTIAL RECEIVERS**

SLLS440A – OCTOBER 2000 – REVISED MAY 2001

**PARAMETER MEASUREMENT INFORMATION**



NOTE: All input pulses are supplied by a generator having the following characteristics:  $t_r$  or  $t_f \leq 1$  ns, pulse repetition rate (PRR) = 0.5 Mpps, Pulsewidth =  $500 \pm 10$  ns.  $C_L$  includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.



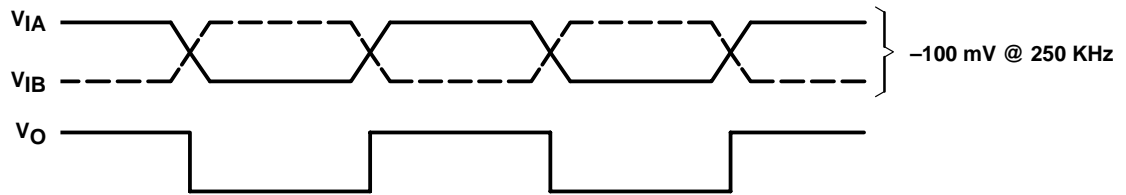
**Figure 4. Enable/Disable Time Test Circuit and Waveforms**

## PARAMETER MEASUREMENT INFORMATION

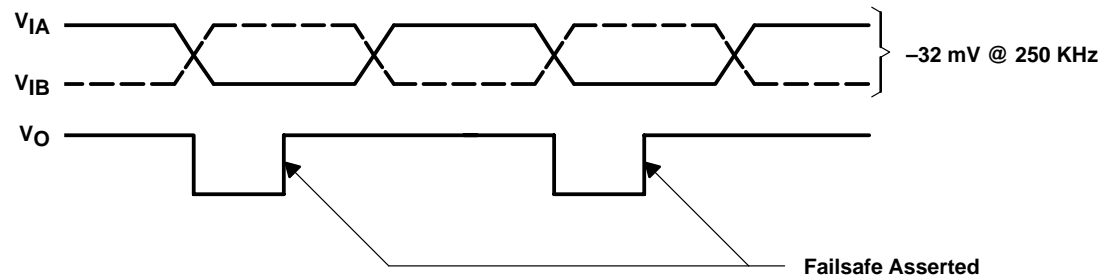
Table 1. Receiver Minimum and Maximum  $V_{IT3}$   
 Input Threshold Test Voltages

APPLIED VOLTAGES†		RESULTANT INPUTS		
$V_{IA}$ (mV)	$V_{IB}$ (mV)	$V_{ID}$ (mV)	$V_{IC}$ (mV)	Output
-2000	-1900	-100	-1950	L
-2000	-1968	-32	-1984	H
4300	4400	-100	4350	L
4368	4400	-32	4384	H

† These voltages are applied for a minimum of 1.5  $\mu$ s.



a) No Failsafe



b) Failsafe Asserted

Figure 5.  $V_{IT3}$  Failsafe Threshold Test

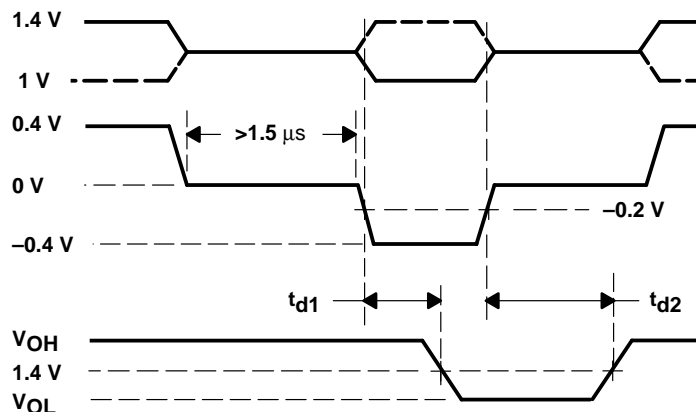
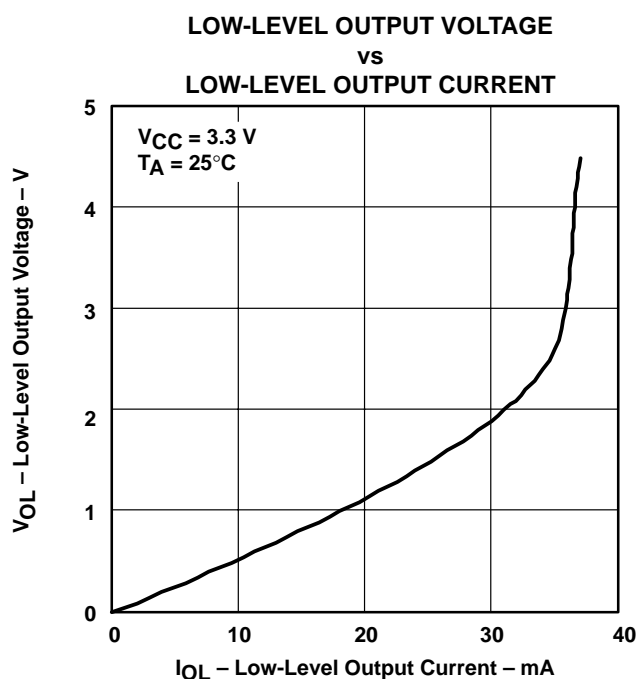


Figure 6. Waveforms for Failsafe Activate and Deactivate

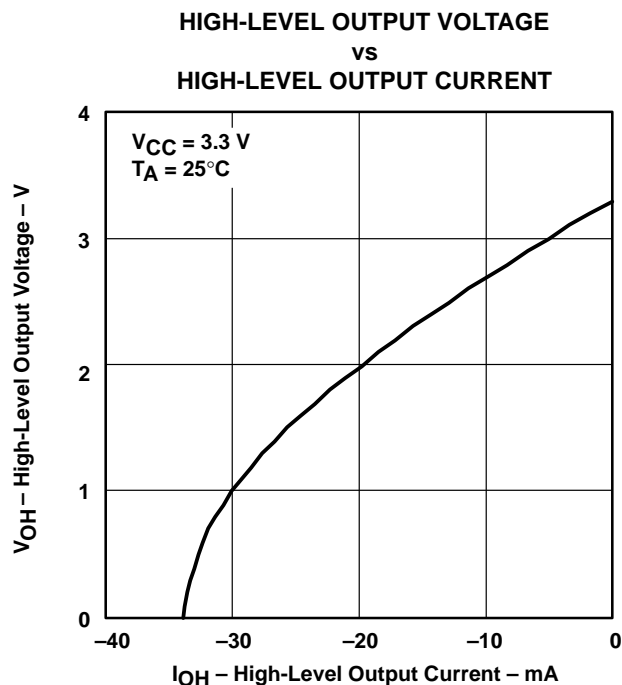
**SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B  
SN65LVDT3486B, SN65LVDS9637B, SN65LVDT9637B  
HIGH-SPEED DIFFERENTIAL RECEIVERS**

SLLS440A – OCTOBER 2000 – REVISED MAY 2001

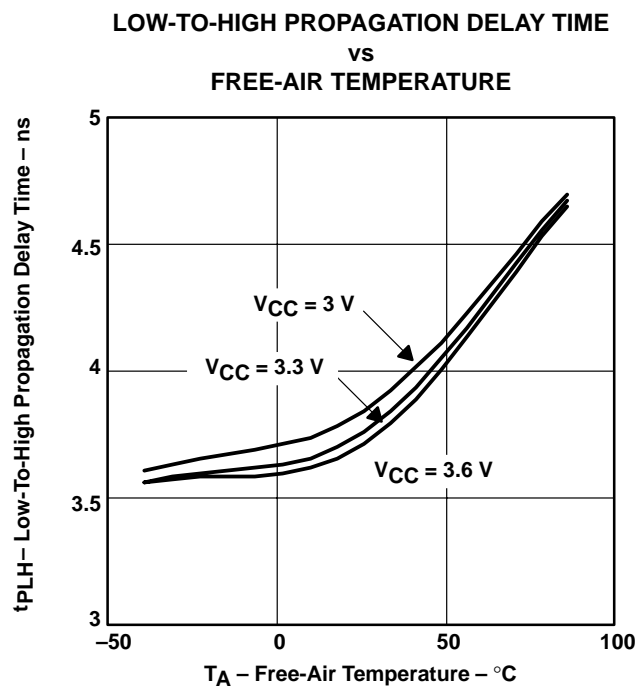
**TYPICAL CHARACTERISTICS**



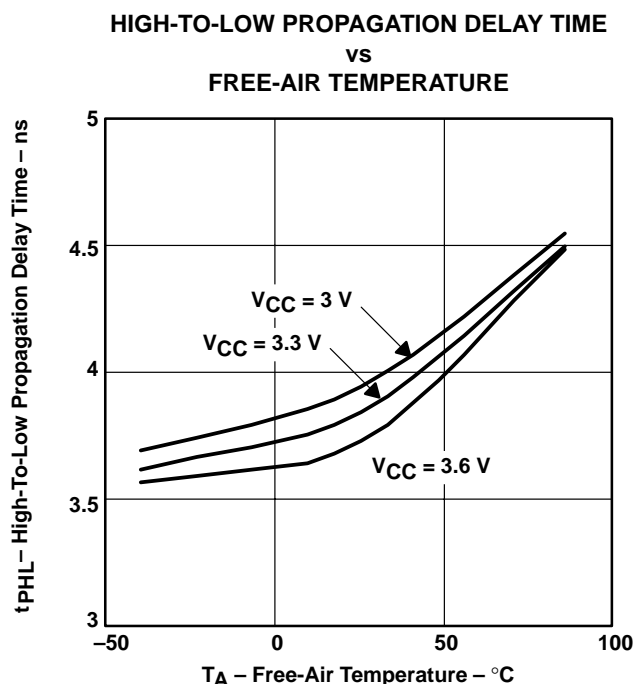
**Figure 7**



**Figure 8**



**Figure 9**



**Figure 10**

## TYPICAL CHARACTERISTICS

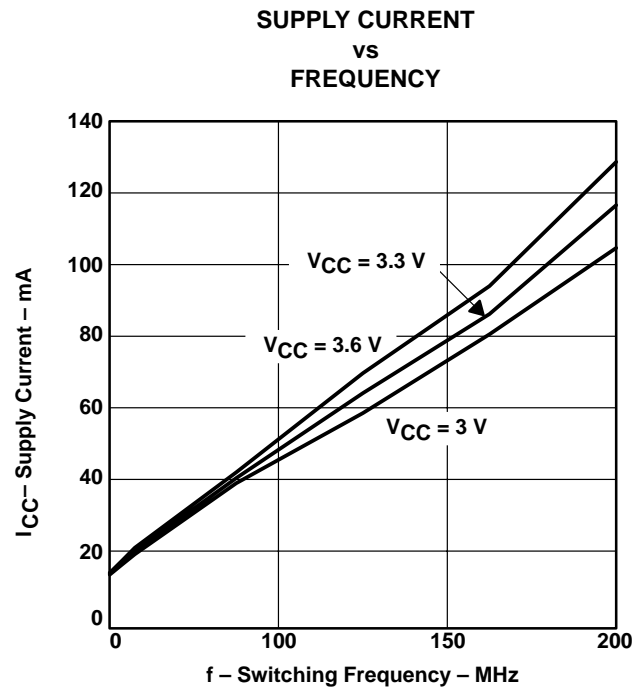
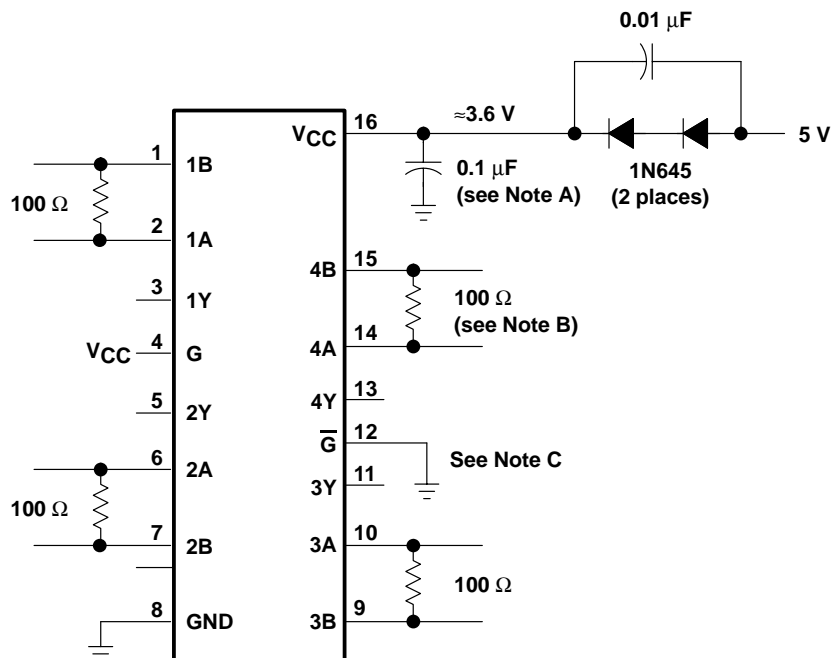


Figure 11

**SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B  
SN65LVDT3486B, SN65LVDS9637B, SN65LVDT9637B  
HIGH-SPEED DIFFERENTIAL RECEIVERS**

SLLS440A – OCTOBER 2000 – REVISED MAY 2001

**APPLICATION INFORMATION**



- NOTES: A. Place a 0.1-μF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V<sub>CC</sub> and the ground plane. The capacitor should be located as close as possible to the device terminals.
- B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.
- C. Unused enable inputs should be tied to V<sub>CC</sub> or GND as appropriate.

**Figure 12. Operation with 5-V Supply**

**related information**

IBIS modeling is available for this device. Please contact the local TI sales office or the TI Web site at [www.ti.com](http://www.ti.com) for more information.

For more application guidelines, please see the following documents:

- *Low-Voltage Differential Signalling Design Notes* (TI literature number SLLA014)
- *Interface Circuits for TIA/EIA-644 (LVDS)* (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

## APPLICATION INFORMATION

### terminated failsafe

A differential line receiver commonly has a fail-safe circuit to prevent it from switching on input noise. Current LVDS fail-safe solutions require either external components with subsequent reduction in signal quality or integrated solutions with limited application. This family of receivers has a new integrated fail-safe that solves the limitations seen in present solutions. A detailed theory of operation is presented in application note *The Active Fail-Safe Feature of the SN65LVDS32A*, literature number SLLA082.

Figure 13 shows one receiver channel with active fail-safe. It consists of a main receiver that can respond to a high-speed input differential signal. Also connected to the input pair are two fail-safe receivers that form a window comparator. The window comparator has a much slower response than the main receiver and detects when the input differential falls below 80 mV. A 600-ns fail-safe timer filters the window comparator outputs. When fail-safe is asserted, the fail-safe logic drives the main receiver output to logic high.

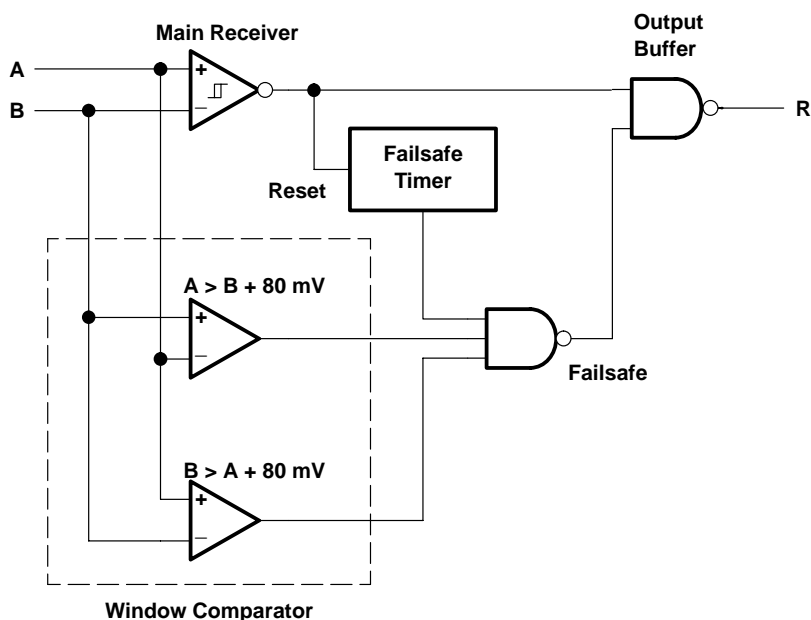


Figure 13. Receiver With Terminated Failsafe

## APPLICATION INFORMATION

### ECL/PECL-to-LVTTL conversion with TI's LVDS receiver

The various versions of emitter-coupled logic (i.e. ECL, PECL and LVPECL) are often the physical layer of choice for system designers. Designers know of the established technology and that it is capable of high-speed data transmission. In the past, system requirements often forced the selection of ECL. Now technologies like LVDS provide designers with another alternative. While the total exchange of ECL for LVDS may not be a design option, designers have been able to take advantage of LVDS by implementing a small resistor divider network at the input of the LVDS receiver. TI has taken the next step by introducing a wide common-mode LVDS receiver (no divider network required) which can be connected directly to an ECL driver with only the termination bias voltage required for ECL termination ( $V_{CC} - 2\text{ V}$ ).

Figures 14 and 15 show the use of an LV/PECL driver driving 5 meters of CAT-5 cable and being received by TI's wide common-mode receiver and the resulting eye pattern. The values for R3 are required in order to provide a resistor path to ground for the LV/PECL driver. With no resistor divider, R1 simply needs to match the characteristic load impedance of  $50\ \Omega$ . The R2 resistor is a small value and is intended to minimize any possible common-mode current reflections.

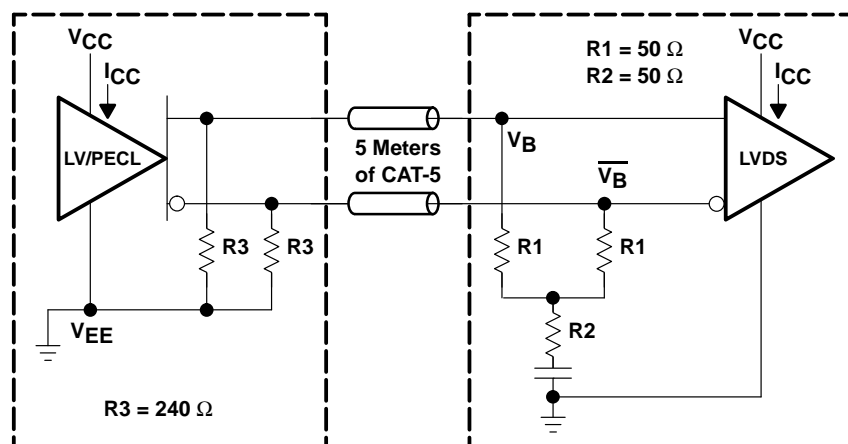


Figure 14. LVPECL or PECL to Remote Wide Common-Mode LVDS Receiver

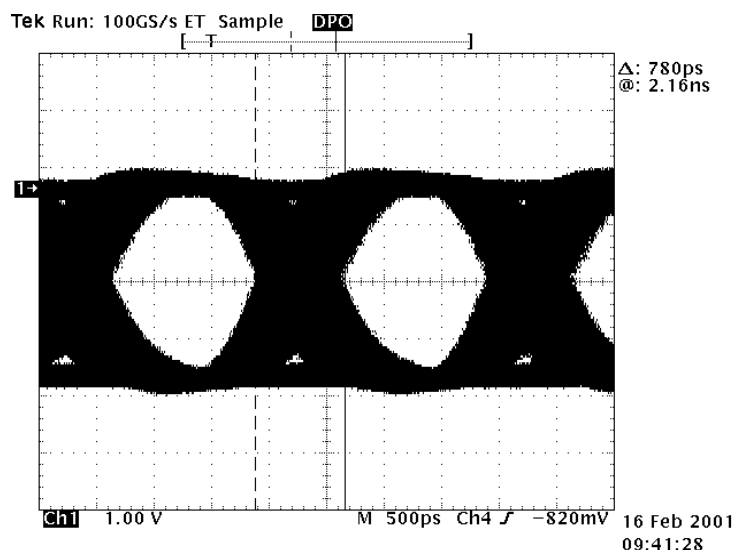


Figure 15. LV/PECL to Remote SN65LVDS32B at 500 Mbps Receiver Output (CH1)



## APPLICATION INFORMATION

### test conditions

- $V_{CC} = 3.3\text{ V}$
- $T_A = 25^\circ\text{C}$  (ambient temperature)
- All four channels switching simultaneously with NRZ data. Scope is pulse-triggered simultaneously with NRZ data.

### equipment

- Tektronix PS25216 programmable power supply
- Tektronix HFS 9003 stimulus system
- Tektronix TDS 784D 4-channel digital phosphor oscilloscope – DPO

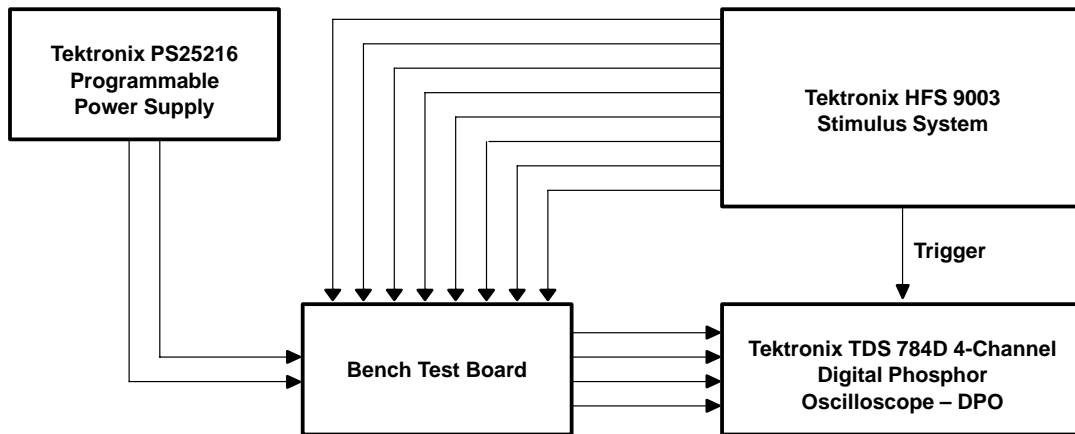


Figure 16. Equipment Setup

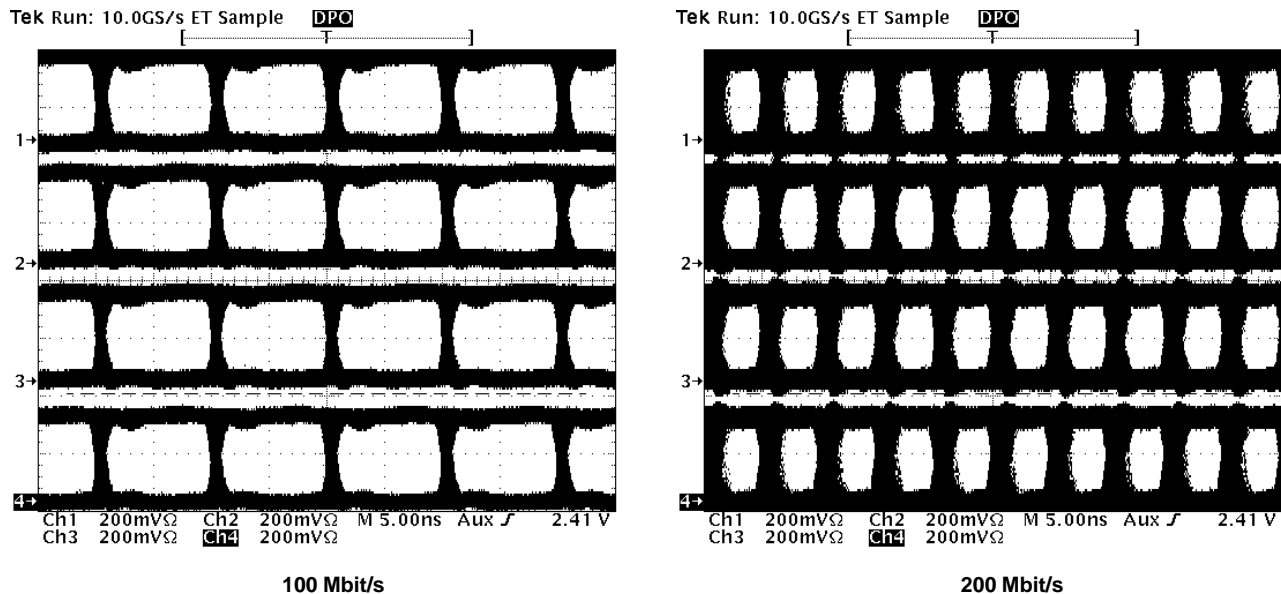


Figure 17. Typical Eye Pattern SN65LVDS32B

**SN65LVDS32B, SN65LVDT32B, SN65LVDS3486B  
SN65LVDT3486B, SN65LVDS9637B, SN65LVDT9637B  
HIGH-SPEED DIFFERENTIAL RECEIVERS**

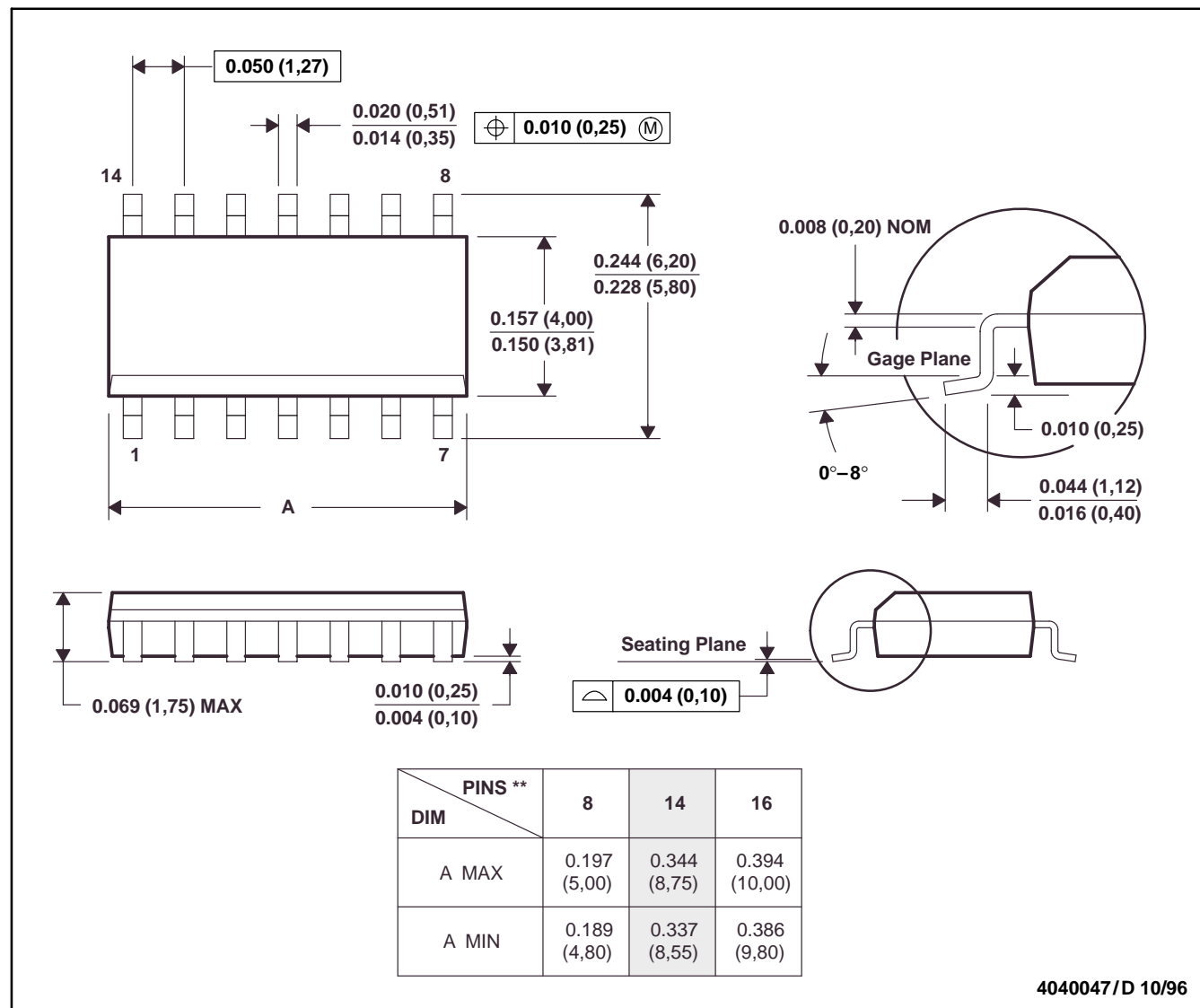
SLLS440A – OCTOBER 2000 – REVISED MAY 2001

**MECHANICAL DATA**

**D (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14 PIN SHOWN**



- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65LVDS32BD	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS32BDR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS3486BD	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS3486BDR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS9637BD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDS9637BDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDT32BD	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDT32BDR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDT3486BD	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDT3486BDR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDT9637BD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
SN65LVDT9637BDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated

Copyright © Each Manufacturing Company.

All Datasheets cannot be modified without permission.

This datasheet has been download from :

[www.AllDataSheet.com](http://www.AllDataSheet.com)

100% Free DataSheet Search Site.

Free Download.

No Register.

Fast Search System.

[www.AllDataSheet.com](http://www.AllDataSheet.com)