Low Voltage 1:15 Differential ÷1/÷2 ECL/PECL Clock Driver

MC100LVE222

LOW VOLTAGE 1:15 DIFFERENTIAL ÷1/÷2 ECL/PECL CLOCK DRIVER

FA SUFFIX
TQFP PACKAGE
CASE 848D–03

The MC100LVE222 is a low voltage, low skew 1:15 differential ÷1/÷2 ECL fanout buffer designed with clock distribution in mind. The device features fully differential clock paths to minimize both device and system skew. The LVE222 can be used as a simple fanout buffer or outputs can be configured to provide half frequency outputs. The combination of 1x and 1/2x frequencies is flexible providing for a myriad of combinations. All timing differences between the 1x and 1/2x signals are compensated for internal to the chip so that the output–to–output skew is identical regardless of what output frequencies are selected.

- Fifteen Differential Outputs
- 200ps Part–to–Part Skew
- 50ps Output–to–Output Skew
- Selectable 1x or 1/2x Frequency Outputs
- Extended Power Supply Range of –3.0V to –5.25V (+3.0V to +5.25V)
- 52–Lead TQFP Packaging
- ESD > 2000V

The fsel and CLK_Sel input pins are asynchronous control signals. As a result, changing these inputs could cause indeterminent excursions on the outputs immediately following the changes on the inputs.

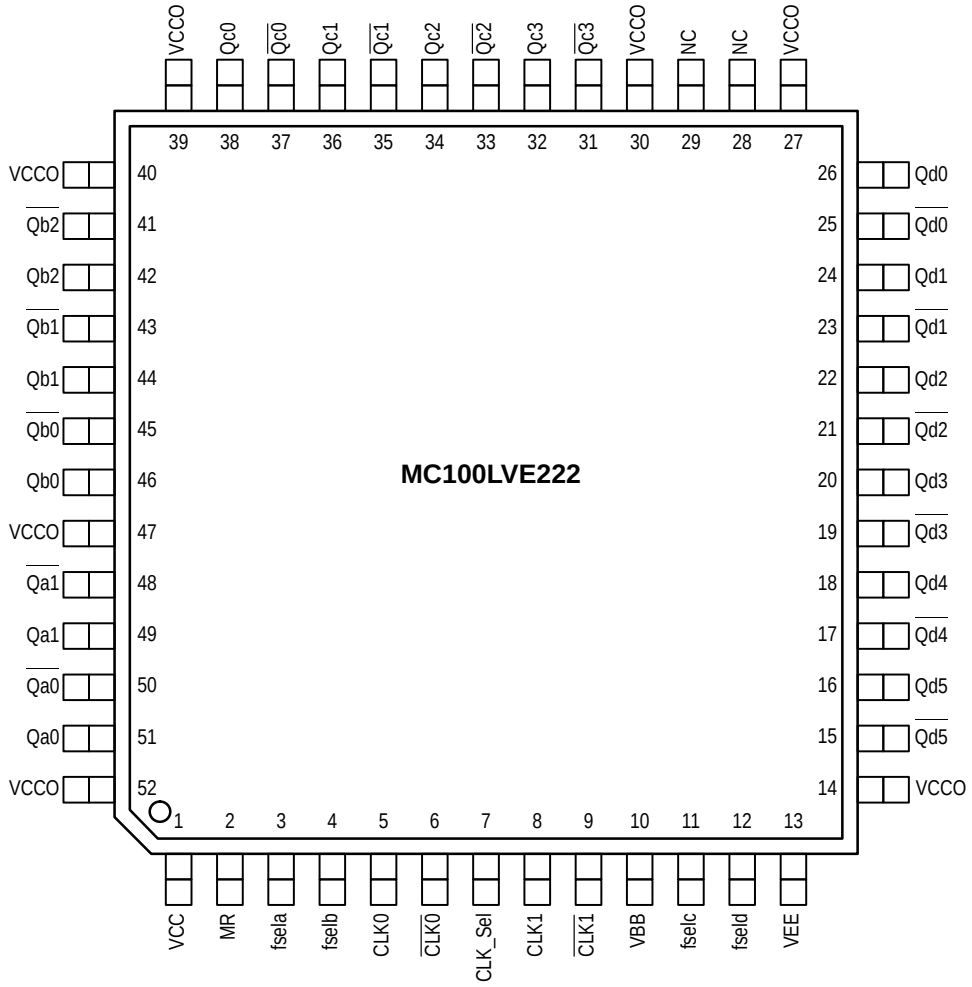
For applications which require a single–ended input, the V_{BB} reference voltage is supplied. For single–ended input applications the V_{BB} reference should be connected to the CLK input and bypassed to ground via a 0.01µf capacitor. The input signal is then driven into the CLK input.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications all fifteen differential pairs will be used and therefore terminated. In the case where fewer than fifteen pairs are used it is necessary to terminate at least the output pairs adjacent to the output pair being used in order to maintain minimum skew. Failure to follow this guideline will result in small degradations of propagation delay (on the order of 10–20ps) of the outputs being used, while not catastrophic to most designs this will result in an increase in skew. Note that the package corners isolate outputs from one another such that the guideline expressed above holds only for outputs on the same side of the package.

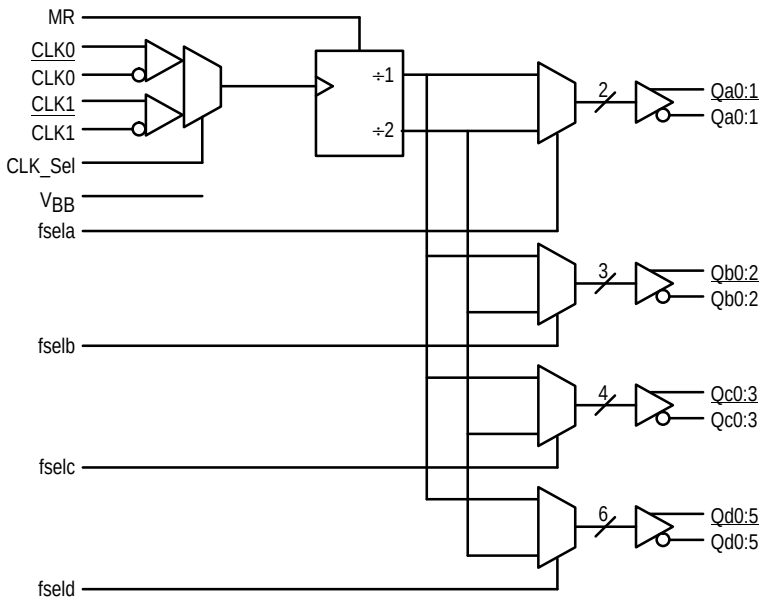
The MC100LVE222, as with most ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the LVE222 to be used for high performance clock distribution in +3.3V systems. Designers can take advantage of the LVE222's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line, terminations are typically used as they require no additional power supplies, if parallel termination is desired a terminating voltage of V_{CC}–2.0V will need to be provided. For more information on using PECL, designers should refer to Motorola Application Note AN1406/D.

The MC100LVE222 is packaged in the 52–lead TQFP package. For a 3.3V supply this package provides the optimum performance and minimizes board space requirements. The LVE222 will operate from a standard 100E –4.5V supply or a 5.0V PECL supply. The 52–lead TQFP utilizes a 10x10mm body with a lead pitch of 0.65mm.

Pinout: 52–Lead TQFP (Top View)



LOGIC SYMBOL



FUNCTION TABLE

Input	Function	
	0	**1**
MR	Active	Reset
CLK_Sel	CLK0	CLK1
fseln	÷1	÷2

ECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	–1.085	–1.005	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	–1.025	–0.955	–0.880	V
V_{OL}	Output LOW Voltage	–1.830	–1.695	–1.555	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	–1.810	–1.705	–1.620	V
V_{IH}	Input HIGH Voltage	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	–1.165		–0.880	V
V_{IL}	Input LOW Voltage	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	–1.810		–1.475	V
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
V_{EE}	Power Supply Voltage	–3.0		–5.25	–3.0		–5.25	–3.0		–5.25	–3.0		–5.25	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current $\overline{CLK0}$, $\overline{CLK1}$ Others	–300 0.5			–300 0.5			–300 0.5			–300 0.5			µA
I_{EE}	Power Supply Current		122	136		122	136		122	136		125	139	mA

PECL DC CHARACTERISTICS

Symbol	Characteristic	–40°C			0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1.]	2.215	2.295	2.420	2.275	2.345	2.420	2.275	2.345	2.420	2.275	2.345	2.420	V
V_{OL}	Output LOW Voltage[1.]	1.470	1.605	1.745	1.490	1.595	1.680	1.490	1.595	1.680	1.490	1.595	1.680	V
V_{IH}	Input HIGH Voltage[1.]	2.135		2.420	2.135		2.420	2.135		2.420	2.135		2.420	V
V_{IL}	Input LOW Voltage[1.]	1.490		1.825	1.490		1.825	1.490		1.825	1.490		1.825	V
V_{BB}	Output Reference Voltage[1.]	1.92		2.04	1.92		2.04	1.92		2.04	1.92		2.04	V
V_{CC}	Power Supply Voltage	3.0		5.25	3.0		5.25	3.0		5.25	3.0		5.25	V
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current $\overline{CLK0}$, $\overline{CLK1}$ Others	–300 0.5			–300 0.5			–300 0.5			–300 0.5			µA
I_{EE}	Power Supply Current		122	136		122	136		122	136		125	139	mA

1. These values are for V_{CC} = 3.3V. Level Specifications will vary 1:1 with V_{CC}.

ECL AC CHARACTERISTICS (V_{EE} = V_{EE} (min) to V_{EE} (max); V_{CC} = V_{CCO} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended) MR	 1040 990 1100	 1140 1140 1250	 1240 1290 1400	 1060 1010 1130	 1160 1160 1280	 1260 1310 1430	 1080 1030 1170	 1180 1180 1320	 1280 1330 1470	 1120 1070 1220	 1220 1220 1370	 1320 1370 1520	ps	 Note 1. Note 2.
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)			50 200			50 200			50 200			50 200	ps	Note 3.
V_{PP}	Minimum Input Swing	400			400			400			400			mV	Note 4.
V_{CMR}	Common Mode Range V_{PP} < 500mV V_{PP} ≥ 500mV	 V_{EE} +1.3 V_{EE} +1.6		 –0.4 –0.4	 V_{EE} +1.2 V_{EE} +1.5		 –0.4 –0.4	 V_{EE} +1.2 V_{EE} +1.5		 –0.4 –0.4	 V_{EE} +1.2 V_{EE} +1.5		 –0.4 –0.4	V	Note 5.
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the LVE222. A differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

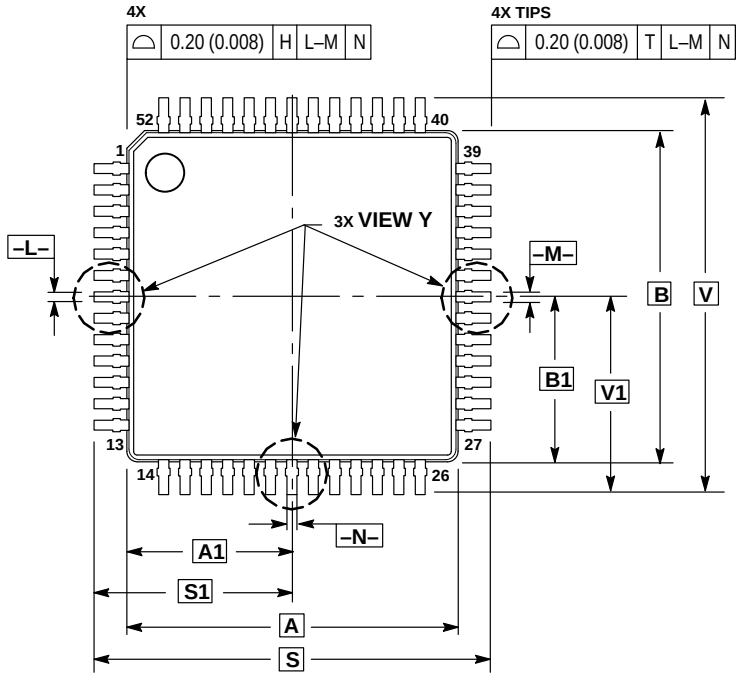
PECL AC CHARACTERISTICS (V_{EE} = GND; V_{CC} = V_{CCO} = V_{CC} (min) to V_{CC} (max))

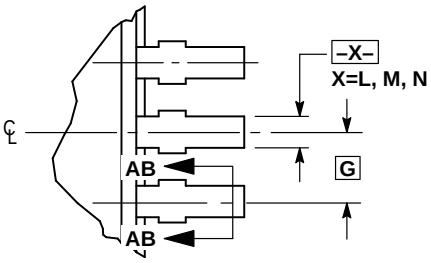
Symbol	Characteristic	–40°C			0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended) MR	 1040 990 1100	 1140 1140 1250	 1240 1290 1400	 1060 1010 1130	 1160 1160 1280	 1260 1310 1430	 1080 1030 1170	 1180 1180 1320	 1280 1330 1470	 1120 1070 1220	 1220 1220 1370	 1320 1370 1520	ps	 Note 1. Note 2.
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)			50 200			50 200			50 200			50 200	ps	Note 3.
V_{PP}	Minimum Input Swing	400			400			400			400			mV	Note 4.
V_{CMR}	Common Mode Range V_{PP} < 500mV V_{PP} ≥ 500mV	 1.3 1.6		 V_{CC} –0.4 V_{CC} –0.4	 1.2 1.5		 V_{CC} –0.4 V_{CC} –0.4	 1.2 1.5		 V_{CC} –0.4 V_{CC} –0.4	 1.2 1.5		 V_{CC} –0.4 V_{CC} –0.4	V	Note 5.
t_r/t_f	Output Rise/Fall Time	200		600	200		600	200		600	200		600	ps	20%–80%

1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. The within–device skew is defined as the worst case difference between any two similar delay paths within a single device.
4. V_{PP}(min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP}(min) is AC limited for the LVE222. A differential input as low as 50 mV will still produce full ECL levels at the output.
5. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP}(min).

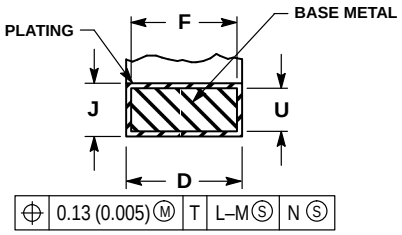
OUTLINE DIMENSIONS

FA SUFFIX
TQFP PACKAGE
CASE 848D–03
ISSUE C

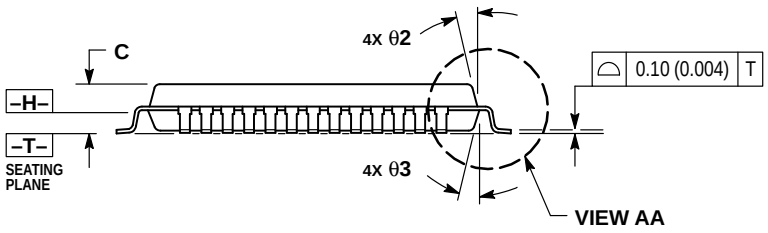


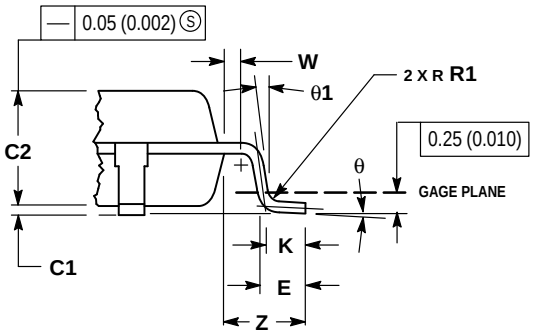


VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE





VIEW AA

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°

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