1:5 Clock Distribution Chip

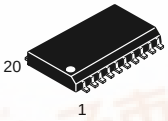
MC100LVEL14
MC100EL14

The MC100LVEL/100EL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The LVEL14 is functionally and pin compatible with the EL14 but is designed to operate in ECL or PECL mode for a voltage supply range of –3.0V to –3.8V (or 3.0V to 3.8V). If a single-ended input is to be used the V_{BB} output should be connected to the CLK input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the LVEL14 under single-ended input conditions, as a result this pin can only source/sink up to 0.5mA of current.

The LVEL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

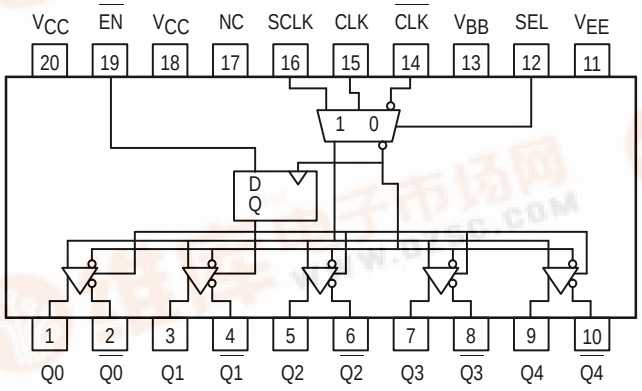
The common enable (EN) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

- 50ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- 75kΩ Internal Input Pulldown Resistors
- >2000V ESD Protection
- V_{EE} Range of –3.0V to –5.5V



DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-04

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
CLK	Diff Clock Inputs
SCLK	Scan Clock Input
EN	Sync Enable
SEL	Clock Select Input
V_{BB}	Reference Output
$Q_{0–4}$	Diff Clock Outputs

FUNCTION TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK or SCLK

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Characteristic	Rating	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V)	0 to –6.0	VDC
I_{out}	Output Current Continuous Surge	50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
V_{EE}	Operating Range[1,2]	–5.7 to –4.2	V

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 100EL Series: –4.20V to –5.50V
   10EL Series: –4.94V to –5.50V

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1])

Symbol	Characteristic	–40°C			0°C to 85°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max		
V_{OH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	mV	V_{IN} = V_{IH}(max)
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1810	–1705	–1620	mV	or V_{IL}(min)
V_{OHA}	Output HIGH Voltage	–1095	—	—	–1035	—	—	mV	V_{IN} = V_{IH}(max)
V_{OLA}	Output LOW Voltage	—	—	–1555	—	—	–1610	mV	or V_{IL}(min)
V_{IH}	Input HIGH Voltage	–1165	—	–880	–1165	—	–880	mV	
V_{IL}	Input LOW Voltage	–1810	—	–1475	–1810	—	–1475	mV	
I_{IL}	Input LOW Current $\overline{CLK}$ Others	–300 0.5	—	—	–300 0.5	—	—	µA	V_{IN} = V_{IL}(max)

1. This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –3.0V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

MC100LVEL14 AC/DC CHARACTERISTICS (V_{EE} = –3.8V to –3.0V; V_{CC} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current 100LVEL 100EL		32 32	40 40		32 32	40 40		32 32	40 40		34 34	42 42	mA
V_{BB}	Output Ref Voltage 100LVEL 100EL	–1.43 –1.38		–1.30 –1.26	–1.38 –1.38		–1.27 –1.26	–1.35 –1.38		–1.25 –1.26	–1.31 –1.38		–1.19 –1.26	V
I_{IH}	Input High Current			150			150			150			150	µA
t_{PLH} t_{PHL}	Prop Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	520 470 470		720 770 770	550 500 500		750 800 800	580 530 530	680 680 680	780 830 830	630 580 580		830 880 880	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew[1]			200 50			200 50			200 50			200 50	ps
t_S	Setup Time $\overline{EN}$	0			0			0			0			ps
t_H	Hold Time $\overline{EN}$	0			0			0			0			ps
V_{PP}	Minimum Input Swing CLK	150			150			150			150			mV
V_{CMR}	Common Mode Range[2] V_{PP} < 500mV V_{PP} ≥ 500mV	 –2.0 –1.8		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	 –2.1 –1.9		 –0.4 –0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	230		500	ps

1. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR}(min) will be fixed at 3.3V – |V_{CMR}(min)|.

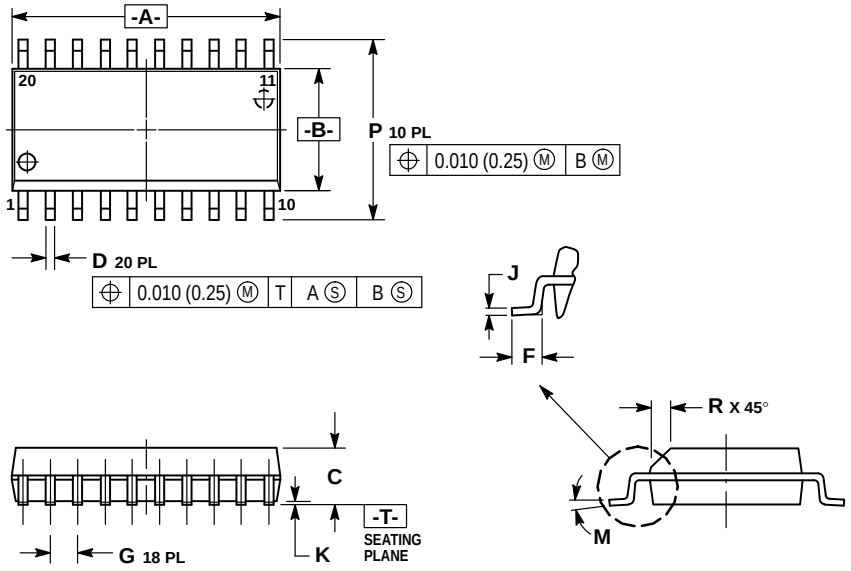
MC100EL14 AC/DC CHARACTERISTICS (V_{EE} = –4.2V to –5.5V; V_{CC} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current 100LVEL 100EL		32 32	40 40		32 32	40 40		32 32	40 40		34 34	42 42	mA
V_{BB}	Output Ref Voltage 100LVEL 100EL	–1.43 –1.38		–1.30 –1.26	–1.38 –1.38		–1.27 –1.26	–1.35 –1.38		–1.25 –1.26	–1.31 –1.38		–1.19 –1.26	V
I_{IH}	Input High Current			150			150			150			150	µA
t_{PLH} t_{PHL}	Prop Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	520 470 470		720 770 770	550 500 500		750 800 800	580 530 530	680 680 680	780 830 830	630 580 580		830 880 880	ps
t_{SKEW}	Part-to-Part Skew Within-Device Skew[1]			200 50			200 50			200 50			200 50	ps
t_S	Setup Time $\overline{EN}$	0			0			0			0			ps
t_H	Hold Time $\overline{EN}$	0			0			0			0			ps
V_{PP}	Minimum Input Swing CLK	150			150			150			150			mV
V_{CMR}	Common Mode Range[2] V_{PP} < 500mV V_{PP} ≥ 500mV	 –3.2 –3.0		 –0.4 –0.4	 –3.3 –3.1		 –0.4 –0.4	 –3.3 –3.1		 –0.4 –0.4	 –3.3 –3.1		 –0.4 –0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	230		500	230		500	230		500	230		500	ps

1. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
2. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –4.5V. Note for PECL operation, the V_{CMR}(min) will be fixed at 5.0V – |V_{CMR}(min)|.

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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