÷2/4, ÷4/6 Clock Generation Chip

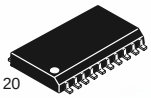
MC100LVEL39
MC100EL39

The MC100LVEL39 is a low skew ÷2/4, ÷4/6 clock generation chip designed explicitly for low skew clock generation applications. The MC100EL39 is pin and functionally equivalent to the MC100LVEL39 but is specified for operation at the standard 100K ECL voltage supply. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended LVECL or, if positive power supplies are used, LVPECL input signal. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device (see Interfacing section of the ECLinPS™ Data Book DL140/D). If a single-ended input is to be used, the V_{BB} output should be connected to the CLK input and bypassed to ground via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the LVEL39 under single-ended input conditions, as a result, this pin can only source/sink up to 0.5mA of current.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

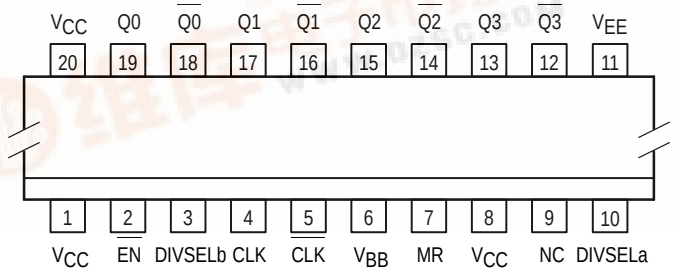
Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple LVEL39s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one LVEL39, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2/4 and the ÷4/6 outputs of a single device.

- 50ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- 75kΩ Internal Input Pulldown Resistors
- >2000V ESD Protection
- Low Voltage V_{EE} Range of –3.0 to –3.8V



DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-04

Pinout: 20-Lead SOIC (Top View)



PIN DESCRIPTION

PIN	FUNCTION
CLK	Diff Clock Inputs
EN	Sync Enable
MR	Master Reset
V_{BB}	Reference Output
Q_0, Q_1	Diff ÷2/4 Outputs
Q_2, Q_3	Diff ÷4/6 Outputs
DIVSEL	Frequency Select Input

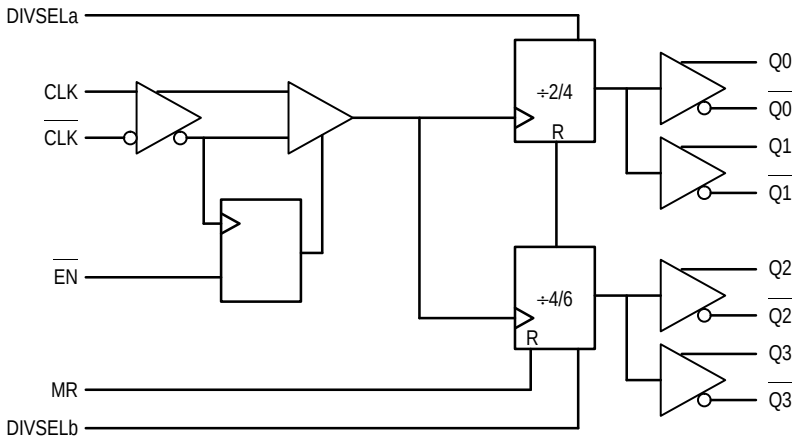
FUNCTION TABLE

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold $Q_{0–3}$
X	X	H	Reset $Q_{0–3}$

Z = Low-to-High Transition
ZZ = High-to-Low Transition

DIVSELa	Q_0, Q_1 OUTPUTS
0	Divide by 2
1	Divide by 4
DIVSELb	**Q_2, Q_3 OUTPUTS**
0	Divide by 4
1	Divide by 6

LOGIC DIAGRAM



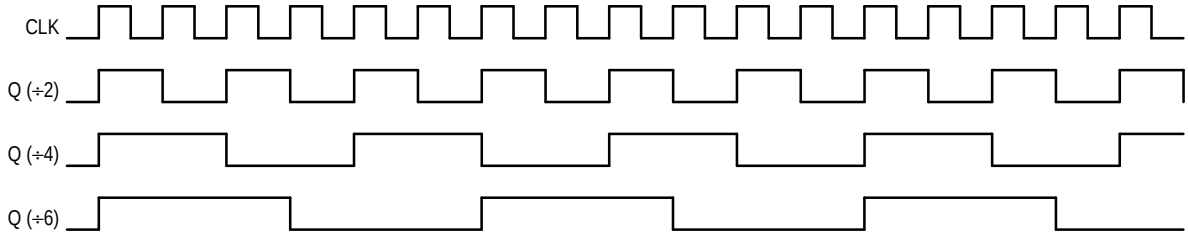


Figure 1. Timing Diagrams

MC100LVEL39
DC CHARACTERISTICS (V_{EE} = –3.8V to –3.0; V_{CC} = GND)

Symbol	Characteristic	–40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		50	59		50	59		50	59		54	61	mA
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
I_{IH}	Input High Current			150			150			150			150	μA

MC100LVEL39
AC CHARACTERISTICS (V_{EE} = –3.8V to –3.0; V_{CC} = GND)

Symbol	Characteristic		–40°C			0°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Toggle Frequency		1000			1000			1000			1000			MHz
t_{PLH} t_{PHL}	Propagation Delay to Output	CLK → Q (Diff) CLK → Q (S.E.) MR → Q	760 710 600		960 1010 900	780 730 600		980 1030 900	800 750 610		1000 1050 910	850 800 630		1050 1100 930	ps
t_{SKEW}	Within-Device Skew[1]	$Q_0 - Q_3$			50			50			50			50	ps
	Part-to-Part	$Q_0 - Q_3$ (Diff)			200			200			200			200	
t_S	Setup Time	$\overline{EN}$ → CLK DIVSEL → CLK	250 400			250 400			250 400			250 400			ps
t_H	Hold Time	CLK → $\overline{EN}$ CLK → Div_Sel	100 150			100 150			100 150			100 150			ps

MC100LVEL39 (continued)
AC CHARACTERISTICS (V_{EE} = –3.8V to –3.0; V_{CC} = GND)

Symbol	Characteristic		–40°C Min	–40°C Typ	–40°C Max	0°C Min	0°C Typ	0°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Typ	85°C Max	Unit
V_{PP}	Minimum Input Swing	CLK	250			250			250			250			mV
V_{CMR}	Common Mode Range[3]	V_{PP} < 500mV	–2.0		–0.4	–2.1		–0.4	–2.1		–0.4	–2.1		–0.4	V
		V_{PP} ≥ 500mV	–1.8		–0.4	–1.9		–0.4	–1.9		–0.4	–1.9		–0.4	
t_{RR}	Reset Recovery Time				100			100			100			100	ps
t_{PW}	Minimum Pulse Width	CLK	500			500			500			500			ps
		MR	700			700			700			700			
t_r, t_f	Output Rise/Fall Times Q (20% – 80%)		280		550	280		550	280		550	280		550	ps

1. Skew is measured between outputs under identical transitions.
2. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
3. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –3.3V. Note for PECL operation, the V_{CMR}(min) will be fixed at 3.3V – |V_{CMR}(min)|.

MC100EL39
DC CHARACTERISTICS (V_{EE} = –4.2V to –5.46; V_{CC} = GND)

Symbol	Characteristic	–40°C Min	–40°C Typ	–40°C Max	0°C Min	0°C Typ	0°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Typ	85°C Max	Unit
I_{EE}	Power Supply Current		50	59		50	59		50	59		54	61	mA
V_{BB}	Output Reference Voltage	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	–1.38		–1.26	V
I_{IH}	Input High Current			150			150			150			150	μA

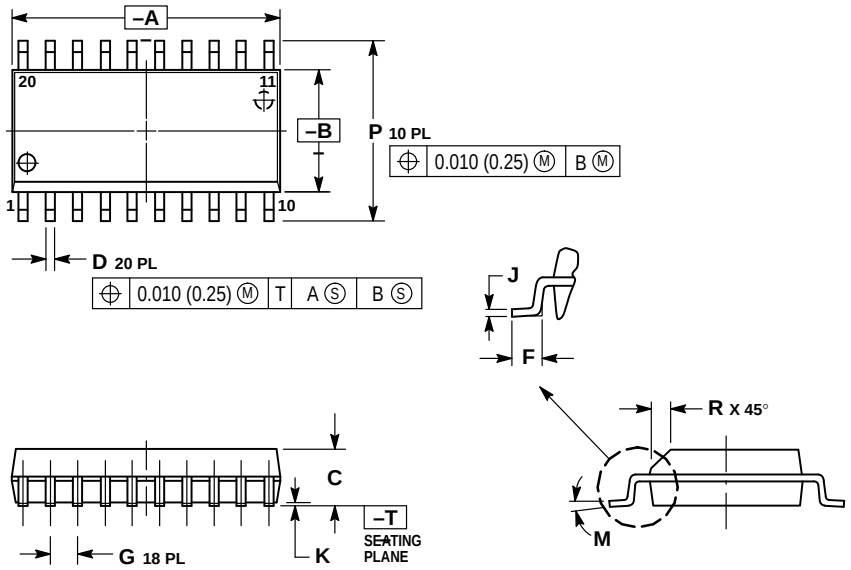
MC100EL39
AC CHARACTERISTICS (V_{EE} = –4.2V to –5.46; V_{CC} = GND)

Symbol	Characteristic		–40°C Min	–40°C Typ	–40°C Max	0°C Min	0°C Typ	0°C Max	25°C Min	25°C Typ	25°C Max	85°C Min	85°C Typ	85°C Max	Unit
f_{MAX}	Maximum Toggle Frequency		1000			1000			1000			1000			MHz
t_{PLH} t_{PHL}	Propagation Delay to Output	CLK → Q (Diff)	760		960	780		980	800		1000	850		1050	ps
		CLK → Q (S.E.)	710		1010	730		1030	750		1050	800		1100	
		MR → Q	600		900	600		900	610		910	630		930	
t_{SKEW}	Within-Device Skew[1]	$Q_0 - Q_3$			50			50			50			50	ps
	Part-to-Part	$Q_0 - Q_3$ (Diff)			200			200			200			200	
t_S	Setup Time	$\overline{EN}$ → CLK	250			250			250			250			ps
		DIVSEL → CLK	400			400			400			400			
t_H	Hold Time	CLK → $\overline{EN}$	100			100			100			100			ps
		CLK → Div_Sel	150			150			150			150			
V_{PP}	Minimum Input Swing	CLK	250			250			250			250			mV
V_{CMR}	Common Mode Range[3]	V_{PP} < 500mV	–3.2		–0.4	–3.3		–0.4	–3.3		–0.4	–3.3		–0.4	V
		V_{PP} ≥ 500mV	–3.0		–0.4	–3.1		–0.4	–3.1		–0.4	–3.1		–0.4	
t_{RR}	Reset Recovery Time				100			100			100			100	ps
t_{PW}	Minimum Pulse Width	CLK	500			500			500			500			ps
		MR	700			700			700			700			
t_r, t_f	Output Rise/Fall Times Q (20% – 80%)		280		550	280		550	280		550	280		550	ps

1. Skew is measured between outputs under identical transitions.
2. Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
3. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP}min and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = –4.5V. Note for PECL operation, the V_{CMR}(min) will be fixed at 5.0V – |V_{CMR}(min)|.

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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