Dual LVTTL/LVCMOS to Differential LVPECL Translator

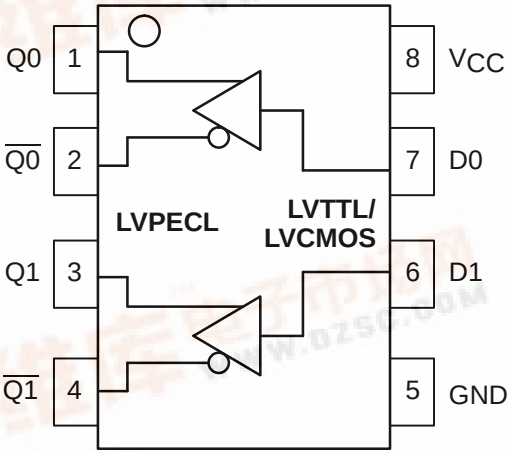
MC100LVELT22

The MC100LVELT22 is a dual LVTTL/LVCMOS to differential LVPECL translator. Because LVPECL (Low Voltage Positive ECL) levels are used, only +3.3V and ground are required. The small outline 8-lead SOIC package and the low skew, dual gate design of the LVELT22 makes it ideal for applications which require the translation of a clock and a data signal.

- 350ps Typical Propagation Delay
- <100ps Output–to–Output Skew
- Differential LVPECL Outputs
- Small Outline SOIC Package
- Flow Through Pinouts

D SUFFIX
8–LEAD PLASTIC SOIC PACKAGE
CASE 751-05

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



PIN DESCRIPTION

PIN	FUNCTION
Qn	Diff PECL Outputs
Dn	LVTTL/LVCMOS Inputs
V_{CC}	+3.3V Supply
GND	Ground

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	7.0	V
V_{IN}	Input Voltage	0 to V_{CC}	V
I_{OUT}	Current Applied to Output in Low Output State Continuous Surge	50 100	mA
T_A	Operating Temperature Range (In Free-Air)	–40 to 85	°C
T_{STG}	Storage Temperature Range	–55 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

LVTTL/LVCMOS INPUT DC CHARACTERISTICS (V_{CC} = 3.3V ±5%; T_A = –40°C to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			20	µA	V_{IN} = 2.7V
I_{IHH}	Input HIGH Current			100	µA	V_{IN} = V_{CC}
I_{IL}	Input LOW Current			–0.2	mA	V_{IN} = 0.5V
V_{IK}				–1.2	V	I_{IN} = –18mA
V_{IH}	Input HIGH Voltage	2.0			V	
V_{IL}	Input LOW Voltage			0.8	V	

LVPECL OUTPUT DC CHARACTERISTICS (V_{CC} = 3.3V ±5%; T_A = –40°C to 85°C)

		–40°C		0°C		25°C			85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Typ	Max	Min	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	2.275	2.420	2.275	2.420	2.275	2.345	2.420	2.275	2.420	V	V_{CC} = 3.3V Note 1.
V_{OL}	Output LOW Voltage	1.490	1.680	1.490	1.680	1.490	1.595	1.680	1.490	1.680	V	V_{CC} = 3.3V Note 1.
I_{CC}	Power Supply Current		23		23			23		24	mA	

1. Levels will vary 1:1 with V_{CC}.

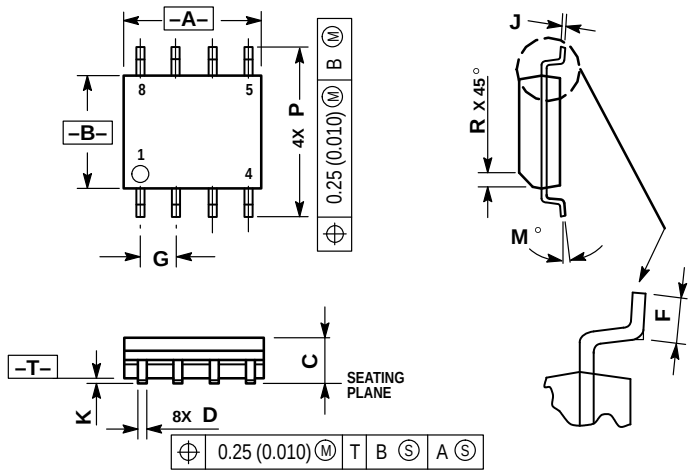
AC CHARACTERISTICS (V_{CC} = 3.3V ±5%; T_A = –40°C to 85°C)

		–40°C		0°C		25°C			85°C			
Symbol	Characteristic	Min	Max	Min	Max	Min	Typ	Max	Min	Max	Unit	Condition
t_{PLH}	Propagation Delay	200	600	200	600	200	350	600	200	600	ps	Note 2.
t_{skew}	Skew Output–to–Output Part–to–Part		100 400		100 400		30	100 400		100 400	ps	
t_r/t_f	Output Rise/Fall Time	250	550	200	500	200		500	200	500	ps	20–80%
f_{MAX}	Maximum Input Frequency	300		300		300			300		MHz	Note 3.

2. Specifications for standard TTL input signal.
3. f_{MAX} specification is set to anticipated input frequency limitations.

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–05
ISSUE P



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0 °	7 °
P	5.80	6.20
R	0.25	0.50

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405; Denver, Colorado 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298