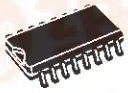
# 74VHC174

## HEX D-TYPE FLIP FLOP WITH CLEAR

**PRELIMINARY DATA**

- HIGH SPEED:
  $f_{MAX}$ =175 MHz (TYP.) at $V_{CC}$ = 5V
- LOW POWER DISSIPATION:
  $I_{CC}$ = 4 µA (MAX.) at $T_A$ = 25 °C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28% $V_{CC}$ (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 8 mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  $V_{CC}$ (OPR) = 2V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 174
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP}$ = 0.8V (Max.)



**M**
(Micro Package)

**T**
(TSSOP Package)

**ORDER CODES :**
74VHC174M 74VHC174T

### DESCRIPTION

The 74VHC174 is an advanced high-speed CMOS HEX D-TYPE FLIP FLOP WITH CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring $C^2MOS$ technology.

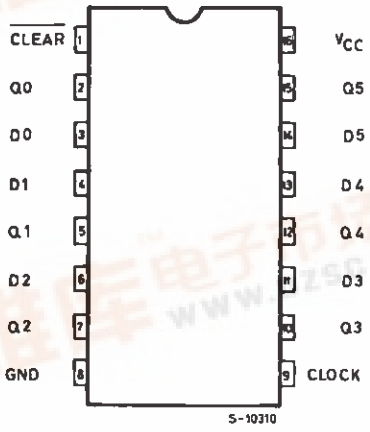
Information signals applied to D inputs are transfered to the Q outputs on the positive going edge of the clock pulse.

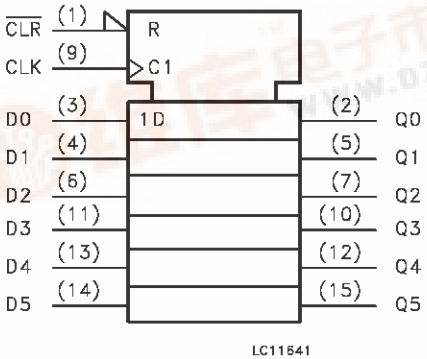
When the $\overline{CLEAR}$ input is held low, the Q outputs are held low independently of the other inputs.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

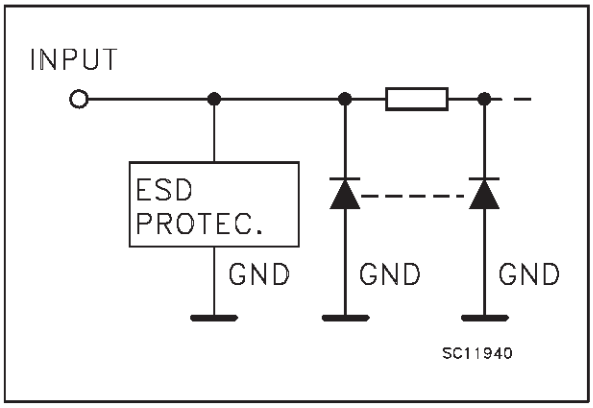
All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

### PIN CONNECTION AND IEC LOGIC SYMBOLS



## INPUT EQUIVALENT CIRCUIT




## PIN DESCRIPTION

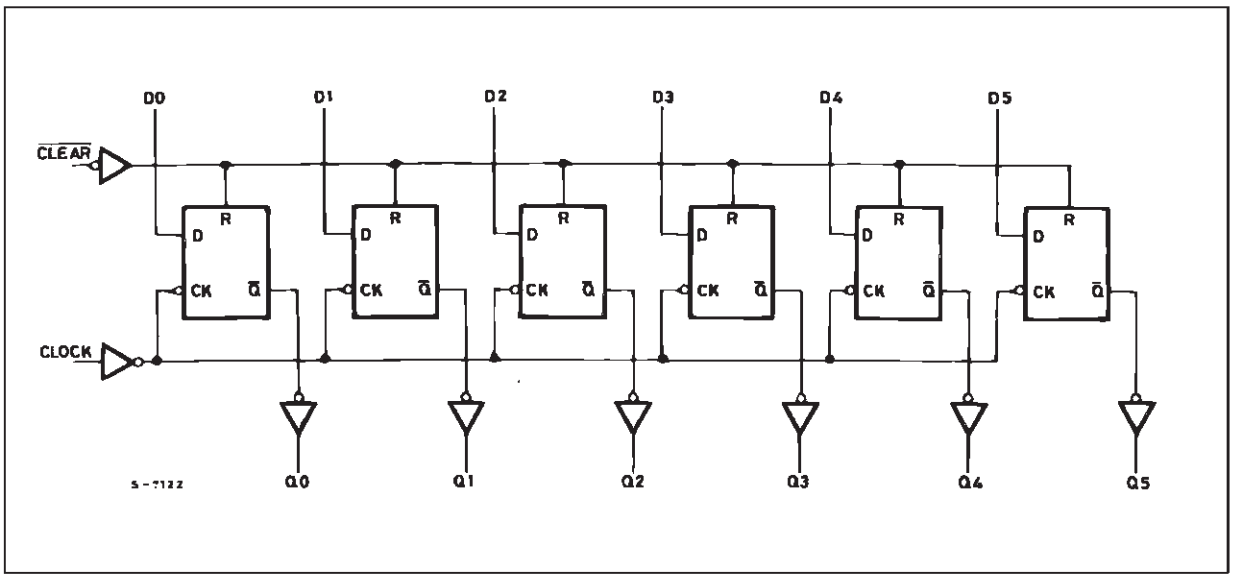
| PIN No | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1 | $\overline{CLEAR}$ | Asyncronous Master Reset (Active LOW) |
| 2, 5, 7, 10, 12, 15 | Q0 to Q5 | Flip-Flop Outputs |
| 3, 4, 6, 11, 13, 14 | D0 to D5 | Data Inputs |
| 9 | CLOCK | Clock Input (LOW-to-HIGH, Edge- Triggered) |
| 8 | GND | Ground (0V) |
| 16 | $V_{CC}$ | Positive Supply Voltage |

## TRUTH TABLE

| INPUTS | | | OUTPUTS | FUNCTION |
|---|---|---|---|---|
| $\overline{CLEAR}$ | D | CLOCK | Q | |
| L | X | X | L | CLEAR |
| H | L | ↑ | L | |
| H | H | ↑ | H | |
| H | X | ↓ | $Q_n$ | NO CHANGE |

X: Don't Care

## LOGIC DIAGRAM




This logic diagram has not be used to estimate propagation delays

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | -0.5 to +7.0 | V |
| $V_I$ | DC Input Voltage | -0.5 to +7.0 | V |
| $V_O$ | DC Output Voltage | -0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | DC Input Diode Current | - 20 | mA |
| $I_{OK}$ | DC Output Diode Current | ± 20 | mA |
| $I_O$ | DC Output Current | ± 25 | mA |
| $I_{CC}$ or $I_{GND}$ | DC $V_{CC}$ or Ground Current | ± 50 | mA |
| $T_{stg}$ | Storage Temperature | -65 to +150 | °C |
| $T_L$ | Lead Temperature (10 sec) | 300 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.0 to 5.5 | V |
| $V_I$ | Input Voltage | 0 to 5.5 | V |
| $V_O$ | Output Voltage | 0 to $V_{CC}$ | V |
| $T_{op}$ | Operating Temperature | -40 to +85 | °C |
| dt/dv | Input Rise and Fall Time (see note 1) ($V_{CC}$ = 3.3 ± 0.3V)<br>($V_{CC}$ = 5.0 ± 0.5V) | 0 to 100<br>0 to 20 | ns/V<br>ns/V |

1) $V_{IN}$ from 30% to 70% of $V_{CC}$

## DC SPECIFICATIONS

| Symbol | Parameter | Test Conditions | | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | |
| $V_{IH}$ | High Level Input Voltage | 2.0 | | 1.5 | | | 1.5 | | V |
| | | 3.0 to 5.5 | | 0.7$V_{CC}$ | | | 0.7$V_{CC}$ | | |
| $V_{IL}$ | Low Level Input Voltage | 2.0 | | | | 0.5 | | 0.5 | V |
| | | 3.0 to 5.5 | | | | 0.3$V_{CC}$ | | 0.3$V_{CC}$ | |
| $V_{OH}$ | High Level Output Voltage | 2.0 | $I_O$=-50 µA | 1.9 | 2.0 | | 1.9 | | V |
| | | 3.0 | $I_O$=-50 µA | 2.9 | 3.0 | | 2.9 | | |
| | | 4.5 | $I_O$=-50 µA | 4.4 | 4.5 | | 4.4 | | |
| | | 3.0 | $I_O$=-4 mA | 2.58 | | | 2.48 | | |
| | | 4.5 | $I_O$=-8 mA | 3.94 | | | 3.8 | | |
| $V_{OL}$ | Low Level Output Voltage | 2.0 | $I_O$=50 µA | | 0.0 | 0.1 | | 0.1 | V |
| | | 3.0 | $I_O$=50 µA | | 0.0 | 0.1 | | 0.1 | |
| | | 4.5 | $I_O$=50 µA | | 0.0 | 0.1 | | 0.1 | |
| | | 3.0 | $I_O$=4 mA | | | 0.36 | | 0.44 | |
| | | 4.5 | $I_O$=8 mA | | | 0.36 | | 0.44 | |
| $I_I$ | Input Leakage Current | 0 to 5.5 | $V_I$ = 5.5V or GND | | | ±0.1 | | ±1.0 | µA |
| $I_{CC}$ | Quiescent Supply Current | 5.5 | $V_I$ = $V_{CC}$ or GND | | | 4 | | 40 | µA |

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

| Symbol | Parameter | Test Condition | | | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | $C_L$ (pF) | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | | Min. | Typ. | Max. | Min. | Max. | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay Time CK to Q | 3.3(*) | 15 | | | 7.2 | 11.0 | 1.0 | 13.0 | ns |
| | | 3.3(*) | 50 | | | 9.7 | 14.5 | 1.0 | 16.5 | |
| | | 5.0(**) | 15 | | | 4.9 | 7.2 | 1.0 | 8.5 | |
| | | 5.0(**) | 50 | | | 6.4 | 9.2 | 1.0 | 10.5 | |
| $t_{PHL}$ | Propagation Delay Time $\overline{CLR}$ to Q | 3.3(*) | 15 | | | 7.4 | 11.4 | 1.0 | 13.5 | ns |
| | | 3.3(*) | 50 | | | 9.9 | 14.9 | 1.0 | 17.0 | |
| | | 5.0(**) | 15 | | | 5.1 | 7.6 | 1.0 | 9.0 | |
| | | 5.0(**) | 50 | | | 6.6 | 9.6 | 1.0 | 11.0 | |
| $t_w$ | $\overline{CLR}$ pulse Width LOW | 3.3(*) | | | | | 5.0 | | 5.0 | ns |
| | | 5.0(**) | | | | | 5.0 | | 5.0 | |
| $t_w$ | CK pulse Width HIGH r LOW | 3.3(*) | | | | | 5.0 | | 5.0 | ns |
| | | 5.0(**) | | | | | 5.0 | | 5.0 | |
| $t_s$ | Setup Time D to CK HIGH or LOW | 3.3(*) | | | | | 5.0 | | 6.0 | ns |
| | | 5.0(**) | | | | | 4.5 | | 4.5 | |
| $t_h$ | Hold Time D to CK HIGH or LOW | 3.3(*) | | | | | 0.0 | | 0.0 | ns |
| | | 5.0(**) | | | | | 0.5 | | 0..5 | |
| $t_{REM}$ | Removal Time $\overline{CLR}$ to CK | 3.3(*) | | | | | 3.0 | | 3.0 | ns |
| | | 5.0(**) | | | | | 2.5 | | 2.5 | |
| $f_{MAX}$ | Maximum Clock Frequency | 3.3(*) | 15 | | 95 | 150 | | 80 | | MHz |
| | | 3.3(*) | 50 | | 55 | 85 | | 50 | | |
| | | 5.0(**) | 15 | | 130 | 175 | | 110 | | |
| | | 5.0(**) | 50 | | 90 | 120 | | 80 | | |

(*) Voltage range is 3.3V ± 0.3V
(**) Voltage range is 5V ± 0.5V

## CAPACITIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | Min. | Typ. | Max. | Min. | Max. | |
| $C_{IN}$ | Input Capacitance | | | 4 | 10 | | 10 | pF |
| $C_{PD}$ | Power Dissipation Capacitance (note 1) | | | 29 | | | | pF |

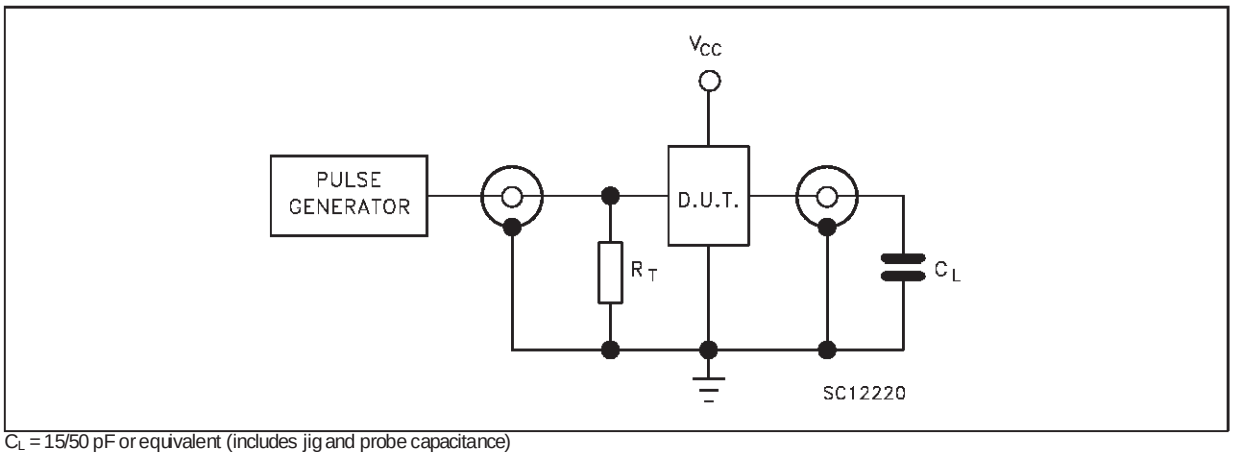
1) $C_{PD}$ is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/6$ (per Flip-Flop)

## DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Parameter | Test Conditions | | Value | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ (V) | | $T_A$ = 25 °C | | | -40 to 85 °C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | |
| $V_{OLP}$ | Dynamic Low Voltage Quiet Output (note 1, 2) | 5.0 | $C_L$ = 50 pF | | 0.3 | 0.8 | | | V |
| $V_{OLV}$ | | | | -0.8 | -0.3 | | | | |
| $V_{IHD}$ | Dynamic High Voltage Input (note 1, 3) | 5.0 | | 3.5 | | | | | |
| $V_{ILD}$ | Dynamic Low Voltage Input (note 1, 3) | 5.0 | | | | 1.5 | | | |

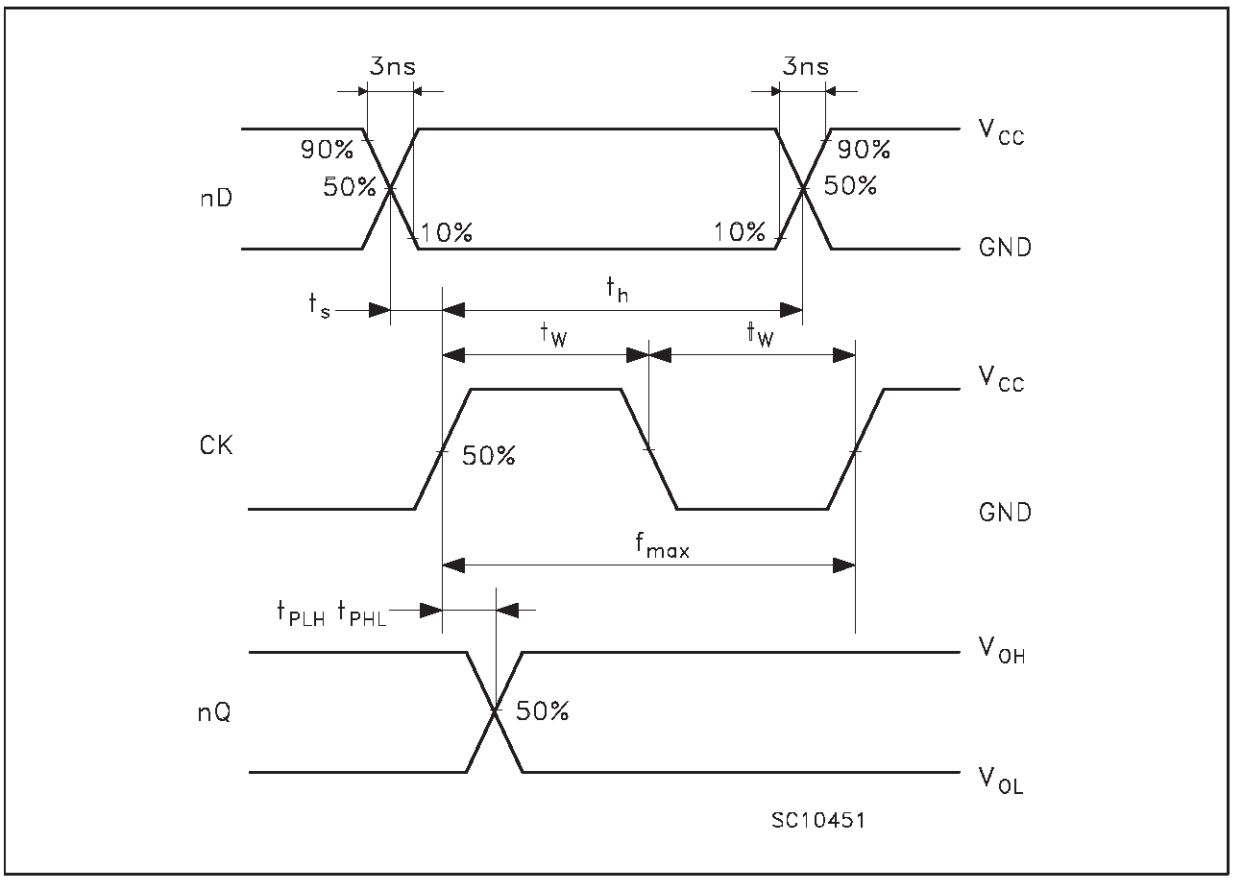
1) Worst case package.
2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n -1) outputs switching and one output at GND.
3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$), f=1MHz.

## TEST CIRCUIT

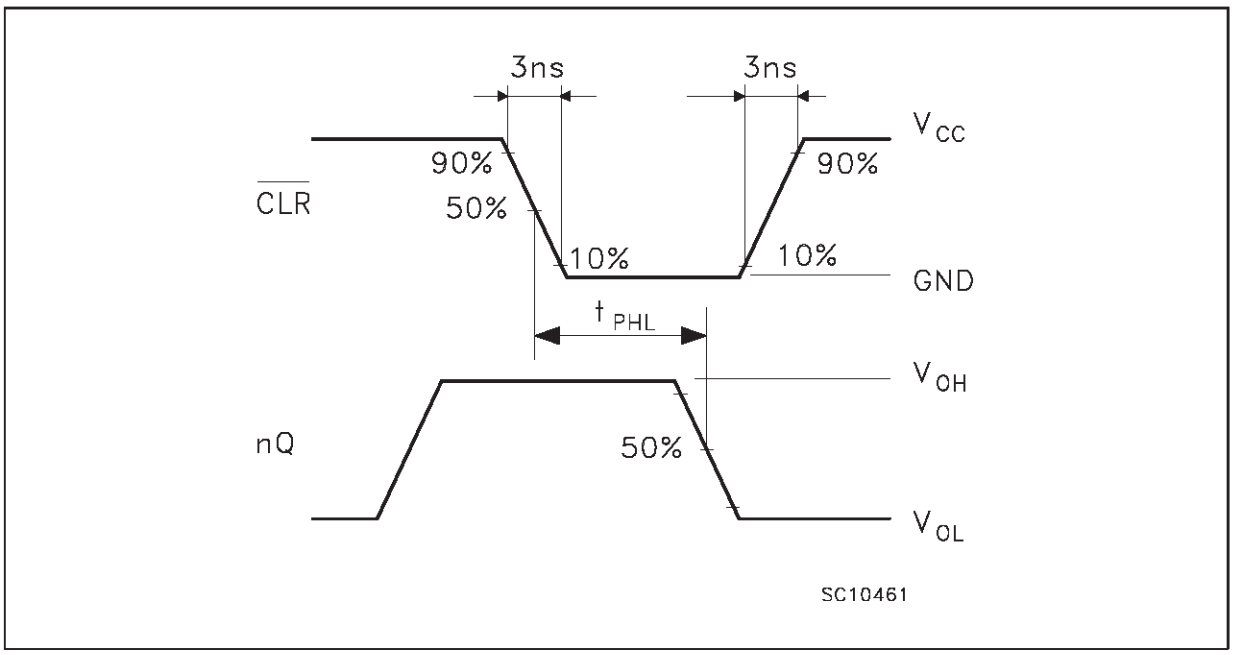



$C_L$ = 15/50 pF or equivalent (includes jig and probe capacitance)
$R_T$ = $Z_{OUT}$ of pulse generator (typically 50Ω)

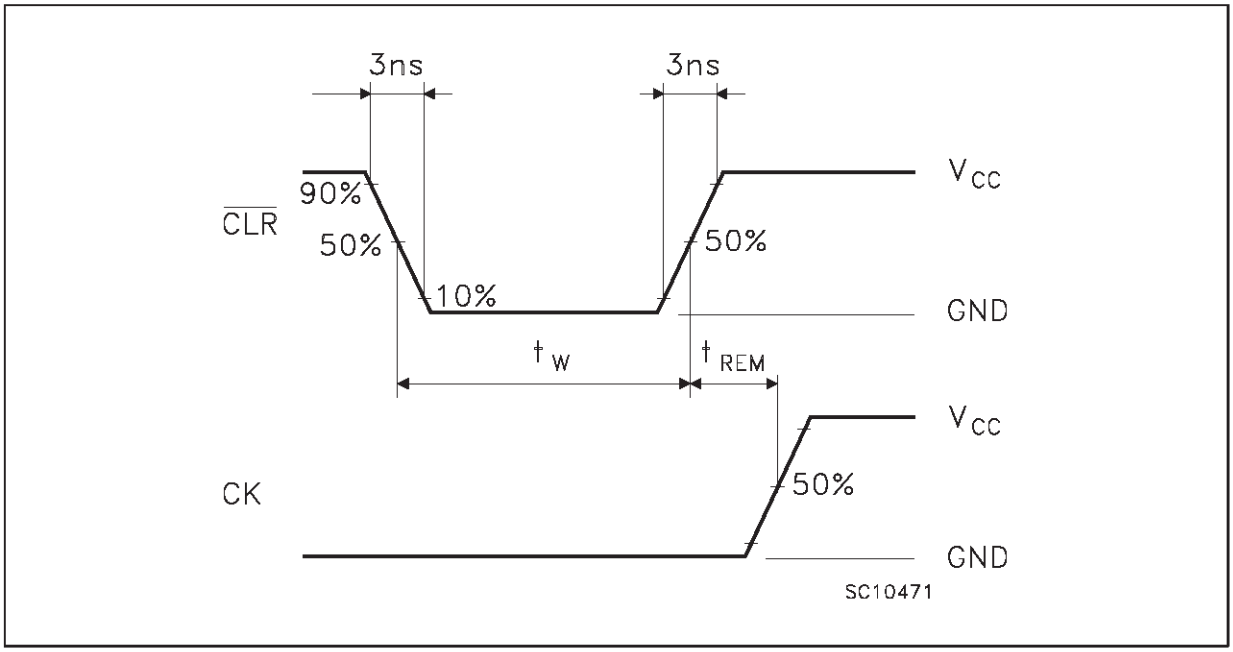
**WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES** (f=1MHz; 50% duty cycle)



**WAVEFORM 2: PROPAGATION DELAYS** (f=1MHz; 50% duty cycle)

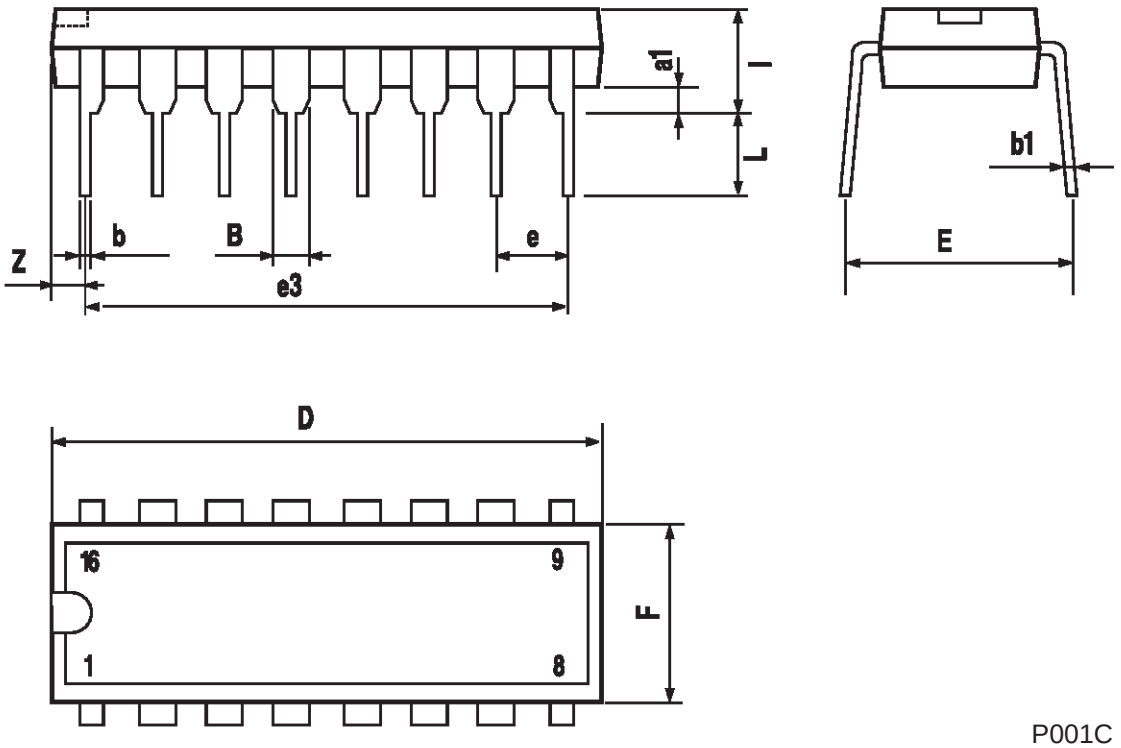



**WAVEFORM 3: RECOVERY TIME** (f=1MHz; 50% duty cycle)



## Plastic DIP-16 (0.25) MECHANICAL DATA

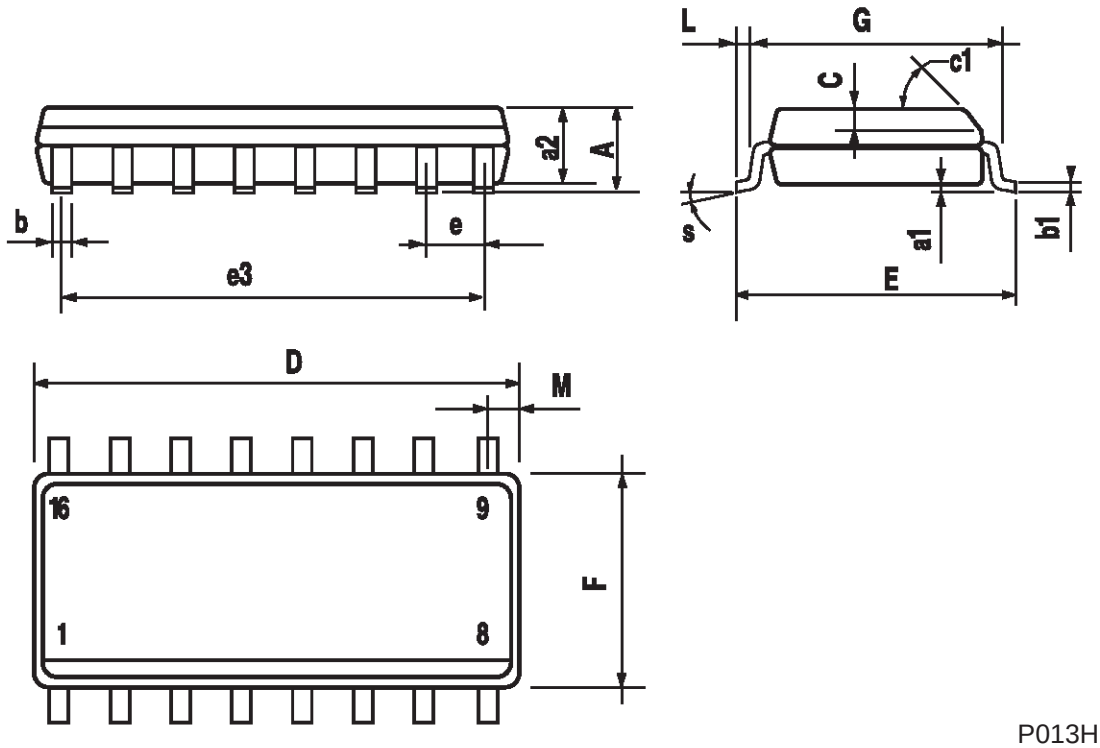
| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.51 | | | 0.020 | | |
| B | 0.77 | | 1.65 | 0.030 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 17.78 | | | 0.700 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.27 | | | 0.050 |




P001C

## SO-16 MECHANICAL DATA

| DIM. | mm | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.2 | 0.004 | | 0.007 |
| a2 | | | 1.65 | | | 0.064 |
| b | 0.35 | | 0.46 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.019 | |
| c1 | 45 (typ.) | | | | | |
| D | 9.8 | | 10 | 0.385 | | 0.393 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F | 3.8 | | 4.0 | 0.149 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.208 |
| L | 0.5 | | 1.27 | 0.019 | | 0.050 |
| M | | | 0.62 | | | 0.024 |
| S | 8 (max.) | | | | | |

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