FAIRCHILD SEMICONDUCTOR™

April 1994
Revised April 1999

74VHC4316
Quad Analog Switch with Level Translator

General Description

These devices are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Three supply pins are provided on the 4316 to implement a level translator which enables this circuit to operate with 0V–6V logic levels and up to ±6V analog switch levels. The 4316 also has a common enable input in addition to each switch's control which when HIGH will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 20 ns
- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. (V_{CC}–V_{EE} = 4.5V)
  30 typ. (V_{CC}–V_{EE} = 9V)
- Low quiescent current: 80 µA maximum (74VHC)
- Matched switch characteristics
- Individual switch controls plus a common enable
- Pin functional compatible with 74HC4316

Ordering Code:

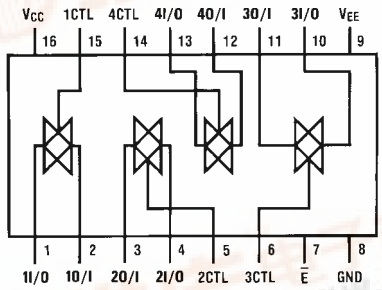
Order Number	Package Number	Package Description
74VHC4316M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74VHC4316WM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74VHC4316MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC4316N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Truth Table

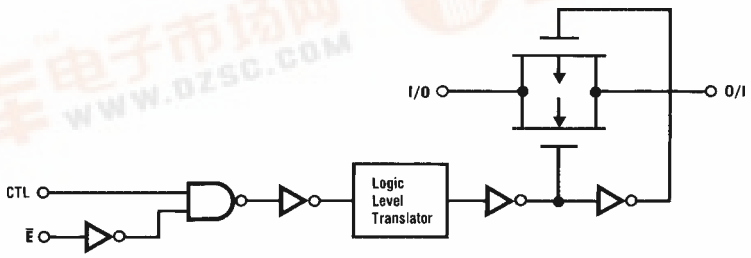
Inputs		Switch
$\overline{E}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"

Connection Diagram



Top View

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
Supply Voltage (V_{EE})		0	−6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temperature Range (T_A)		−40	+85	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns
	V_{CC} = 12.0V		250	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C	T_A = −40°C to +85°C		Units
					Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH			2.0V		1.5	1.5	
	Level Input			4.5V		3.15	3.15	V
	Voltage			6.0V		4.2	4.2	
V_{IL}	Maximum LOW			2.0V		0.5	0.5	
	Level Input			4.5V		1.35	1.35	V
	Voltage			6.0V		1.8	1.8	
R_{ON}	Minimum "ON"	V_{CTL} = V_{IH},	GND	4.5V	100	170	200	Ω
	Resistance	I_S = 2.0 mA	−4.5V	4.5V	40	85	105	
	(Note 5)	V_{IS} = V_{CC} to V_{EE}	−6.0V	6.0V	30	70	85	
		(*Figure 1*)						
		V_{CTL} = V_{IH},	GND	2.0V	100	180	215	
		I_S = 2.0 mA	GND	4.5V	40	80	100	
		V_{IS} = V_{CC} or V_{EE}	−4.5V	4.5V	50	60	75	
		(*Figure 1*)	−6.0V	6.0V	20	40	60	
R_{ON}	Maximum "ON"	V_{CTL} = V_{IH}	GND	4.5V	10	15	20	
	Resistance	V_{IS} = V_{CC} to V_{EE}	−4.5V	4.5V	5	10	15	Ω
	Matching		−6.0V	6.0V	5	10	15	
I_{IN}	Maximum Control Input Current	V_{IN} = V_{CC} or GND	GND	6.0V		±0.1	±1.0	µA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS} = V_{CC} or V_{EE}						
		V_{IS} = V_{EE} or V_{CC}	GND	6.0V		±30	±300	nA
		V_{CTL} = V_{IL}	−6.0V	6.0V		±50	±500	
		(*Figure 2*)						
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{IS} = V_{CC} to V_{EE}						
		V_{CTL} = V_{IH},	GND	6.0V		±20	±75	nA
		V_{OS} = OPEN	−6.0V	6.0V		±30	±150	
		(*Figure 3*)						
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	GND	6.0V		1.0	10	µA
		I_{OUT} = 0 µA	−6.0V	6.0V		4.0	40	

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for VHC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V – 6.0V, V_{EE} = 0V – 6V, C_L = 50 pF unless otherwise specified

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A=+25°C		T_A=−40°C to +85°C	Units
					Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation		GND	3.3V	15	30	37	
	Delay Switch In to		GND	4.5V	5	10	13	ns
	Out		–4.5V	4.5V	4	8	12	
			–6.0V	6.0V	3	7	11	
t_{PZL}, t_{PZH}	Maximum Switch Turn	R_L = 1 kΩ	GND	3.3V	25	97	120	
	"ON" Delay		GND	4.5V	20	35	43	ns
	(Control)		–4.5V	4.5V	15	32	39	
			–6.0V	6.0V	14	30	37	
t_{PHZ}, t_{PLZ}	Maximum Switch Turn	R_L = 1 kΩ	GND	3.3V	35	145	180	
	"OFF" Delay		GND	4.5V	25	50	63	ns
	(Control)		–4.5V	4.5V	20	44	55	
			–6.0V	6.0V	20	44	55	
t_{PZL}, t_{PZH}	Maximum Switch		GND	3.3V	27	120	150	
	Turn "ON" Delay		GND	4.5V	20	41	52	ns
	(Enable)		–4.5V	4.5V	19	38	48	
			–6.0V	6.0V	18	36	45	
t_{PLZ}, t_{PHZ}	Maximum Switch		GND	3.3V	42	155	190	
	Turn "OFF" Delay		GND	4.5V	28	53	67	ns
	(Enable)		–4.5V	4.5V	23	47	59	
			–6.0V	6.0V	21	47	59	
	Minimum Frequency	R_L = 600Ω, V_{IS} = $2V_{PP}$	0V	4.5	40			
	Response (*Figure 7*)	at (V_{CC}–V_{EE}/2)	–4.5V	4.5V	100			MHz
	20 log (V_{OS}/V_{IS})= –3 dB	(Note 6)(Note 7)						
	Control to Switch	R_L = 600Ω, f = 1 MHz	0V	4.5V	100			
	Feedthrough Noise	C_L = 50 pF	–4.5V	4.5V	250			mV
	(*Figure 8*)	(Note 7)(Note 8)						
	Crosstalk Between	R_L = 600Ω, f = 1 MHz	0V	4.5V	–52			
	any Two Switches		–4.5V	4.5V	–50			dB
	(*Figure 9*)							
	Switch OFF Signal	R_L = 600Ω, f = 1 MHz						
	Feedthrough	V_{CTL} = V_{IL}	0V	4.5V	–42			dB
	Isolation		–4.5V	4.5V	–44			
	(*Figure 10*)	(Note 7)(Note 8)						
THD	Sinewave Harmonic	R_L = 10 KΩ, C_L = 50 pF,						
	Distortion	f = 1 KHz						%
	(*Figure 11*)	V_{IS} = 4 V_{PP}	0V	4.5V	0.013			
		V_{IS} = 8 V_{PP}	–4.5V	4.5V	0.008			
C_{IN}	Maximum Control				5			pF
	Input Capacitance							
C_{IN}	Maximum Switch				35			pF
	Input Capacitance							
C_{IN}	Maximum Feedthrough	V_{CTL} = GND			0.5			pF
	Capacitance							
C_{PD}	Power Dissipation				15			pF
	Capacitance							

Note 6: Adjust 0 dBm for f = 1 kHz (Null R_L/Ron Attenuation).

Note 7: V_{IS} is centered at V_{CC}–V_{EE}/2.

Note 8: Adjust for 0 dBm.

AC Test Circuits and Switching Time Waveforms

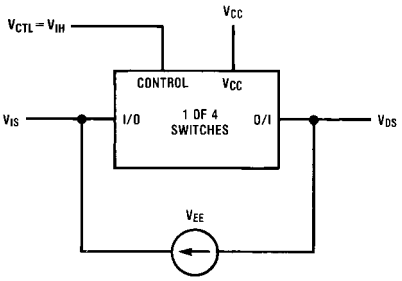


FIGURE 1. "ON" Resistance

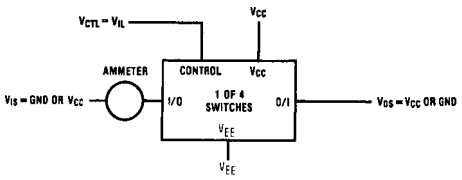


FIGURE 2. "OFF" Channel Leakage Current

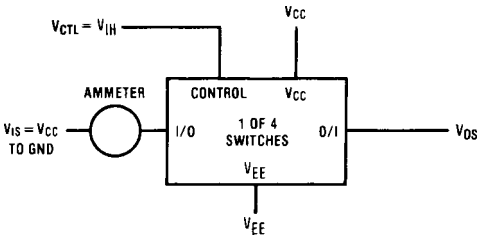


FIGURE 3. "ON" Channel Leakage Current

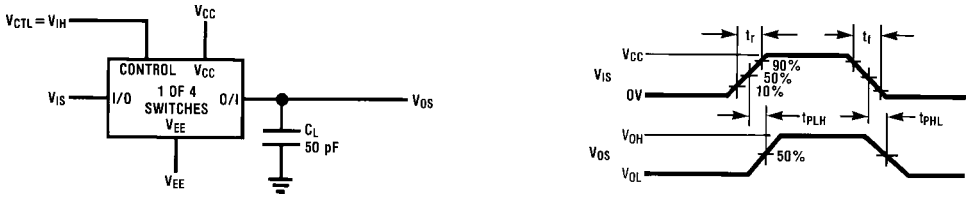


FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

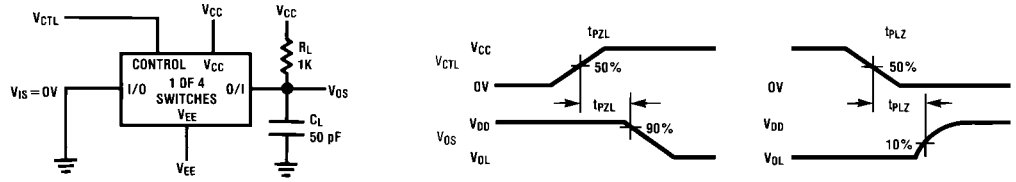


FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

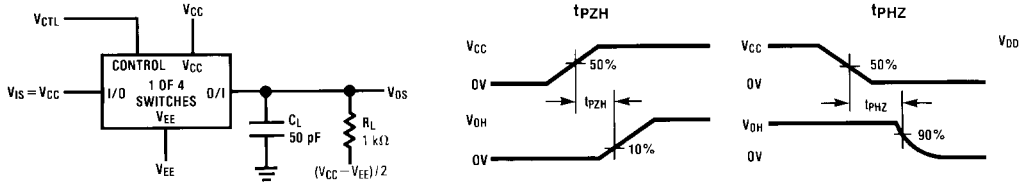


FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

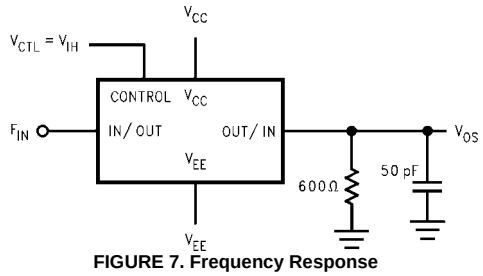


FIGURE 7. Frequency Response

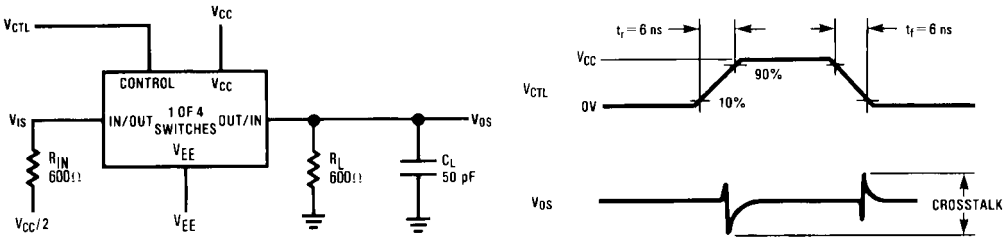


FIGURE 8. Crosstalk: Control Input to Signal Output

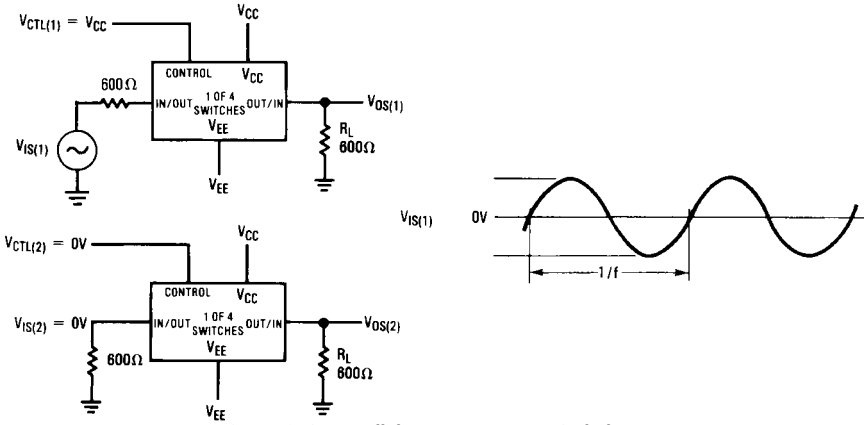


FIGURE 9. Crosstalk between Any Two Switches

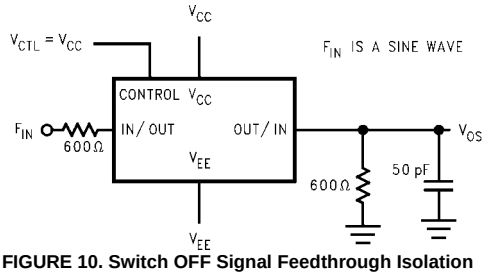


FIGURE 10. Switch OFF Signal Feedthrough Isolation

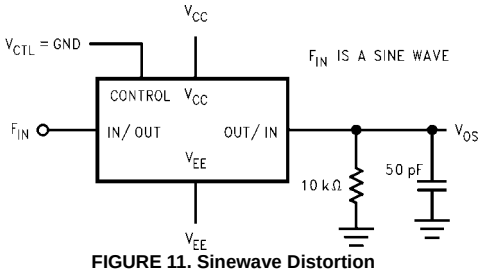
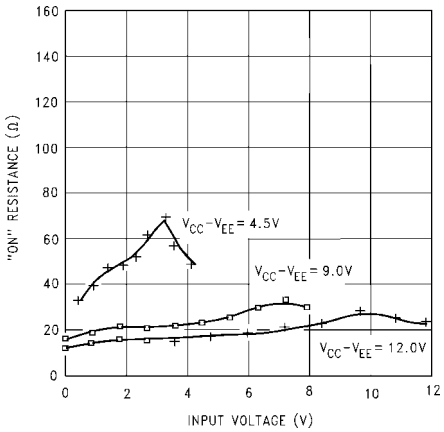


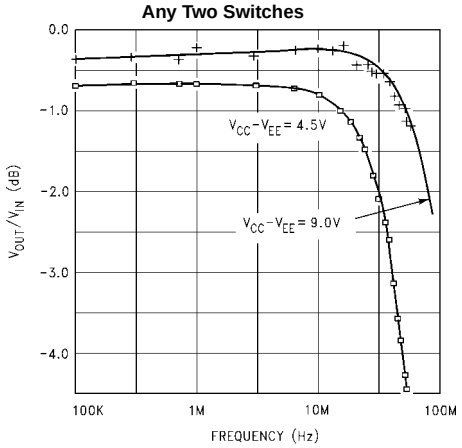
FIGURE 11. Sinewave Distortion

Typical Performance Characteristics

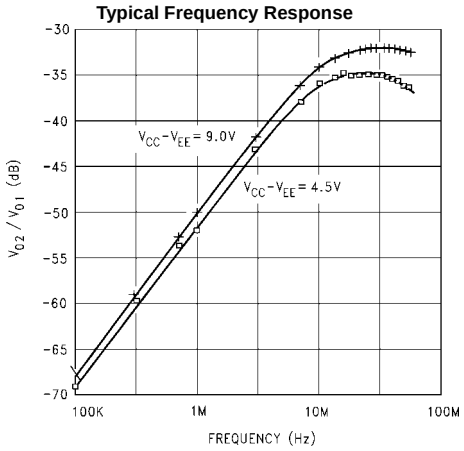
Typical "ON" Resistance



Typical Crosstalk between Any Two Switches



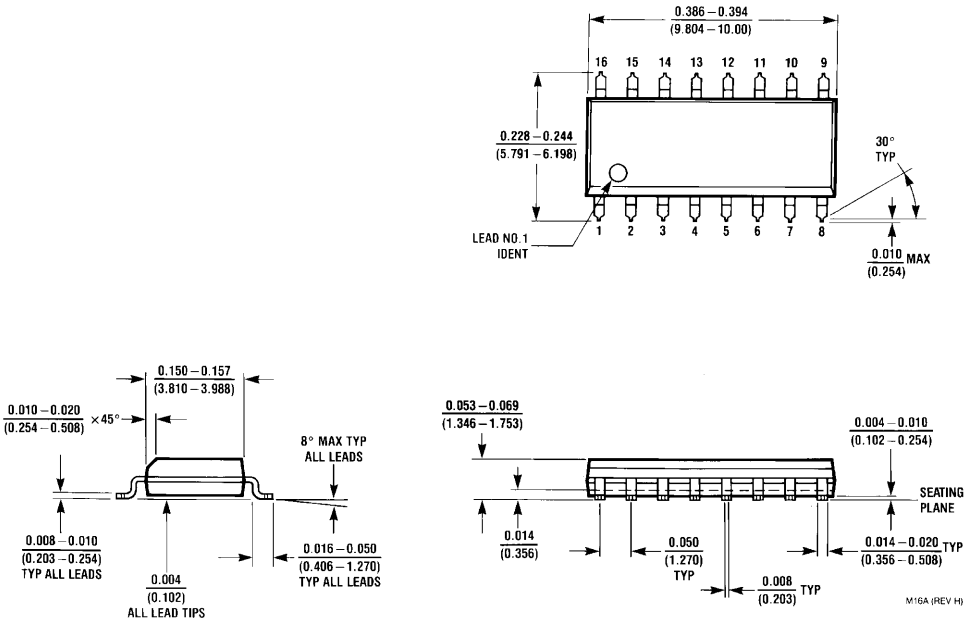
Typical Frequency Response



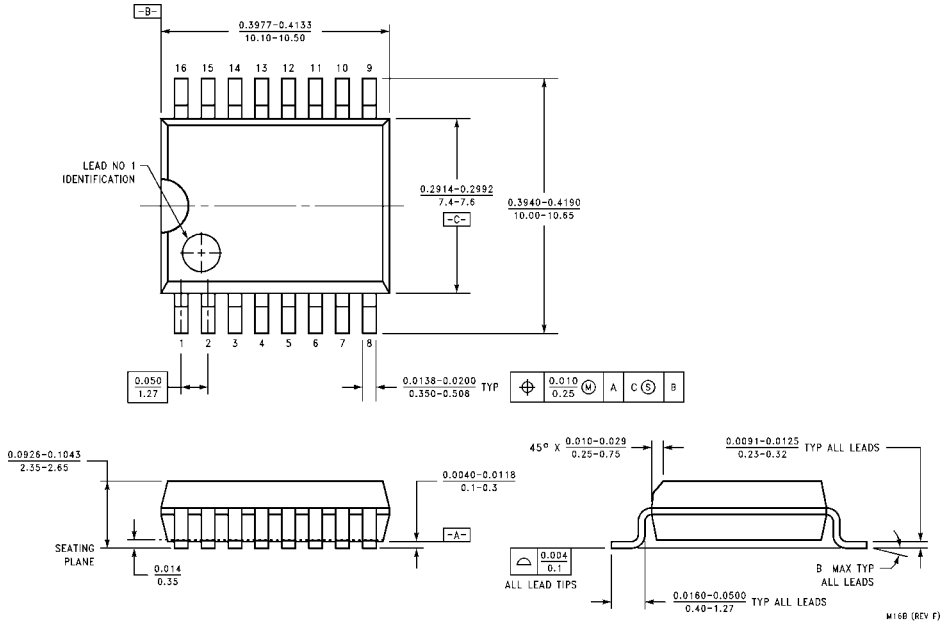
Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).

Physical Dimensions inches (millimeters) unless otherwise noted

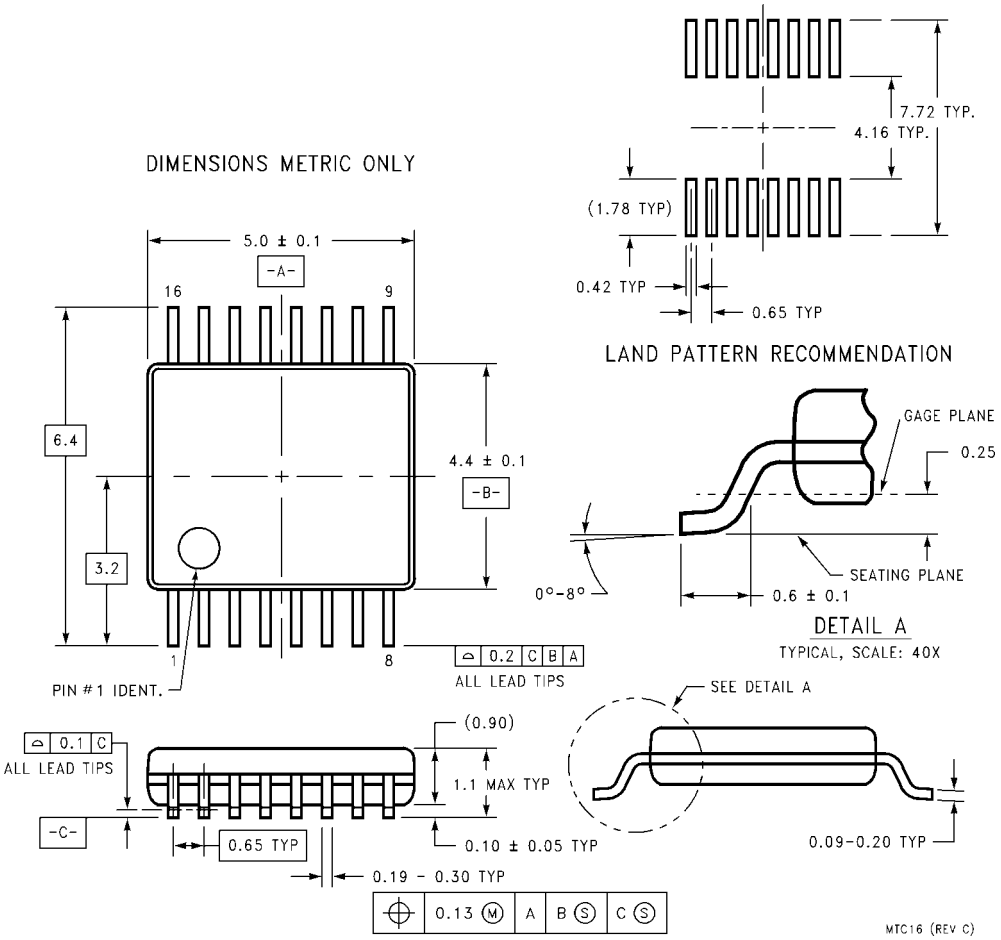


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A



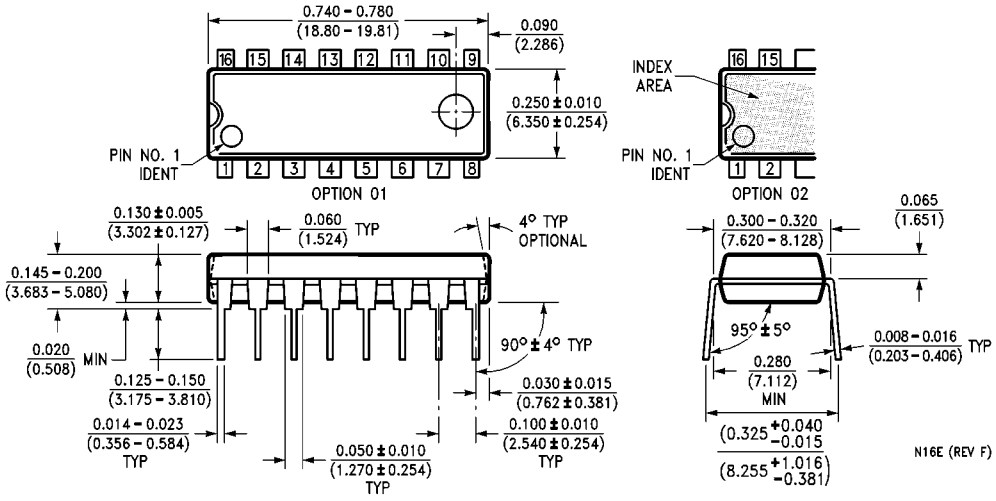
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M16B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E